VMIVME-6000

1553 COMMUNICATIONS INTERFACE BOARD

PRODUCT MANUAL

DOCUMENT NO. 500-006000-000 E

Revised September 30, 1999

VMIC
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
(256) 880-0444 Fax: (256) 882-0859
1-800-322-3616

COPYRIGHT AND TRADEMARKS

(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	09/09/93	Release	93-0712
B	10/26/93	Changed pages ii, and 3-2 per ECO	94-0070
C	11/20/97	Changed pages ii, viii, and Section 4 pages 4-124, 4-137, 4-153, 4-160, 4-161, 4-166, and 4-173	97-0778
D	02/05/99	Change pages ii and 4-165	99-0116
E	09/30/99	Cover, pages ii and 4-186	99-0786

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VMIC ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

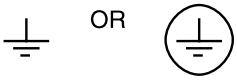
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

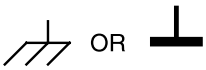
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



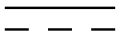
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

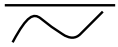


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-6000
1553 COMMUNICATIONS INTERFACE BOARD

TABLE OF CONTENTS

VMIVME-6000
1553 COMMUNICATIONS INTERFACE BOARD

TABLE OF CONTENTS (CONTINUED)

VMIVME-6000
1553 COMMUNICATIONS INTERFACE BOARD

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

SECTION 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The VMIVME-6000 is a microprogrammed MIL-STD-1553 interface specifically for VMEbus computers. The VMIVME-6000 is a single 6U VMEbus printed circuit board that requires only one backplane slot for operation. The 1553 bus may be customer selected (by jumpers) to be accessible through the VMEbus P2 connector or through the front panel of the board.

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-6000 can function as a Bus Controller/Simulator, Multiple Remote Terminal and/or Monitor. The VMIVME-6000 is based on a microprogram-driven CMOS ASIC chip set that provides the versatility needed by tester and simulator environments, while meeting the needs of todays system power, space, and reliability requirements. The board provides 128 k x 16-bits of on-board RAM for constructing control blocks and storing transmitted and received 1553 data. Once initialized by the host, the VMIVME-6000 on-board processor can retrieve and store all control block data and commands needed for 1553 operation. The board also provides two levels of maskable interrupts to allow flexible data and exception processing. The VMIVME-6000 is compatible with the protocol of 1553B, 1553A, as well as F16, and F18 derivatives of these specifications. A block diagram of the VMIVME-6000 is shown in Figure 1.2-1.

The VMIVME-6000 VMEbus slave interface supports standard byte and word transfers. All byte accesses to the I/O registers must be done as Even/Odd since the registers are word (16-bits) length. Longword accesses to the on-board registers or memory will cause a Bus Error.

During Interrupt Acknowledge cycles, the VMIVME-6000 supports Release-on-Acknowledge (ROAK). The board will provide a 16-bit interrupt vector (programmable by the host) during the cycle.

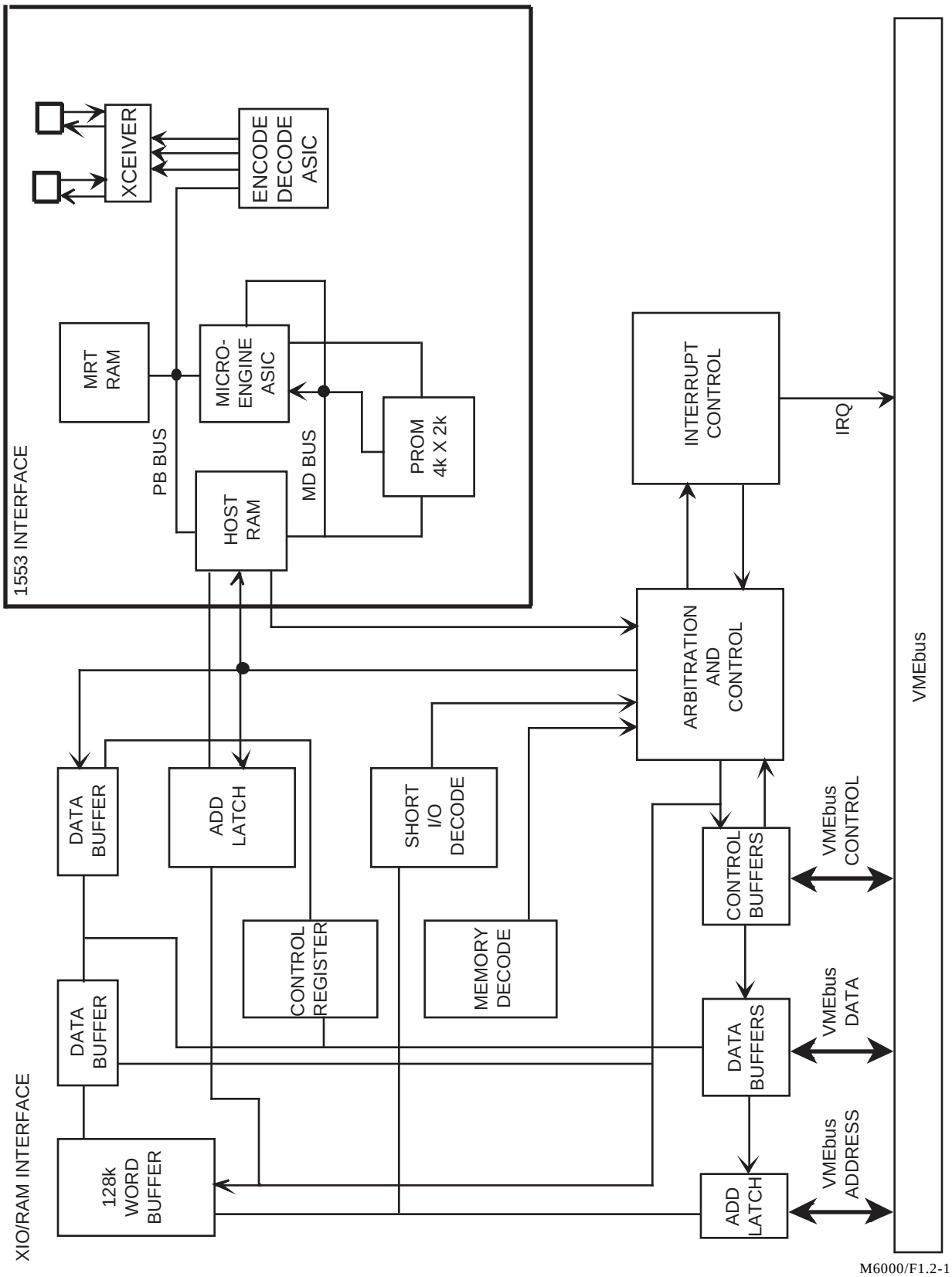


Figure 1.2-1. VMIVME-6000 Block Diagram

1.3 REFERENCE MATERIAL LIST

The reader should refer to The VMEbus Specification for a detailed explanation fo the VMEbus. The VMEbus Specification is available from the following source:

VITA
VFEA International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

For general information regarding the Aircraft Internal Time Division Command/Response Multiplex Databus, refer to the following documents:

MIL-STD-1553B
MIL-HDBK-1553B

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-006000-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-6000 is a single-slot, 6U Eurocard form factor MIL-STD-1553 simulator board for the VMEbus. The host interacts with the VMIVME-6000 through Configuration registers located in short I/O space to execute External Input/Output (XIO) commands, and by constructing Control Blocks (CBs) in the 128 k x 16 bit on-board memory located in standard addressing space. There is an extra 8 k x 16 bit MRT/MON mode memory (accessible through the XIO commands) which is used by the microprogram-driven CMOS ASIC chip set to access the host and ASIC supplied 1553 MRT/MON mode.

3.2 VMEbus INTERFACE

The VMIVME-6000 VMEbus slave interface has six word-length I/O Configuration register locations that are accessible by the host. These registers may be mapped on the VMEbus starting at address C000H of the short I/O space, in 64-byte increments. The VMEbus base address of these I/O registers is programmable on the header marked as E1 through E9. The Address Offset register in this short I/O space is used to offset the base address of the 128 k x 16-bit memory. This allows configuration of the memory space through software. The details of the I/O configuration registers are shown in Section 4.2. The 128 k x 16-bit memory supports standard (A24), (D16) addressing and will respond to address modifiers 3DH, 39H, 2DH, 29H.

3.3 REGISTERS AND MEMORY

The VMIVME-6000 Configuration registers take one VMEbus cycle in order to complete the access because they are accessed directly. The XIO registers, which are located in the ASICs, are accessed indirectly using a polling method involving the XIO Address and XIO Data registers. Basically, a read cycle consists of writing to the XIO Address register and polling a status bit until the ASIC micro-engine has a chance to write the data to the XIO Data registers at which time the host can read the valid data. An XIO write cycle consists of writing the XIO Address and Data registers and polling to verify completion.

The 8 k x 16 MRT/MON RAM is accessed indirectly from the MRT/MON RAM Address and Data XIO Registers, a type of double indirect method. The MRT/MON RAM contains information about the 32 possible RTs. The 128 k x 16-bit SRAM memory is located in standard addressing space and contains the Control Block information used by the 1553 micro-engine to control the board.

This memory is where all data that is transmitted and received will be located. Data pointers are used to locate the data buffers and an easy-to-use buffer linking method allows the user to extend the buffering to double, triple, etc. buffering.

3.4 1553 CONTROL

The VMIVME-6000 uses a custom 8 MIPs microengine interfaced to a 1553 encoder/decoder and the on-board memory to perform the intended 1553 processing. The simulator mode uses Control Blocks in memory that are strung together using either linked lists or table look-up methods. The VMIVME-6000 can simulate responses of RTs that are not present, inject and detect errors, and posts all pertinent information in memory.

MRT/MON mode simulates or monitors up to 32 remote terminals while supporting different aircraft protocol in different simulated RTs, error injection and detection, and buffering all information associated with each message.

SECTION 4

PROGRAMMING

4.1 PROGRAMMING THE VMIVME-6000

The VMIVME-6000 is programmed by accessing configuration registers to execute External Input/Output (XIO) commands, and by constructing Control Blocks (CB's) in static RAM. Once the board is programmed and started, it operates out of the on-board memory without host intervention. The VMIVME-6000 consists of several groups of registers and memory that are used to configure and control the board. These groups and their relationships are shown in Figure 4.1-1. The Configuration registers are located in short I/O space. Two XIO registers, the XIO Address register and XIO Data register, are used to access the XIO registers themselves. Two XIO registers, the MRT/MON RAM Address and Data registers, are used to access the MRT/MON RAM. Control Blocks for the different modes are set up in the 128 k x 16 static RAM. This block of memory is located in VMEbus standard addressing space. The A and B interrupts are controlled by various registers and memory locations in the previously mentioned groups.

The following five sections will describe the registers, memory, and programming features:

4.2 REGISTERS
4.3 OPERTIONAL MODES
4.4 EXTERNAL MRT/MON RAM
4.5 INTERRUPTS
4.6 ERROR INJECTION

Various aspects are covered in multiple sections due to the fact that the sections are so interrelated.

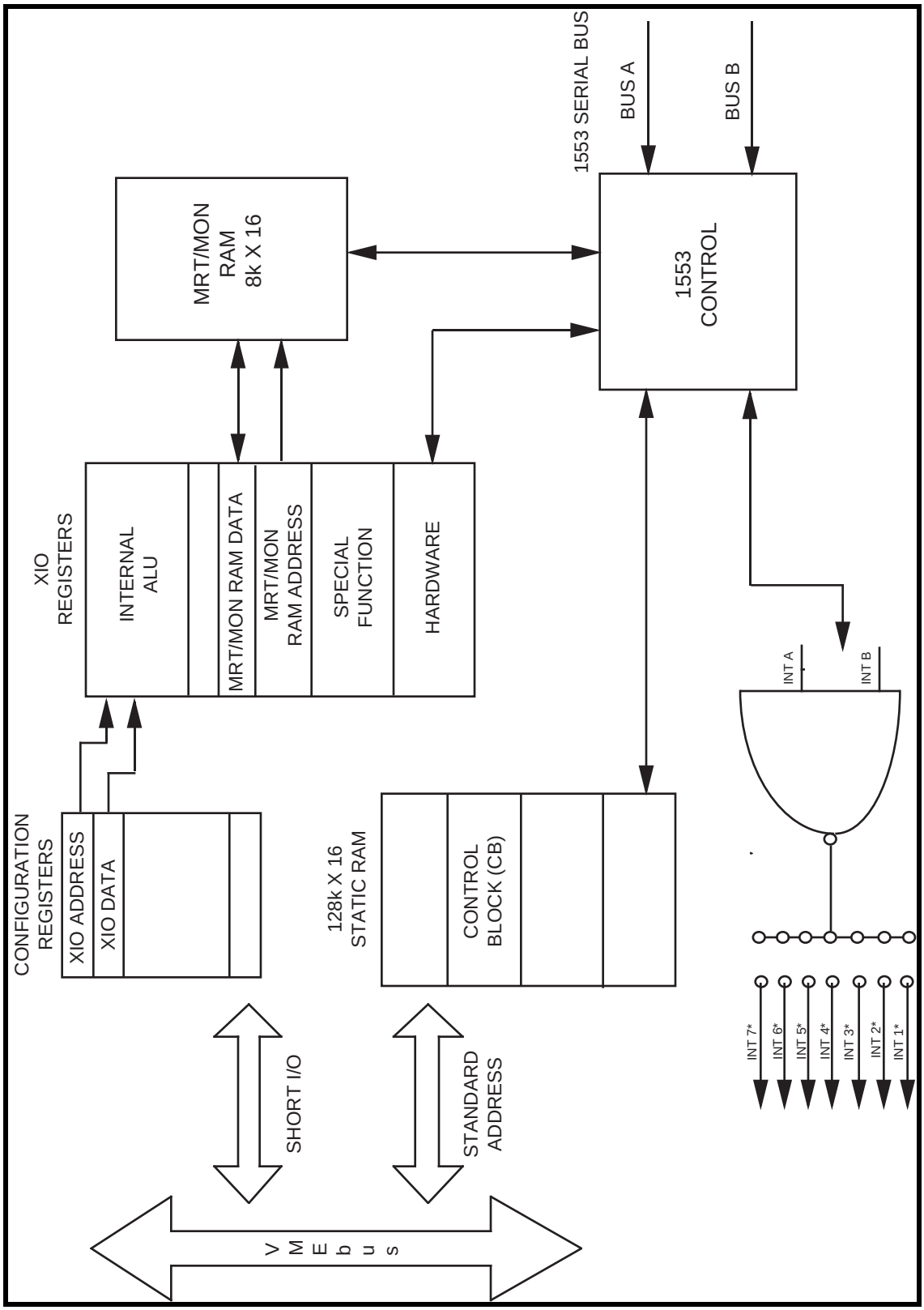


Figure 4.1-1. VMIVME-6000 Programming Block Diagram

4.2 REGISTERS

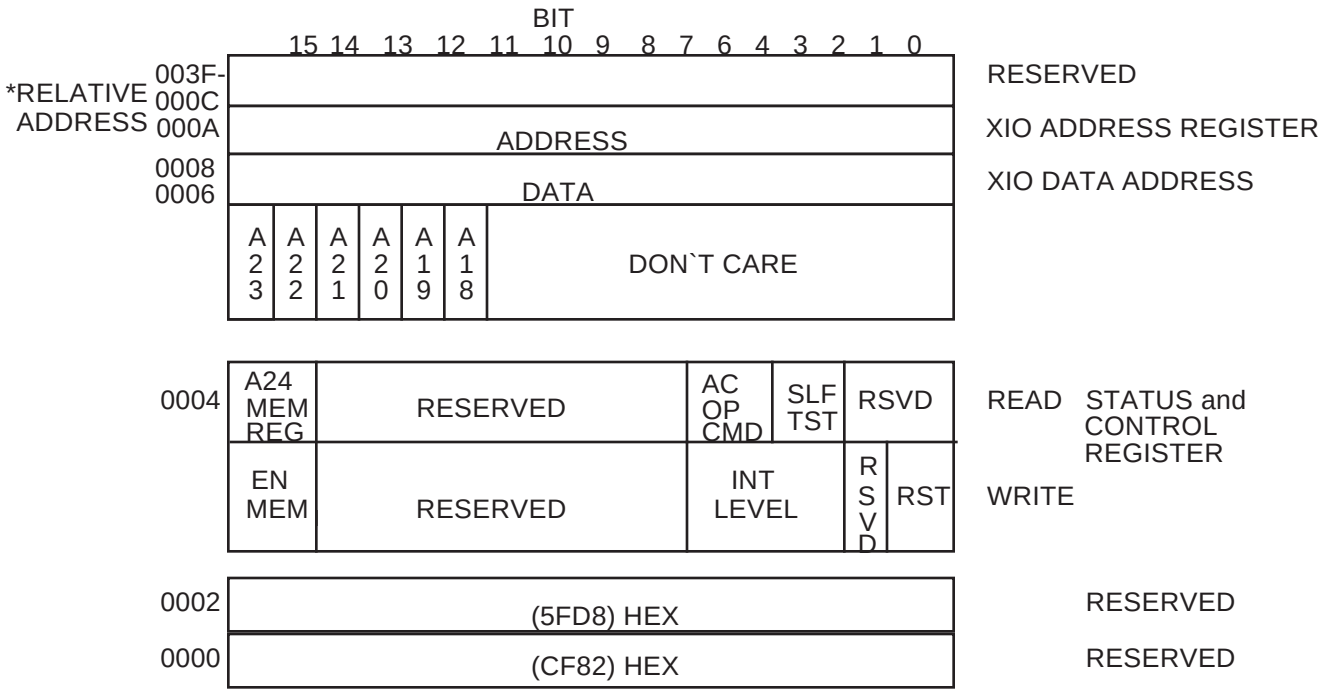
The registers section will describe the configuration registers and the External Input/Output (XIO) registers and all their bit level definitions. The XIO address and XIO Data Configuration registers are used to access the XIO registers themselves. Figure 4.1-1 shows that a pair of XIO registers, the MRT/MON RAM address and data registers are used to access the MRT/MON RAM, but the MRT/MON RAM will be described in Section 4.4, EXTERNAL MRT/MON RAM. The Control Block structures for the on-board RAM will be discussed in Section 4.3, OPERATIONAL MODES. The VMIVME-6000 is programmed by accessing the VMIVME-6000 slave configuration registers located in short I/O space to execute External Input/Output (XIO) commands, and by constructing Control Blocks (CBs) in the 128 k x 16-bit on-board memory located in standard addressing space. Once the Board is programmed and started, it operates out of the on-board memory without host intervention. This section will deal with the Configuration registers and XIO commands.

The registers section is comprised of the following sections:

The registers section will contain a description of the particular register group and will be followed by a page for each register describing it in detail.

4.2.1 Configuration Registers

The VMIVME-6000 has 6-word length registers mapped in the short I/O space of the VMEbus, as shown in Figure 4.2-1. These registers are used by the host to program and obtain control and status information to/from the board during operation.



* ADDRESS RELATIVE TO SHORT I/O JUMPER SETTINGS.

M6000/F4.2-1

Figure 4.2-1. VMIVME-6000 Configuration Registers

Name: **Status and Control Register**
Address: **Base Address + 0004 (Hex)**
Address Space: **VMEbus short I/O**
Type: **Read (Status) / Write (Control)**

Description: A READ of this register will provide the host status of the VMIVME-6000 as defined below:

BIT 15 A logic "one" indicates the A24 memory registers can be accessed.

BITS14-4 Reserved.

BIT 3 This bit (logic "one") indicates that the board is ready to accept its full set of operational commands.

BIT 2 A logic "one" in this bit indicates the Board passed its self-test.

BITS1-0 Reserved, set to zero

Description: Host WRITES to this register cause specific actions to be executed.

BIT 15 A logic "one" written to this bit will enable reads and writes to the on-board memory by the host. A logic "zero" disables memory.

BITS14-5 Reserved, set to zero

BITS4-2 Are written by the host to match the selected interrupt level of headers E10 - E17. The 3 bits (2 through 4) form a BCD indication of the level, and are compared to A03, A02, and A01.

BIT 1 Reserved, set to zero

BIT 0 Writing a logic "one" to this bit will reset all on-board logic.

Name: **Offset Register**
Address: **Base Address + 0006 (Hex)**
Address Space: **VMEbus short I/O**
Type: **Read / Write**

Description: The Offset Register is programmed by the host to select the A24 VMEbus address of the on-board memory. Bit 15 of the register corresponds to address line A23, while bit 10 corresponds to address line A18. As an example, if the host wants the 256 kbytes of memory to start at $100000, the Offset Register would be programmed to 10XX where the Xs are "don't cares".

BIT 15 A23
BIT 14 A22
BIT 13 A21
BIT 12 A20

BIT 11 A19
BIT 10 A18
BIT 9 Don`t Care, set to logic "zero"
BIT 8 Don`t Care, set to logic "zero"

BIT 7 Don`t Care, set to logic "zero"
BIT 6 Don`t Care, set to logic "zero"
BIT 5 Don`t Care, set to logic "zero"
BIT 4 Don`t Care, set to logic "zero"

BIT 3 Don`t Care, set to logic "zero"
BIT 2 Don`t Care, set to logic "zero"
BIT 1 Don`t Care, set to logic "zero"
BIT 0 Don`t Care, set to logic "zero"

Name: **XIO Data Register**
Address: **Base Address + 0008 (Hex)**
Address Space: **VMEbus short I/O**
Type: **Read/Write**

Description: All data accesses to the XIO Registers (READ and WRITE) must be through this register. Before accessing this register, the address of the XIO to be executed must be written to the XIO Address Register.

BIT 15 Data Bit 15
BIT 14 Data Bit 14
BIT 13 Data Bit 13
BIT 12 Data Bit 12

BIT 11 Data Bit 11
BIT 10 Data Bit 10
BIT 9 Data Bit 9
BIT 8 Data Bit 8

BIT 7 Data Bit 7
BIT 6 Data Bit 6
BIT 5 Data Bit 5
BIT 4 Data Bit 4

BIT 3 Data Bit 3
BIT 2 Data Bit 2
BIT 1 Data Bit 1
BIT 0 Data Bit 0

Name: XIO Address Register
Address: Base Address + 000A (Hex)
Address Space: VMEbus short I/O
Type: Write

Description: The host writes the XIO address to be executed to this register prior to accessing the XIO Data register. The addresses of the XIO commands are shown in Section 4.2.2. This register is WRITE ONLY. Note that once the XIO address is written into this register, it will remain until the host loads another XIO address, or a reset is generated. This allows the host to poll an XIO register by loading the XIO Address register once, then reading the XIO Data register until the desired results are obtained.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

4.2.2 XIO Registers

Relative addresses 0 through 1FE(Hex) bytes are written to the XIO Address register (000AH) of the VMIVME-6000 to specify XIO registers. These registers are programmed by the host to provide configuration and operational information for the VMIVME-6000. All data written/read to/from the XIO registers is done so through the XIO Data register (0008). Table 4.2.2-1 shows the three particular types of XIO and their relative address spaces that may be executed. Table 4.2.2-2 shows a map of all the XIO registers and the page where their description is located.

Table 4.2.2-1. XIO Register Group

Address (Hex)	Description
0000 - 007E	Hardware Registers
0080 - 00FE	Special Function Registers
0100 - 01FE	Internal ALU Registers

M6000/T4.2.2-1

To access an XIO register, the host must first load the XIO Address register with the address of the desired XIO. The host may then Read or Write data to the XIO Data register, depending on the type of access. Note that once the XIO address is loaded into the XIO Address register, it will not change until the register is loaded again, or a reset is generated. This allows the host to poll an XIO register by writing the XIO Address once, then reading the XIO Data register until the desired results are obtained. The XIO Hardware registers are programmed by the host to enable specific functions such as interrupts, or to read exception pointers provided by the board. Accesses to these registers require no on-board processor (firmware) interaction to complete the cycle. Therefore, data is read or written from/to the register in one VMEbus cycle.

When the host executes a Write Special Function XIO or writes to an XIO ALU register, the actual execution of the command is done by the on-board processor **after** the VMEbus cycle for the XIO Data register access is completed. The data (if required) is latched into an internal XIO register, and a flag is set to the internal firmware requesting service of the XIO. When the VMEbus cycle is completed, the on-board processor will interpret the Special Function or ALU register, and use the data accordingly. When the function is completed, the board will set bit 11 of the Active Status register. The host can read the Active Status Register (ASR) until bit 11 is detected, or program the board to provide a B Interrupt when the XIO is complete. After the bit is detected or the B Interrupt on XIO complete is asserted, the host must read the ASR again to clear bit 11 of the ASR.

NOTE

NO OTHER SPECIAL FUNCTION OR ALU REGISTER XIO COMMANDS SHOULD BE PERFORMED UNTIL BIT 11 OF THE ASR IS SET (DETECTED BY THE HOST) INDICATING THE PREVIOUS SPECIAL FUNCTION XIO IS COMPLETE, AND THE ASR IS READ A SECOND TIME TO CLEAR BIT 11.

Similarly, a Read Special Function or a read of an ALU register XIO involves the on-board firmware. When a READ Special Function/ALU register is performed, the board uses the address provided in the XIO Address register to identify the particular READ data. The board will complete the VMEbus read cycle, but the data in the XIO Data register will be invalid. After completion of the cycle, the on-board processor will move the requested data into the XIO Data register, and set bit 11 of the ASR. The host can read the ASR until bit 11 is detected, or program the board to provide a B Interrupt on XIO Complete. When bit 11 of the ASR is set or the B Interrupt is asserted, the host must read the ASR again to clear bit 11. The host may then execute the same Read Special Function XIO, and will receive the valid data. The same procedure, polling the ASR for bit 11 and then again reading the ASR to clear bit 11, must be followed on the second Special Function Read XIO. Special attention must be given to execution of XIO Commands while the VMIVME-6000 is "Actively" executing 1553 bus traffic. Section 4.2.4 describes the procedure for processing "Active XIO Commands".

Table 4.2.2-2. XIO Register Map

Hardware Register	Write Address	Read Address	Page
Control Register	0000		4-14
Status Word "Set" Mask	0002		4-15
Status Word "Clear" Mask	0004		4-15
Option Register	0006		4-16
Reserved	0008 thru 0012		
A Interrupt Pointer		0000	4-17
A Interrupt Map		0002	4-18
B Interrupt Pointer		0004	4-19
B Interrupt Map		0006	4-20
Current Control Block Pointer		0008	4-21
Current Control Block Map		000A	4-22
Last Posted ISR Pointer		000C	4-23
Last Posted ISR Map		000E	4-24
Monitor Ring Buffer Pointer		0010	4-25
Monitor Ring Buffer Map		0012	4-26
Last Status Word		0014	4-27
Last Command Word		0016	4-28
Active Status Register (ASR)		0018	4-29
A Interrupt Vector		001A	4-30
B Interrupt Vector		001C	4-31
Reserved	001E thru 007E	001E thru 007E	
Special Function Register	**Write Address**	**Read Address**	**Page**
Start Command	0080		4-33
Reserved	0082 thru 0084	0082 thru 0084	
Reset Board Command	0086		4-34
Clear Board Command	0088		4-35
Orderly Shutdown	008A		4-36
Time Tag Increments	008C		4-37
Time Tag MSW	008E	008E	4-38
Time Tag LSW	0090	0090	4-39
Time Tag Reset	0092		4-40
Time Tag Start	0094		4-41
Time Tag Halt	0096		4-42
Active Status Register (ASR)	0098		4-43
Reserved	009A thru 009E	009A thru 009E	
Manchester Error Type (MET)	00A0		4-44
Error Bit Time	00A2		4-45
Frame Length Register	00A4		4-46
Reserved	00A6 thru 00a8	00A6 thru 00A8	
MRT/MON RAM Address	00AA		4-47
MRT/MON RAM Data	00AC	00AC	4-48
Reserved	00AE thur 00FE	00AE thur 00FE	

4.2.2-2. XIO Register Map (Continued)

ALU Registers	Write Address	Read Address	Page
Control Block Address (W)	0100	0100	4-50
Control Block Map (W)	0102	0102	4-51
Current Buffer Pointer (R/W)	0104	0104	4-52
DMA Disable (W)	0106	0106	4-53
ISR (R)	0108	0108	4-54
TSR (R)	010A	010A	4-55
A Interrupt Mask (W)	010C	010C	4-56
B Interrupt Mask (W)	010E	010E	4-57
Auto Retry B int Mask (W)	0110	0110	4-58
Command Word Trigger (W)	0112	0112	4-59
Command Word Mask (W)	0114	0114	4-60
Reserved	0116 thru 0118	0116 thru 0118	
Auto Retry TSR Mask	011A	011A	4-61
Auto Retry ISR Mask	011C	011C	4-62
ISR Mask (W)	011E	011e	4-63
TSR Mask (W)	0120	0120	4-64
Error Mask (W)	0122	0122	4-65
BC Pointer Table Origin (W)	0124	0124	4-66
BC Pointer Table Length (W)	0126	0126	4-67
Lower Error Select Word (W)	0128	0128	4-68
Error Generation (Diagmode) (W)	012A	012A	4-70
Upper Error Select Word (W)	012C	012C	4-69
Built In Test Word (R)	012E	012E	4-71
DMA Timeout (W)	0130	0130	4-72
Reserved	0132	0132	
Response Time (W)	0134	0134	4-73
BC Intermessage Gap (W)	0136	0136	4-74
Ring Buffer Address (W)	0138	0138	4-75
Ring Buffer Map (W)	013A	013A	4-76
Status Word 1 Mask (W)	013C	013C	4-77
Status Word 2 Mask (W)	013E	013E	4-78
Reserved	0140 thru 0142	0140 thru 0142	
Word Count Error Plus (W)	0144	0144	4-79
Word Count Error Minus (W)	0146	0146	4-80
Major Frame Time LSW (W)	0148	0148	4-81
Major Frame Time MSW (W)	014A	014A	4-82
Minor Frame Time LSW (W)	014C	014C	4-83
Minor Frame Time MSW (W)	014E	014E	4-84
Programming Error (R)	0150	0150	4-85
Data Word Gap (W)	0152	0152	4-86
Dynamic BC RT Map (W)	0154	0154	4-87
Dynamic BC RT Address (W)	0156	0156	4-88
Dynamic BC Map (W)	0158	0158	4-89
Dynamic BC Address (W)	015A	015A	4-90
Dynamic DMA Disable (W)	015C	015C	4-91

4.2.2-2. XIO Register Map (Concluded)

ALU Registers	Write Address	Read Address	Page
Dynamic Status Word Mask (W)	015E	015E	4-92
Reserved	0160 thru 017E	0160 thru 017E	
Microcode Revision (R)	0180	0180	4-93
Reserved	0182 thru 0196	0182 thru 0196	
Lost B Interrupt Count (R)	0198	0198	4-94
Lost B Interrupt Pointer (R)	019A	019A	4-95
Reserved	019C thur 01FE	019C thur 01FE	

NOTE

THE REGISTERS ARE READ/WRITE, THE (W) AND (R) ARE INCLUDED WITH THE REGISTER NAME TO INDICATE THE USAGE OF THE REGISTER.

4.2.2.1 Hardware Registers

The first 80 (Hex) bytes of the XIO map are the Hardware registers located in the Host Interface ASIC. These registers are programmed by the host to enable specific functions such as interrupts, or to read exception pointers provided by the board. Accesses to these registers require no micro-code (firmware) interaction to complete the cycle, and therefore data is read or written from/to the register in one VMEbus cycle. The following pages will show the functions and addresses of the hardware registers.

Choose Hardware Registers in the following manner:

a. Write address of chosen hardware register into the XIO Address register located at offset 000A (Hex) in VMEbus short I/O space.

b. Register Write: Write desired data to the XIO Data register, located at offset 0008 (Hex) in VMEbus short I/O space.

   Register Read: Read data from the XIO Data register, located at offset 0008 (Hex) in VMEbus short I/O space.

XIO REGISTERS
HARDWARE

Name: **Control Register**
Address: **0000 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Control Register allows easy host access to hardware functions of the VMIVME-6000. The Control Register is write only.

BIT 15 Halt Immediately- Setting this bit to a logic "one" stops the VMIVME-6000 immediately regardless of its operation. The board will perform its "self-test" and return to OFF mode.
BIT 14 Enable A Interrupts
BIT 13 Enable B Interrupts
BIT 12 Generate B Interrupt on Active XIO complete

BIT 11 Clear A Interrupt Pointer- A Logic "one" set in any of bits 7-11 will "clear" the particular Pointer register.
BIT 10 Clear B Interrupt Pointer
BIT 9 Clear Last Data Buffer/Control Block Pointer
BIT 8 Clear Pointer to Last Posted ISR

BIT 7 Clear Ring Buffer Pointer
BIT 6 Not Used
BIT 5 Clear ASR- Setting this bit to a logic "1" will clear the Active Status register (ASR).
BIT 4 Enable Vectored Interrupts

BIT 3 Reserved, set to logic "zero"
BIT 2 Reserved, set to logic "zero"
BIT 1 Reserved, set to logic "zero"
BIT 0 Reserved, set to logic "zero"

XIO REGISTERS
HARDWARE

Name: **Status Word Set Mask/Clear Mask**
Address: **Set Mask: 0002 (Hex), Clear Mask: 0004 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The VMIVME-6000 Status Word Set Mask and its companion register the Clear Mask provide the host a global means to "set" and/or "clear" MIL-STD-1553 Status Word (SW) bits (excluding the Terminal Address) "on the fly" when the board is operating in MRT mode. **After** each MIL-STD-1553 status word transmission, the VMIVME-6000 will set and/or clear bits in the SW skeleton based on the Status Word Set and Status Word Clear registers. If these registers are left "zero", there will be no "real-time" changing of the Status Word. These two registers work with the individual RT Status Word Set and Clear Mask registers located in the MRT RAM space (Section 4.4), to provide the actual set/clear function.

A logic "one" set in a particular bit of the status word "set" mask will cause the corresponding bit to be set in the SW skeleton. Likewise, a logic "one" set in the status word "clear" mask will cause the corresponding bit to be cleared from the status word skeleton. If both bits are set, the "clear" will have priority.

* The status word skeletion bits are the actual bits the firmware will use to transmit on the MIL-STD-1553 bus.

BIT 15	**Reserved, set to logic "zero"**	**BIT 7**	**Status Word Bit 7**
BIT 14	**Reserved, set to logic "zero"**	**BIT 6**	**Status Word Bit 6**
BIT 13	**Reserved, set to logic "zero"**	**BIT 5**	**Status Word Bit 5**
BIT 12	**Reserved, set to logic "zero"**	**BIT 4**	**Status Word Bit 4**
BIT 11	**Reserved, set to logic "zero"**	**BIT 3**	**Status Word Bit 3**
BIT 10	**Status Word Bit 10**	**BIT 2**	**Status Word Bit 2**
BIT 9	**Status Word Bit 9**	**BIT 1**	**Status Word Bit 1**
BIT 8	**Status Word Bit 8**	**BIT 0**	**Status Word Bit 0**

NOTE:

The Status Word Skeleton is updated after each MIL-STD-1553 transmission. When the user sets or clears a bit, there will be a message transmission lag until the skeleton is updated.

XIO REGISTERS
HARDWARE

Name: **Option Register**
Address: **0006 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: This register contains additional host selected options.

BIT 15 Reserved, set to logic "zero"
BIT 14 Enable BC Pointer Table - Bus Controller will get Links from a table (as opposed to the Control Block). The Bus Control Table Pointer and Bus Control Table Length ALU register should be programmed to use this option.
BIT 13 A Interrupt on B Interrupt Not Serviced
BIT 12 Post Zero ISR* - A logic "one" in this bit will cause the board to post all ISRs* including those with no bits set.
BIT 11 Transmit On Already Active 1553 Bus - If this bit is set, the VMIVME-6000 will not check the 1553 bus to ensure "no activity" before it transmits.
BIT 10 Post Zero TSR -** A logic "one" in this bit will cause the board to post all TSRs including those with no bits set.
BIT 9 Set Terminal Flag on Loop Error - Set terminal flag in MIL-STD-1553 Status Word if loop-around error occurs. (MRT mode)
BIT 8 Initialize All 32 RTs Using One Set of RT Control/Subaddress Blocks -
If set, during MRT initialization, board will initialize all RT parameters except the terminal address using the information from one host- supplied set of Header Block, RT Control Block, and Subaddress Blocks. Useful for quick set-up of board to monitor or simulate all bus traffic.
BIT 7 Continue on DMA Error
BIT 6 Inhibit Transmitter Timeout - Disable transmitter timeout circuitry (all modes).
BIT 5 Instrumentation BIT - The board uses the instrumentation bit to validate command and status responses.
BIT 4 B Interrupt after MRT/MON Initialization Complete
BIT 3 Subsystem Flag Set on DMA Error - (MRT mode only)
BIT 2 Reserved, set to logic "zero"
BIT 1 Reserved, set to logic "zero"
BIT 0 Reserved, set to logic "zero"

***ISR:** Interrupt Status Register
****TSR**: Transmission Status Register

XIO Registers
Hardware

Name: "A" Interrupt Pointer
Address: 0000 (Hex)
Address Space: XIO
Type: Read

Description: The VMIVME-6000 provides a 16-bit pointer of the on-board memory that contains the address of the last data buffer (MRT/MON mode) or Control Block (Simulator BC) that caused an A level interrupt.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: "A" Interrupt Map
Address: 0002 (Hex)
Address Space: XIO
Type: Read

Description: The VMIVME-6000 provides a 4-bit map of the on-board memory that contains the address of the last data buffer (MRT/MON mode) or Control Block (Simulator BC) that caused an A level interrupt.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Address Bit 19
BIT 2 Address Bit 18
BIT 1 Address Bit 17
BIT 0 Address Bit 16

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: **"B" Interrupt Pointer**
Address: **0004 (Hex)**
Address Space: **XIO**
Type: **Read**

Description: The VMIVME-6000 provides a 16-bit pointer of the on-board memory that contains the address of the last data buffer (MRT/MON mode) or Control Block (Simulator, BC) that caused a B level interrupt.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: **"B" Interrupt map**
Address: **0006 (Hex)**
Address Space: **XIO**
Type: **Read**

Description: The VMIVME-6000 provides a 4-bit map of the on-board memory that contains the address of the last data buffer (MRT/MON mode) or Control Block (Simulator, BC) that caused a B level interrupt.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Address Bit 19
BIT 2 Address Bit 18
BIT 1 Address Bit 17
BIT 0 Address Bit 16

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: **Current Control Block Pointer**
Address: **0008 (Hex)**
Address Space: **XIO**
Type: **Read**

Description: In **Bus Controller Mode (Simulator mode)**, the VMIVME-6000 provides a 16-bit pointer that contains the on-board memory address of the current control block being executed. In **MRT Mode**, it is the last data buffer to be updated.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: **Current Control Block Map**
Address: **000A (Hex)**
Address Space: **XIO**
Type: **Read**

Description: In **Bus Control Mode (Simulator mode)**, the VMIVME-6000 provides a 4-bit map that contains the on-board memory address of the current control block being executed. In **MRT Mode**, it is the last data buffer to be updated.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Address Bit 19
BIT 2 Address Bit 18
BIT 1 Address Bit 17
BIT 0 Address Bit 16

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: **Last Posted ISR* Pointer**
Address: **000C (Hex)**
Address Space **XIO**
Type: **Read**

Description: This register contains a 16-bit pointer to the on-board memory address of the last posted nonzero Interrupt Status Register as determined by the ISR mask **(all modes)**.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

***ISR**: INTERRUPT STATUS REGISTER

XIO Registers
Hardware

Name: **Last Posted ISR* Map**
Address: **000E (Hex)**
Address Space: **XIO**
Type: **Read**

Description: This register contains a 4-bit map to the on-board memory address of the last posted non zero ISR as determined by the ISR mask **(all modes)**.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Address Bit 19
BIT 2 Address Bit 18
BIT 1 Address Bit 17
BIT 0 Address Bit 16

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

***ISR**: INTERRUPT STATUS REGISTER

XIO Registers
Hardware

Name: **Monitor Ring Buffer Pointer**
Address: **0010 (Hex)**
Address Space: **XIO**
Type: **Read**

Description: If the board is operating in **Monitor Mode**, this register will contain the lower 16-bit on-board memory address of the last entry in the monitor ring buffer.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: **Monitor Ring Buffer Map**
Address: **0012 (Hex)**
Address Space: **XIO**
Type: **Read**

Description: If the board is operating in **Monitor Mode**, this register will contain the upper 4-bit on-board memory address of the last entry in the monitor ring buffer.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Address Bit 19
BIT 2 Address Bit 18
BIT 1 Address Bit 17
BIT 0 Address Bit 16

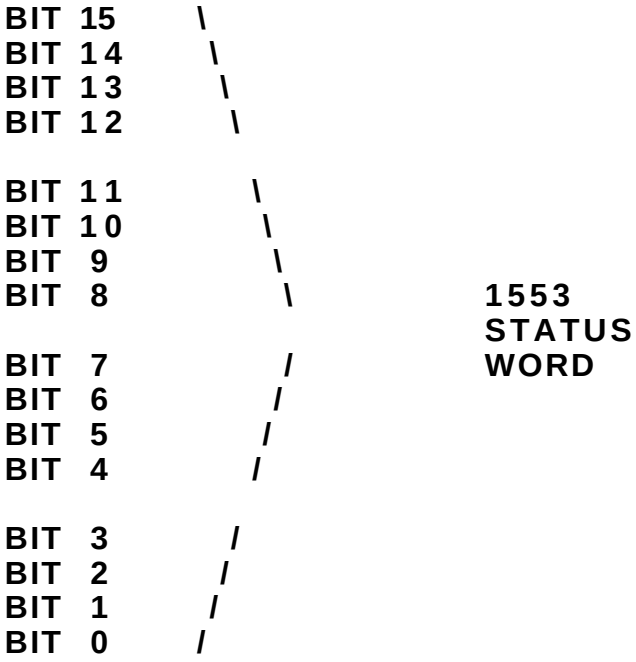
NOTE

EACH OF THE POINTER AND MAP COMBINATIONS DISCUSSED ABOVE MAKE UP A 20-bit ADDRESS. THE UPPER 4-bits OF THE 24-bit ADDRESS (IF USED) MUST BE KEPT AS AN OFFSET BY THE HOST AND ADDED TO THE POINTER/MAP ADDRESS.

XIO Registers
Hardware

Name: Last Status Word
Address: 0014 (Hex)
Address Space: XIO
Type: Read

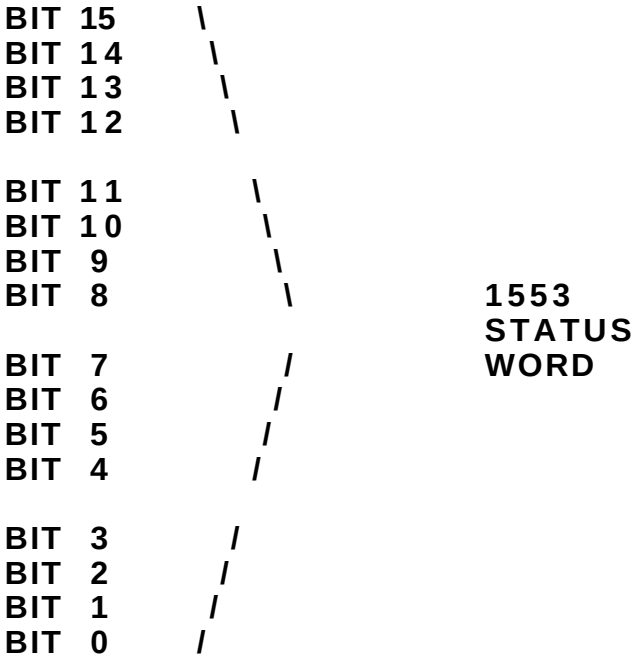
Description: This register will contain the Last Status Word updated by the board as a remote terminal.



XIO Registers
Hardware

Name: Last Command Word
Address: 0016 (Hex)
Address Space: XIO
Type: Read

Description: This register will contain the Last Command Word received by the board as a remote terminal.



XIO Registers
Hardware

Name: **Active Status Register (ASR)**
Address: **0018 (Hex)**
Address Space: **XIO**
Type: **Read (Write performed at Special Function XIO 0098)**

Description: The ASR provides the VMIVME-6000's current status. This register is Read/Write and may be read from this address and written to as a Special Function XIO 0098 (Hex) (see Special Function XIO, Section 4.2.2.2). The ASR is cleared upon Power-Up Reset and may be cleared by the host via a CLEAR Command (0088 Hex) or by setting bit 5 of the Control register (000 Hex). See Control Register, Hardware registers this section and Clear Command, Special Function registers Section 4.2.2.2.

BIT 15 **Board Active -** The board is busy executing control blocks, self test, or lengthy XIO commands such as a "clear".
BIT 14 **A Interrupt Requested -** A match of the A Interrupt Mask and a ISR has occurred for a previous message.
BIT 13 **B Interrupt Requested -** A match of the B Interrupt Mask and a ISR hasoccurred for a previous message.
BIT 12 **B Interrupt Requested on Active XIO Complete -** The board has generated a B interrupt to signal completion of a XIO.
BIT 11 **Active XIO Finished -** The VMIVME-6000 has completed servicing an XIO command.
BIT 10 **ALU Self-Test Failed -** The VMIVME-6000 has determined that there is a problem with the internal ALU, Sequencer, or RAM.
BIT 9 **Host Self-Test Failed -** The VMIVME-6000 has failed BIT in communication with the host interface ASIC.
BIT 8 **XMIT/RCV Self-Test Failed -** "Loopback " of transmitted data did not match, or there was a transmission error.
BIT 7 **Orderly Shutdown -** A logic "one" in this bit signals that the host has requested the board to "shutdown" and return to OFF mode.
BITS 6, 5, 4 Current Mode
0 - OFF
1 - Bus Controller/Simulator
2 - Diagmode
4 - MRT/MON
BIT 3 **B Interrupt Not Serviced -** The current B Interrupt was asserted before the previous B Interrupt was serviced.
BIT 2 **Self-Test Complete**
BIT 1 **Bit Failed -** An internal VMIVME-6000 BIT failed.
BIT 0 **Error -** The VMIVME-6000 has detected what it considers an error. (Maskable via the Error Mask except during Power-up)

XIO Registers
Hardware

Name: **"A" Interrupt Vector Register**
Address: **001A (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The VMIVME-6000 provides vector interrupt capability during VMEbus interrupt acknowledge cycles. The host selected vectors for the A level interrupts should be written to this location during initialization of the board. A detailed discussion of interrupts is included in Section 4.5.

BIT 15 Vector Bit 15
BIT 14 Vector Bit 14
BIT 13 Vector Bit 13
BIT 12 Vector Bit 12

BIT 11 Vector Bit 11
BIT 10 Vector Bit 10
BIT 9 Vector Bit 9
BIT 8 Vector Bit 8

BIT 7 Vector Bit 7
BIT 6 Vector Bit 6
BIT 5 Vector Bit 5
BIT 4 Vector Bit 4

BIT 3 Vector Bit 3
BIT 2 Vector Bit 2
BIT 1 Vector Bit 1
BIT 0 Vector Bit 0

XIO Registers
Hardware

Name: **"B" Interrupt Vector Register**
Address: **001C (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The VMIVME-6000 provides vector interrupt capability during VMEbus interrupt acknowledge cycles. The host selected vectors for the B level interrupts should be written to these locations during initialization of the board. A detailed discussion of interrupts is included in Section 4.5.

BIT 15 Vector Bit 15
BIT 14 Vector Bit 14
BIT 13 Vector Bit 13
BIT 12 Vector Bit 12

BIT 11 Vector Bit 11
BIT 10 Vector Bit 10
BIT 9 Vector Bit 9
BIT 8 Vector Bit 8

BIT 7 Vector Bit 7
BIT 6 Vector Bit 6
BIT 5 Vector Bit 5
BIT 4 Vector Bit 4

BIT 3 Vector Bit 3
BIT 2 Vector Bit 2
BIT 1 Vector Bit 1
BIT 0 Vector Bit 0

4.2.2.2 Special Function Registers

The next 80 (Hex) bytes of the VMIVME-6000 make up the Special Function Registers. These registers are accessed by the host to instruct the board to perform a special function such as a START, SHUTDOWN, or CLEAR. Accesses to these registers require interaction with the on-board firmware. For this reason, the Special Functions must be executed in a specific manner.

When the host executes a Write Special Function, the actual execution of the command is done by the microcode AFTER the VMEbus cycle is completed for the write to the XIO Data Register. The data (if required) is latched into an internal XIO Register, and a flag is set to the internal firmware requesting service of the XIO. When the VMEbus cycle is completed, the on-board processor will interpret the Special Function and use the data accordingly. When the function is completed, the board will set bit 11 of the ASR. The host can poll the ASR until bit 11 is detected. After the bit is detected, the host must read the ASR again to clear bit 11. No other XIO commands should be performed until bit 11 of the ASR is set (detected by the host) indicating the previous Special Function XIO is complete, and the ASR is read a second time to clear bit 11.

Similarly, a Read Special Function XIO involves the on-board firmware. When a Read Special Function is performed, the board uses the address provided in the XIO Address register to identify the particular Read data. The board will complete the VMEbus read cycle, but the data will be invalid. After completion of the cycle. The on-board processor will move the requested data into the XIO register, and set bit 11 of the ASR. The host must read the ASR until bit 11 is detected. When bit 11 of the ASR is set, the host must read the ASR again to clear bit 11. The host may then execute the same READ Special Function XIO, and will receive the valid data. The same procedure, polling the ASR for bit 11 and then again reading the ASR to clear bit 11, must be followed on the second Special Function READ XIO. Special Function XIO register addresses and descriptions are shown in the following pages.

XIO REGISTERS
SPECIAL FUNCTION

Name: **Start Command**
Address: **0080 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The START Command places the board in "active mode", executing Control Blocks. The desired mode should be included as data when the XIO START Command is written to the board. The valid choices for the Start Command are 1- Simulator 2- Diagmode, 3- MRT/MON with initialization, 4- MRT/MON without initiatization. Both MRT/MON modes will display a "4" in the Active Status Register (ASR). For more information on operational modes, see Section 4.3.

BIT 15 Reserved, set to zero
BIT 14 Reserved, set to zero
BIT 13 Reserved, set to zero
BIT 12 Reserved, set to zero

BIT 11 Reserved, set to zero
BIT 10 Reserved, set to zero
BIT 9 Reserved, set to zero
BIT 8 Reserved, set to zero

BIT 7 Reserved, set to zero
BIT 6 Reserved, set to zero
BIT 5 Reserved, set to zero
BIT 4 Reserved, set to zero

BIT 3 Reserved, set to zero

BIT 2 Bits 2,1,0 Desired Mode
BIT 1 1 - Simulator/Bus Controller
BIT 0 2 - Diagmode
4 - MRT/MON: w/initialization
3 - MRT/MON: w/o initialization (quick start)

Example (for less confusion)

	Bits 2, 1, 0	desired mode
Bit 2	001 (1)	Simulator/B
Bit 1	010 (2)	Diagmode
Bit 0	011 (3)	MRT/MON : W/INIT
	100 (4)	MRT/MON : W/O INIT

XIO REGISTERS
SPECIAL FUNCTION

Name: **Reset board Command**
Address: **0086 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Reset board Command clears all VMIVME-6000 ASIC logic. A reset command may be executed after completion of the VMIVME-6000 self-test at power-up.

BIT 15 Don't Care
BIT 14 Don't Care
BIT 13 Don't Care
BIT 12 Don't Care

BIT 11 Don't Care
BIT 10 Don't Care
BIT 9 Don't Care
BIT 8 Don't Care

BIT 7 Don't Care
BIT 6 Don't Care
BIT 5 Don't Care
BIT 4 Don't Care

BIT 3 Don't Care
BIT 2 Don't Care
BIT 1 Don't Care
BIT 0 Don't Care

XIO REGISTERS
SPECIAL FUNCTION

Name: **Clear Command**
Address: **0088 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Clear Command clears all VMIVME-6000 flags, both A and B bus, and all internal micro-engine registers. It does NOT clear the Time Tag (see Time Tag Reset). A Clear Command should be executed after completion of the VMIVME-6000 self-test at power-up, and before switching modes (i.e., BC Mode-to-MRT Mode).

BIT 15 Don't Care
BIT 14 Don't Care
BIT 13 Don't Care
BIT 12 Don't Care

BIT 11 Don't Care
BIT 10 Don't Care
BIT 9 Don't Care
BIT 8 Don't Care

BIT 7 Don't Care
BIT 6 Don't Care
BIT 5 Don't Care
BIT 4 Don't Care

BIT 3 Don't Care
BIT 2 Don't Care
BIT 1 Don't Care
BIT 0 Don't Care

XIO REGISTERS
SPECIAL FUNCTION

Name: **Orderly ShutdownCommand**
Address: **008A (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Orderly Shutdown Command will stop the board after the current message or control block is completed. Execution of this command will set a corresponding bit (bit 7) in the Active Status Register ASR.

BIT 15 Don't Care
BIT 14 Don't Care
BIT 13 Don't Care
BIT 12 Don't Care

BIT 11 Don't Care
BIT 10 Don't Care
BIT 9 Don't Care
BIT 8 Don't Care

BIT 7 Don't Care
BIT 6 Don't Care
BIT 5 Don't Care
BIT 4 Don't Care

BIT 3 Don't Care
BIT 2 Don't Care
BIT 1 Don't Care
BIT 0 Don't Care

XIO REGISTERS
SPECIAL FUNCTION

Name: **Time Tag Increments**
Address: **008C (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Time Tag Increments register controls the resolution of the Time tag and gap counters. The default time tag value is 64 μsec. If bit 5 of this register is "zero", the increment will be 64 μsec. If bit 5 is a "one", the time tag increments will be 1 μsec.

BIT 15 Don't Care, set to "zero"
BIT 14 Don't Care, set to "zero"
BIT 13 Don't Care, set to "zero"
BIT 12 Don't Care, set to "zero"

BIT 11 Don't Care, set to "zero"
BIT 10 Don't Care, set to "zero"
BIT 9 Don't Care, set to "zero"
BIT 8 Don't Care, set to "zero"

BIT 7 Don't Care, set to "zero"
BIT 6 Don't Care, set to "zero"
BIT 5 Increment bit - logic "zero" = 64 μs - logic "one" =1 μs
BIT 4 Don't Care, set to "zero"

BIT 3 Don't Care, set to "zero"
BIT 2 Don't Care, set to "zero"
BIT 1 Don't Care, set to "zero"
BIT 0 Don't Care, set to "zero"

XIO REGISTERS
SPECIAL FUNCTION

Name: **Time Tag Most Significant Word**
Address: **008E (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Time Tag Counter is a 32-bit value, read or written as two 16-bit segments (Most Significant Word "MSW" and Least Significant Word "LSW"). The resolution of the Time Tag is controlled by The Time Tag Increment.

BIT 15 Time Tag Bit 31
BIT 14 Time Tag Bit 30
BIT 13 Time Tag Bit 29
BIT 12 Time Tag Bit 28

BIT 11 Time Tag Bit 27
BIT 10 Time Tag Bit 26
BIT 9 Time Tag Bit 25
BIT 8 Time Tag Bit 24

BIT 7 Time Tag Bit 23
BIT 6 Time Tag Bit 22
BIT 5 Time Tag Bit 21
BIT 4 Time Tag Bit 20

BIT 3 Time Tag Bit 19
BIT 2 Time Tag Bit 18
BIT 1 Time Tag Bit 17
BIT 0 Time Tag Bit 16

XIO REGISTERS
SPECIAL FUNCTION

Name: **Time Tag Least Significant Word**
Address: **0090 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Time Tag Counter is a 32-bit value, read or written as two 16-bit segments (Most Significant Word "MSW" and Least Significant Word "LSW"). The resolution of the Time Tag is controlled by the Time Tag Increment.

BIT 15 Time Tag Bit 15
BIT 14 Time Tag Bit 14
BIT 13 Time Tag Bit 13
BIT 12 Time Tag Bit 12

BIT 11 Time Tag Bit 11
BIT 10 Time Tag Bit 10
BIT 9 Time Tag Bit 9
BIT 8 Time Tag Bit 8

BIT 7 Time Tag Bit 7
BIT 6 Time Tag Bit 6
BIT 5 Time Tag Bit 5
BIT 4 Time Tag Bit 4

BIT 3 Time Tag Bit 3
BIT 2 Time Tag Bit 2
BIT 1 Time Tag Bit 1
BIT 0 Time Tag Bit 0

XIO REGISTERS
SPECIAL FUNCTION

Name: **Time Tag Reset**
Address: **0092 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: A write XIO Command to this register causes the Time Tag to be reset to "zero". It does **not** stop the counter.

BIT 15 Don`t Care, set to logic "zero"
BIT 14 Don`t Care, set to logic "zero"
BIT 13 Don`t Care, set to logic "zero"
BIT 12 Don`t Care, set to logic "zero"

BIT 11 Don`t Care, set to logic "zero"
BIT 10 Don`t Care, set to logic "zero"
BIT 9 Don`t Care, set to logic "zero"
BIT 8 Don`t Care, set to logic "zero"

BIT 7 Don`t Care, set to logic "zero"
BIT 6 Don`t Care, set to logic "zero"
BIT 5 Don`t Care, set to logic "zero"
BIT 4 Don`t Care, set to logic "zero"

BIT 3 Don`t Care, set to logic "zero"
BIT 2 Don`t Care, set to logic "zero"
BIT 1 Don`t Care, set to logic "zero"
BIT 0 Don`t Care, set to logic "zero"

XIO REGISTERS
SPECIAL FUNCTION

Name: **TimeTag Start**
Address: **0094 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Time Tag counter normally starts upon the reception of the first valid command word. The host may start the counters earlier by issuing a write XIO command to this register.

BIT 15 Don`t Care, set to logic "zero"
BIT 14 Don`t Care, set to logic "zero"
BIT 13 Don`t Care, set to logic "zero"
BIT 12 Don`t Care, set to logic "zero"

BIT 11 Don`t Care, set to logic "zero"
BIT 10 Don`t Care, set to logic "zero"
BIT 9 Don`t Care, set to logic "zero"
BIT 8 Don`t Care, set to logic "zero"

BIT 7 Don`t Care, set to logic "zero"
BIT 6 Don`t Care, set to logic "zero"
BIT 5 Don`t Care, set to logic "zero"
BIT 4 Don`t Care, set to logic "zero"

BIT 3 Don`t Care, set to logic "zero"
BIT 2 Don`t Care, set to logic "zero"
BIT 1 Don`t Care, set to logic "zero"
BIT 0 Don`t Care, set to logic "zero"

XIO REGISTERS
SPECIAL FUNCTION

Name: **Time Tag Halt**
Address: **0096 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: This command stops the Time Tag counter. It does **not** reset the counter. Once the counter is halted, it will not start until a Time Tag Start XIO command is issued, or a valid message is received.

BIT 15 Don`t Care, set to logic "zero"
BIT 14 Don`t Care, set to logic "zero"
BIT 13 Don`t Care, set to logic "zero"
BIT 12 Don`t Care, set to logic "zero"

BIT 11 Don`t Care, set to logic "zero"
BIT 10 Don`t Care, set to logic "zero"
BIT 9 Don`t Care, set to logic "zero"
BIT 8 Don`t Care, set to logic "zero"

BIT 7 Don`t Care, set to logic "zero"
BIT 6 Don`t Care, set to logic "zero"
BIT 5 Don`t Care, set to logic "zero"
BIT 4 Don`t Care, set to logic "zero"

BIT 3 Don`t Care, set to logic "zero"
BIT 2 Don`t Care, set to logic "zero"
BIT 1 Don`t Care, set to logic "zero"
BIT 0 Don`t Care, set to logic "zero"

XIO REGISTERS
SPECIAL FUNCTION

Name: **Active Status Register (ASR)**
Address: **0098 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The ASR provides the VMIVME-6000's current status. This register is Read/Write and may be written to from this address and read as a Hardware register XIO 0018 (Hex). The ASR is cleared upon Power-up Reset and may be cleared by the Host via a Clear Command (0088 Hex) or by setting bit 5 of the Control Register (0000 Hex).

BIT 15 board Active - The board is busy executing control blocks, self test, or lengthy XIO commands such as a "clear".
BIT 14 A Interrupt Requested - A match of the A Interrupt Mask and a ISR has occurred for a previous message.
BIT 13 B Interrupt Requested - A match of the B Interrupt Mask and a ISR has occurred for a previous message.
BIT 12 B Interrupt Requested on Active XIO Complete - The board has generated a B interrupt to signal completion of an XIO.
BIT 11 Active XIO Finished - The VMIVME-6000 has completed servicing an XIO command.
BIT 10 ALU Self-Test Failed - The VMIVME-6000 has determined that there is a problem with the internal ALU, Sequencer, or RAM.
BIT 9 Host Self-Test Failed - The VMIVME-6000 has failed BIT in communication with the Host Interface ASIC.
BIT 8 XMIT/RCV Self-Test Failed - "Loopback" of transmitted data did not match, or there was a transmission error.
BIT 7 Orderly Shutdown - A logic "one" in this bit signals that the host has requested the board to "shut down" and return to OFF mode.
BITS 6, 5, 4 Current Mode
0 - OFF
1 - Bus Controller/Simulator
2 - Diagmode
4 - MRT/MON
BIT 3 B Interrupt Not Serviced - The current B interrupt was asserted before the previous B interrupt was serviced.
BIT 2 Self-Test Complete
BIT 1 Bit Failed - An internal VMIVME-6000 BIT failed.
BIT 0 Error - The VMIVME-6000 has detected what it considers an error. (Maskable via the Error Mask except during Power-up).

XIO REGISTERS
SPECIAL FUNCTION

Name: **Manchester Error Type (MET)**
Address: **00A0 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The Manchester Error Type register is programmed by the host to define the type of Manchester Error to be generated. A detailed discussion of error generation is included in Section 4.6.

BIT 15 **HI BI-0 Error -** Biphase will be high for entire bit time.

BIT 14 **Low BI-0 Error -** Biphase will be low for entire bit time.

BIT 13 **Sync Error -** board will generate a 500 nsec sync error.

BIT 12 **Last Half Sync Error -** Error will be in last 500 nsec of bit time.

BIT 11 **+Transition Error -** Causes transition delay after ideal crossing.

BIT 10 **-Transition Error -** Causes transition before ideal crossing.

BITS 9 - 4 Reserved, set to logic "zero"

BITS 3 - 0 **Transition Error Delay -** If bits 10 and 11 are set, it causes a 21 nsec delay per increment.

XIO REGISTERS
SPECIAL FUNCTION

Name: **Error Bit Time**
Address: **00A2 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: The bit time of a Manchester Error to be generated is selected in this register. Valid bit times are 0-19 (dec). Values out of this range will cause improper board operation. The default bit time is bit 8.

BIT 15 Don`t Care, set to logic "zero"
BIT 14 Don`t Care, set to logic "zero"
BIT 13 Don`t Care, set to logic "zero"
BIT 12 Don`t Care, set to logic "zero"

BIT 11 Don`t Care, set to logic "zero"
BIT 10 Don`t Care, set to logic "zero"
BIT 9 Don`t Care, set to logic "zero"
BIT 8 Don`t Care, set to logic "zero"

BIT 7 Don`t Care, set to logic "zero"
BIT 6 Don`t Care, set to logic "zero"
BIT 5 Don`t Care, set to logic "zero"
BIT 4 MET Bit 4 Bit time = 19 (dec)

BIT 3 MET Bit 3
BIT 2 MET Bit 2
BIT 1 MET Bit 1
BIT 0 MET Bit 0 Bit time = 0 (dec)

XIO REGISTERS
SPECIAL FUNCTION

Name: **Frame Length Register**
Address: **00A4 (Hex)**
Address Space: **XIO**
Type: **Write**

Description: Frame Length refers to the length of the 1553 word in "bit times". The standard valid 1553 word has 20-bit times. The VMIVME-6000 can generate bit count errors by adjusting the frame length or bit times of the word. The range of bit times is from 17 to 32 (dec). Values outside of this range will cause improper board operation. A 17 (dec) in this register would cause a word to be transmitted that had a -3 bit count, while a 27 (dec) would cause a word of +7 bits. Note: This register has no effect on transmitted data unless the bit count error is selected in the error generation select of the particular control block.

BIT 15 Reserved, set to "zero"
BIT 14 Reserved, set to "zero"
BIT 13 Reserved, set to "zero"
BIT 12 Reserved, set to "zero"
BIT 11 Reserved, set to "zero"
BIT 10 Reserved, set to "zero"
BIT 9 Reserved, set to "zero"
BIT 8 Reserved, set to "zero"

BIT 7 Reserved, set to "zero"
BIT 6 Reserved, set to "zero"
BIT 5 FLR Bit 5
BIT 4 FLR Bit 4 Frame length count: 32 (dec) = + 12 bits

BIT 3 FLR Bit 3
BIT 2 FLR Bit 2 Frame length count: 20 (dec) = normal count
BIT 1 FLR Bit 1
BIT 0 FLR Bit 0 Frame length count: 17 (dec) = - 3 bits

Example:

Frame Length Count
100000 (32 DEC) = + 12-bits
010100 (20 DEC) = normal count
010001 (17 DEC) = 3-bits

XIO REGISTERS
SPECIAL FUNCTION

Name: **MRT/MON RAM Address**
Address: **00AA (Hex)**
Address Space: **XIO**
Type: **Write**

Description: An on-board 8 k X 16-bit memory, separate from the 128 k X 16-bit memory, is used by the on-board firmware to hold information used in MRT/MON Mode. The information is stored in the RAM to reduce the DMA overhead while operating in MRT/MON Mode. During operation, it may be necessary for the host to access the external MRT RAM. This is done using the MRT/MON RAM Address and Data registers. Note that, when addressing the MRT/MON RAM, the firmware requires the addresses to be WORD addresses, i.e., the first 16-bit word is address 0, the second 16-bit word is address 1. The last address of the MRT/MON RAM would be 1FFF (Hex). Details of the MRT/MON RAM are included in Section 4.4. Before performing a READ or WRITE from/to the MRT/MON RAM, the host should read the ASR to clear bit 11 in case it was set on a previous XIO.

To READ an MRT/MON RAM location, the host must write the WORD address to the MRT/MON RAM Address register. The on-board firmware will store the address to be used for the read in an internal register. The board will set bit 11 of the ASR when the address has been stored. The host must then read the MRT/MON RAM Data register. The data read on this cycle will not be valid, but the access will cause the firmware to move the data from the MRT/MON RAM to the XIO register and set bit 11 of the ASR. When bit 11 of the ASR is set, the host may again read the MRT/MON Data register to read the valid data.

To write to a location in MRT/MON RAM, the host must first load an address into the MRT/MON Address register. When the operation is completed (bit 11 of the ASR set), the host should write the data to the MRT/MON RAM Data register. The data will be written to the MRT/MON RAM by the operational firmware, and bit 11 of the ASR will again be set when the operation is complete.

BIT 15	**Data bit 15**	**BIT 7**	**Data bit 7**
BIT 14	**Data bit 14**	**BIT 6**	**Data bit 6**
BIT 13	**Data bit 13**	**BIT 5**	**Data bit 5**
BIT 12	**Data bit 12**	**BIT 4**	**Data bit 4**
BIT 11	**Data bit 11**	**BIT 3**	**Data bit 3**
BIT 10	**Data bit 10**	**BIT 2**	**Data bit 2**
BIT 9	**Data bit 9**	**BIT 1**	**Data bit 1**
BIT 8	**Data bit 8**	**BIT 0**	**Data bit 0**

XIO REGISTERS
SPECIAL FUNCTION

Name: **MRT/MON RAM Data**
Address: **00AC (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: An on-board 8 k X 16-bit memory , separate from the 128 k X 16-bit memory, is used by the on-board firmware to hold information used in MRT/MON mode. The information is stored in the RAM to reduce the DMA overhead while operating in MRT/MON mode. During operation , it may be necessary for the host to access the external MRT RAM. This is done using the MRT/MON RAM Address and Data Registers. Note that, when addressing the MRT/MON RAM ,the firmware requires the addresses to be WORD addresses, i.e., the first 16-bit word is address 0, the second 16-bit word is address 1. The last address of the MRT/MON RAM would be 1FFF(Hex). Details of the MRT/MON RAM are included in Section 4.4. Before performing a READ an WRITE from/to the MRT/MON RAM, the host should read the ASR to clear bit 11 in case it was set on a previous XIO.

To READ an MRT/MON RAM location, the host must write the WORD address to the MRT/MON RAM Address register. The on-board firmware will store the address to be used for the read in an internal register. The board will set bit 11 of the ASR when the address has been stored. The host must then read the MRT/MON RAM Data register. The read on this cycle will not be valid, but the access will cause the firmware to move the data from the MRT/MON RAM to the XIO register and set bit 11 of the ASR. When bit 11 of the ASR is set, the host may again read the MRT/MON Data register to read the valid data.

To write to a location in MRT/MON RAM, the host must load an address into the MRT/MON Address register. When the operation is completed (bit 11 of the ASR set), the host should write the data to the MRT/MON RAM Data register. The data will be written to the MRT/MON RAM by the operational firmware, and bit 11 of the ASR will again be set when the operation is complete.

BIT 15	**Address bit 15**	**BIT 7**	**Address bit 7**
BIT 14	**Address bit 14**	**BIT 6**	**Address bit 6**
BIT 13	**Address bit 13**	**BIT 5**	**Address bit 5**
BIT 12	**Address bit 12**	**BIT 4**	**Address bit 4**
BIT 11	**Address bit 11**	**BIT 3**	**Address bit 3**
BIT 10	**Address bit 10**	**BIT 2**	**Address bit 2**
BIT 9	**Address bit 9**	**BIT 1**	**Address bit 1**
BIT 8	**Address bit 8**	**BIT 0**	**Address bit 0**

4.2.3 Internal ALU Registers

The remaining 100 (Hex) bytes of the VMIVME-6000 XIO space are the Internal ALU registers. These registers specify operational parameters for the 1553 functions to be performed. Table 4.2.2-2, the XIO Register Map, lists the ALU registers and their addresses. Accesses to these registers involve internal firmware of the board, and are executed similar to the Special Function XIO.

When the host writes to an ALU register, the address of the register and the data are latched into XIO Registers, and the VMEbus cycle is completed. When the cycle is finished, the on-board processor will move the data from the XIO register to the ALU register specified by the latched address. When the XIO is complete, the board will set bit 11 of the Active Status Register (ASR). The host can read the ASR until bit 11 is detected, or program the board to cause a B Interrupt when the XIO is complete. After the bit or interrupt is detected, the host should again read the ASR to clear bit 11. No other XIO commands should be executed until bit 11 of the ASR is set (detected by the host), signifying that the previous ALU XIO is complete, and is cleared by the second read of the ASR.

Reading an ALU register also involves the on-board firmware. During the VMEbus READ cycle, the ALU address is latched into an XIO register, and the VMEbus read cycle is completed (data read will be invalid). After the cycle is completed, the on-board processor will move the data from the ALU register specified by the latched address into an XIO register and set bit 11 of the ASR. The host should poll the ASR, or use the B Interrupt on XIO complete to determine when the read data is valid. After bit 11 of the ASR or the interrupt is detected by the host, the host must again read the ASR to clear bit 11. The host may then execute the same read of the ALU register, and the data will be valid. The procedure, polling the ASR for bit 11 to be set, and then again reading the ASR to clear bit 11 must also be followed on the second ALU register read.

XIO Registers
Internal ALU Registers

Name: **Control Block Address Register**
Address: **0100 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Control Block Address Register should be initialized with the least significant 16-bits of the address of the first Control Block to be executed. In all modes, this and the Control Block Map register are the only internal registers that **must** be programmed by the host for the board to operate.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO Registers
Internal ALU Registers

Name: **Control Block Map Register**
Address: **0102 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Control Block Map Register should be programmed with the most significant 4-bits of the address of the first Control Block to be executed. It should be noted that all Control Blocks must be built in the same 64 kbyte page of memory.

BIT 15 Don't Care, set to "zero"
BIT 14 Don't Care, set to "zero"
BIT 13 Don't Care, set to "zero"
BIT 12 Don't Care, set to "zero"

BIT 11 Don't Care, set to "zero"
BIT 10 Don't Care, set to "zero"
BIT 9 Don't Care, set to "zero"
BIT 8 Don't Care, set to "zero"

BIT 7 Don't Care, set to "zero"
BIT 6 Don't Care, set to "zero"
BIT 5 Don't Care, set to "zero"
BIT 4 Don't Care, set to "zero"

BIT 3 Address bit 19
BIT 2 Address bit 18
BIT 1 Address bit 17
BIT 0 Address bit 16

XIO REGISTERS
INTERNAL ALU

Name: **Current Buffer Pointer Register**
Address: **0104 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This register contains the current (or last executed) Data Buffer Address (MRT/MON), or Control Block Address (BC, Diagmode).

BIT 15 Address bit 15
BIT 14 Address bit 14
Bit 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO REGISTERS
INTERNAL ALU

Name: **DMA Disable Register**
Address: **0106 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The applications of the VMIVME-6000 vary significantly such that one user may need certain options while another may not. The VMIVME-6000 must DMA in information that might be required to execute the options. Obviously, it is desirable to eliminate DMA overhead when possible. A "one" written to a bit position of the DMA Disable Register will disable the corresponding DMA and that particular option. It is recommended that all unnecessary DMA be disabled. Note that, if a DMA is disabled, in most cases, the disabled function can be globally programmed by the host through a corresponding ALU register. If the DMA is disabled, and the corresponding ALU register is not programmed, the board will use default values for the function.

BIT 15 Unused
BIT 14 Gap Time - Measured intermessage gap in MRT/MON, selected intermessage gap in BC.
BIT 13 LS Time Tag - MRT/MON mode
BIT 12 MS Time Tag - MRT/MON mode

BIT 11 Auto Retry TSR Mask - BC mode
BIT 10 Auto Retry ISR Mask - BC mode
BIT 9 A Interrupt Mask - BC mode
BIT 8 B Interrupt Mask - BC mode

BIT 7 Response Time - BC, MON mode
BIT 6 Status Word 2 - BC,MON mode
BIT 5 Status Word 2 - BC,MON mode
BIT 4 New Data Pointer - MRT mode

BIT 3 Status Word 2 Mask - BC mode
BIT 2 Status Word 2 Mask - BC mode
BIT 1 Error Word Selects - BC mode
BIT 0 Error Generation - BC mode

XIO REGISTER
INTERNAL ALU

Name: **Interrupt Status Register (ISR)**
Address: **0108 (Hex)**
Address Space: **XIO**
Type: **Read**

Description: This register holds the current or last updated Interrupt Status Register. The Interrupt Status Register (ISR) is discussed in detail in Section 4.5.

BIT 15 **Transmission Error -** Refer to the Transmission Status Register (TSR) for more information as to what the error was (all modes).
BIT 14 **DMA Error -** A DMA has encountered some difficulty in transferring data to/from the host.
BIT 13 **Monitor Ring Buffer Page (64 bytes) Full.**
BIT 12 **Interrupt at End of Message -** End of Message interrupt was enable.

BIT 11 **Programming Error -** A programming error was detected.
BIT 10 **Status Word Mask Compared -** The status word received agreed with the SW mask (Bus Controller).
BIT 10 **Ring Buffer Full -** The next message will write over the beginning of the ring buffer.
BIT 9 **Stop -** Control Word in a Bus Controller or Diagmode Control Block had the "stop" bit set.
BIT 8 **Context Lock Lost -** Indicates the message was invalid (MON mode).

BIT 7 **Illegal Command Word Received -** A message was received that was addressed to the board, but required a protocol not enable by the host. (i.e. mode code not enabled)(MRT).
BIT 6 **CW Trigger -** CW Trigger Word (0112 Hex) matched received command word.
BIT 5 **Mode Code was Received -** Mode Code was executed (MRT/MON mode).
BIT 4 **Automatic Retry Successful -** An automatic retry was executed. The retry was successful (Bus Controller mode).
BIT 3 **Automatic Retry Failed -** Retry still did **Not** work. (Bus Controller mode)
BIT 3 **Bus Switchover -** The board ceased processing a message in order to process a message on the remaining bus (MRT/MON mode).
BIT 2 **BIT Failed -** The Built-In-Test was not successful.
BIT 1 **BIT Data Compare -** Data transmitted by board did **NOT** agree with the data received.
BIT 0 **Message was on B (secondary) Bus -**The message was executed on the B bus.

XIO REGISTER
INTERNAL ALU

Name: **Transmission Status Register (TSR)**
Address: **010A (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This register holds the current or last updated Transmission Status Register (TSR).

BIT 15 **Invalid Message Type -** T/R bit inverted. For instance, the Bus Controller (BC) transmits a Command Word with the T/R =1 and then sends data.
BIT 14 **Mode Code Error -** The RT detected an error involving mode codes. Could be protocol or inverted T/R bit.
BIT 13 **Bus Busy -** board had to subdue a transmission due to an already "active" 1553 bus.
BIT 12 **Transmitter Timeout -** A Transmission longer than 800 sec was detected.

BIT 11 **TA Compare -** Terminal Address (TA) in received SW did not compare to TA in CW.
BIT 10 **Instrumentation Bit Error**
BIT 9 **-Word Count Error**
BIT 8 **+Word Count Error**

BIT 7 **Reserved, set to logic "zero"**
BIT 6 **Gap Error -** A Gap between what was supposed to be contiguous words was detected.
BIT 5 **-BIT Count Error**
BIT 4 **+BIT Count Error**

BIT 3 **Response Error -** No response (or an invalid response) was detected.
BIT 2 **Sync Error -** The RT received a word with an improper sync. Note that, the first data word after a receive command will be detected as an RT to RT message.
BIT 1 **Parity -** Improper parity was detected.
BIT 0 **Manchester Error -** Invalid manchester waveform detected by the decoder.

XIO REGISTERS
INTERNAL ALU

Name: **"A" Interrupt Mask**
Address: **010C (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This ALU register holds the current Control Block A Interrupt Mask. The A Interrupt Mask is a mirror image of the Interrupt Status Register (ISR). The host sets bits in the A Interrupt Mask that will correspond to the events described by the ISR. If a bit is set by the board in the ISR, and the host has set the corresponding bit in the A Interrupt Mask, the board will generate an A Interrupt. See ISR for individual bit descriptions (this section).

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Mon Ring Buffer Page Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 SW Mask Compared/Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Auto Retry Successful

BIT 3 Auto Retry Fail/Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (Sec) Bus

XIO REGISTERS
INTERNAL ALU

Name: "B" Interrupt Mask
Address: 010E (Hex)
Address Space: XIO
Type: Read/Write

Description: The current Control Block B Interrupt Mask is contained in this ALU Register. The B Interrupt Mask is a mirror image of the Interrupt Status Register (ISR). The host sets bits in the B Interrupt mask that will correspond to the events described by the Interrupt Status Register. If a bit is set by the board in the ISR, and the host has set the corresponding bit in the B Interrupt Mask, the board will generate a B Interrupt. See ISR (0108 Hex) for individual bit descriptions (this section).

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Mon Ring Buffer Page Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 SW Mask Compared/Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Auto Retry Successful

BIT 3 Auto Retry Fail/Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (Sec) Bus

XIO REGISTERS
INTERNAL ALU

Name: **Auto Retry "B" Interrupt Mask**
Address: **0110 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Auto Retry B Interrupt Mask is programmed by the host to select the conditions that will cause the VMIVME-6000 to assert a B interrupt during an auto retry. If a bit is set in this mask, and the corresponding bit is set in the ISR during an auto retry, a B level interrupt will be generated. Note: The ISR is posted only if a B Interrupt occurs during retries. See ISR for (0108 Hex) individual bit descriptions (this section).

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Mon Ring Buffer Page Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 SW Mask Compared/Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

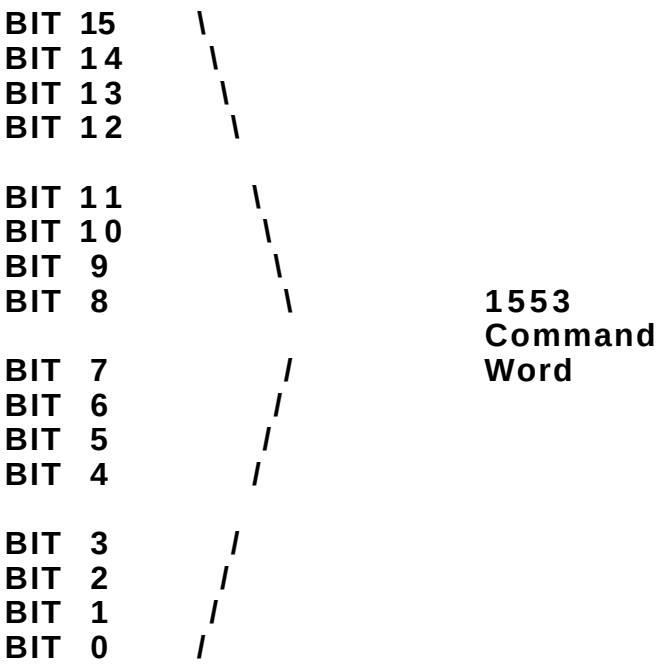
BIT 7 Illegal Command Word Received
BIT 6 CW
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Auto Retry Fail Bus
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (Sec) Bus

XIO REGISTERS
INTERNAL ALU

Name: **Command Word Trigger Register**
Address: **0112 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

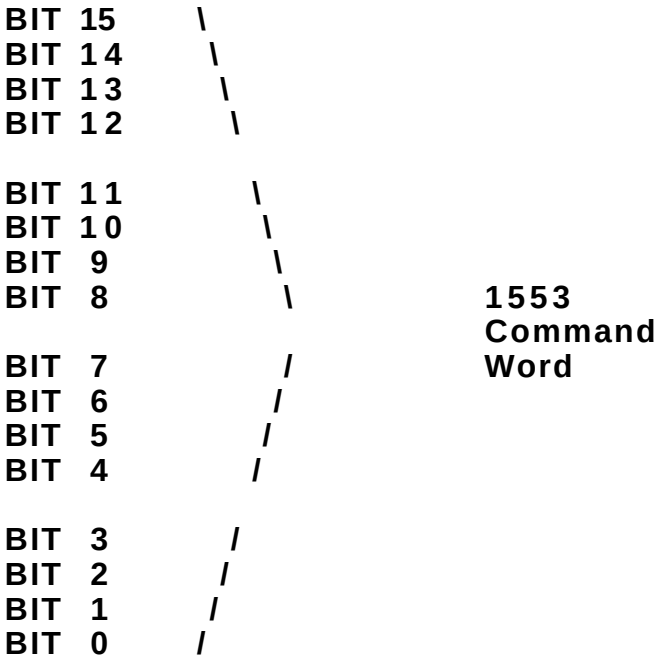
Description: If a Trigger on a particular 1553 Command Word (CW) is desired, the Command Word should be written to this register. If the board receives a Command Word that matches the Command Word Trigger, bit 6 of the ISR will be set to a logic "one".



XIO REGISTERS
INTERNAL ALU

Name: **Command Word Mask Register**
Address: **0114 (Hex)**
Address Space: **XIO**
Type: **ReadWrite**

Description: The Command Word Trigger Mask allows the host to eliminate bits from the CW compare. Corresponding "ones" eliminate those bits from the compare.



XIO REGISTERS
INTERNAL ALU

Name: **Auto Retry TSR Mask**
Address: **011A (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This register should be programmed by the host to establish a Master Auto Retry TSR Mask to be used if the corresponding DMA is disabled in the DMA Disable register. If the DMA is disabled, any bit set in this register that matches a corresponding bit set in the TSR will cause an Auto Retry in BC mode. See TSR (010A Hex) for individual bit descriptions in this section.

BIT 15 Invalid Message Type
BIT 14 Mode Code Error
BIT 13 Bus Busy
BIT 12 Transmitter Timeout

BIT 11 TA Compare
BIT 10 Instrumentation Bit Error
BIT 9 -Word Count Error
BIT 8 +Word Count Error

BIT 7 Reserved, set to logic "zero"
BIT 6 Gap Error
BIT 5 -BIT Count Error
BIT 4 +BIT Count Error

BIT 3 Response Error
BIT 2 Sync Error
BIT 1 Parity
BIT 0 Manchester Error

XIO REGISTERS
INTERNAL ALU

Name: **Auto Retry ISR Mask**
Address: **011C (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This register should be programmed by the host to establish a Master Auto Retry ISR Mask to be used if the corresponding DMA is disabled in the DMA Disable register. If the DMA is disabled, any bit set in this register that matches a corresponding bit set in the ISR will cause an Auto Retry in BC mode. See ISR (0108 Hex) for individual bit descriptions in this section.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Mon Ring Buffer Pages
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 SW Mask Compare/Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Auto Retry Successful

BIT 3 Auto Retry Fail
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (sec) Bus

XIO REGISTERS
INTERNAL ALU

Name: Interrupt Status Register Mask
Address: 011E (Hex)
Address Space: XIO
Type: Read/Write

Description: The Interrupt Status Register Mask may be programmed by the host to determine when the ISR is to be posted to a Control Block or data buffer, and when the ISR pointer is loaded. The ISR will not be posted unless a bit is set in this register that corresponds to a bit in the ISR, or bit 12 of the Option register is set. Default is all "ones" so that all nonzero ISRs will be posted. See ISR (0108 Hex) for individual bit descriptions, this section.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Mon Ring Buffer Pages
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 SW Mask Compare/Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Auto Retry Successful

BIT 3 Auto Retry Fail
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (sec) Bus

XIO REGISTERS
INTERNAL ALU

Name: **Transmission Status Register Mask**
Address: **0120 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Transmission Status Register Mask allows the host to determine which transmission errors cause bit 15 of the ISR to be set. The default is FFFF (Hex). See TSR (010A) for individual bit descriptions, this section .

BIT 15 Invalid Message Type
BIT 14 Mode Code Error
BIT 13 Bus Busy
BIT 12 Transmitter Timeout

BIT 11 TA Compare
BIT 10 Instrumentation Bit Error
BIT 9 -Word Count Error
BIT 8 +Word Count Error

BIT 7 Reserved, set to logic "zero"
BIT 6 Gap Error
BIT 5 -BIT Count Error
BIT 4 +BIT Count Error

BIT 3 Response Error
BIT 2 Sync Error
BIT 1 Parity
BIT 0 Manchester Error

XIO REGISTERS
INTERNAL ALU

Name: Error Mask
Address: 0122 (Hex)
Address Space: XIO
Type Write

Description: The Error Mask determines which conditions in the ISR cause the error bit (bit 0) of the ASR to be set. Default for this register is E88E (Hex).

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Mon Ring Buffer Page Full.
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 SW Mask Compared/Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Auto Retry Successful

BIT 3 Auto Retry Failed/Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

XIO REGISTERS
INTERNAL ALU

Name: **BC Pointer Table Origin**
Address: **0124 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: If the Bus Controller Pointer Table is to be used, this register should be programmed to point to the beginning of the table in on-board memory. See Link (Default Branch) in Section 4.3.2, BC Simulator mode for more details.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO REGISTERS
INTERNAL ALU

Name: BC Pointer Table Count
Address: 0126 (Hex)
Address Space: XIO
Type: Write

Description: The length of the BC Pointer Table is programmed through this register. When it reaches "zero", the board will automatically start over at the beginning of the table. See Link (Default Branch) in Section 4.3.2, BC Simulator mode for more details.

BIT 15 Count bit 15
BIT 14 Count bit 14
BIT 13 Count bit 13
BIT 12 Count bit 12

BIT 11 Count bit 11
BIT 10 Count bit 10
BIT 9 Count bit 9
BIT 8 Count bit 8

BIT 7 Count bit 7
BIT 6 Count bit 6
BIT 5 Count bit 5
BIT 4 Count bit 4

BIT 3 Count bit 3
BIT 2 Count bit 2
BIT 1 Count bit 1
BIT 0 Count bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Lower Error Select Word**
Address: **0128 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Lower Error Select Word ALU location should be programmed by the host if the corresponding DMA is disabled in the DMA Disable register. If the DMA is disabled, then this location will select the word(s) 1 through 16 that will contain errors. Section 4.6 gives details of the Error Word Selects (BC mode only).

BIT 15 Word 16
BIT 14 Word 15
BIT 13 Word 14
BIT 12 Word 13

BIT 11 Word 12
BIT 10 Word 11
BIT 9 Word 10
BIT 8 Word 9

BIT 7 Word 8
BIT 6 Word 7
BIT 5 Word 6
BIT 4 Word 5

BIT 3 Word 4
BIT 2 Word 3
BIT 1 Word 2
BIT 0 Word 1

XIO REGISTERS
INTERNAL ALU

Name: **Upper Error Select Word**
Address: **012C (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Upper Error Select Word ALU location should be programmed by the host if the corresponding DMA is disabled in the DMA Disable register. If the DMA is disabled, then this location will select the word(s) 17 through 32 that will contain errors. Section 4.6 gives details of the Error Word Select (BC mode only).

BIT 15 Word 32
BIT 14 Word 31
BIT 13 Word 30
BIT 12 Word 29

BIT 11 Word 28
BIT 10 Word 27
BIT 9 Word 26
BIT 8 Word 25

BIT 7 Word 24
BIT 6 Word 23
BIT 5 Word 22
BIT 4 Word 21

BIT 3 Word 20
BIT 2 Word 19
BIT 1 Word 18
BIT 0 Word 17

XIO REGISTERS
INTERNAL ALU

Name: **Error Generation (Diagmode)**
Address: **012A (Hex)**
Address Space: **XIO**
Type: **Write**

Description: This register may be used in Diagmode to enable Error Generation (refer to Section 4.6 for details of error generation).

BIT 15 Manchester - The particular bit time is programmable.
BIT 14 Parity
BIT 13 Sync
BIT 12 Bit Count Error - Word length programmable in Frame register.

BIT 11 TA Error - (MRT) Will force an erroneous +1 TA into Status Word.
BIT 10 +Word Count
BIT 9 -Word Count
BIT 8 Respond on Wrong Bus

BIT 7 Gap Between Data Words
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 SW1 - In both MRT and SIM modes.
BIT 2 SW2 - In both MRT and SIM modes.
BIT 1 Error in CW1 (BC)/Positive Sync Words (Diag)
BIT 0 Error in CW2 (BC)/Neg Sync Words (Diag)

XIO REGISTERS
INTERNAL ALU

Name: **Built-In-Test (BIT) Word**
Address: **012E (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The format of the Built-In-Test (BIT) word is updated during the loop around test, Diagmode, and self-test. This register reflects the status of the 1553 logic, which is transmitted in response to a "Transmit BIT Word" Mode Code.

BIT 15 Spare
BIT 14 DMA Error
BIT 13 Bus A Shutdown
BIT 12 Bus B Shutdown

BIT 11 Bus A Self-Test Failure
BIT 10 Bus B Self-Test Failure
BIT 9 Memory Self-Test Failure
BIT 8 ALU Failure

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Reserved, set to logic "zero"
BIT 2 Internal BIT Failure
BIT 1 Reserved, set to logic "zero"
BIT 0 Illegal Mode Code Received

XIO REGISTERS
INTERNAL ALU

Name: DMA Timeout
Address: 0130 (Hex)
Address Space: XIO
Type: Read/Write

Description: Certain DMAs performed by the VMIVME-6000 have a flexible latency. In those cases, the count within the DMA Timeout Register will determine the latency. The default will be 20 μsec. Note that, if DMAs are not completed when needed, the gap will be extended by the amount of extra time needed to complete the DMA.

BIT 15 Count bit 15
BIT 14 Count bit 14
BIT 13 Count bit 13
BIT 12 Count bit 12

BIT 11 Count bit 11
BIT 10 Count bit 10
BIT 9 Count bit 9
BIT 8 Count bit 8

BIT 7 Count bit 7
BIT 6 Count bit 6
BIT 5 Count bit 5
BIT 4 Count bit 4

BIT 3 Count bit 3
BIT 2 Count bit 2
BIT 1 Count bit 1
BIT 0 Count bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Response Time**
Address: **0134 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: If the response time is disabled in the DMA Disable register and the VMIVME-6000 is being used in Bus Simulator mode, the host should program this register with the response time (in microseconds) of the status word(s) to be simulated. (BC/SIM mode only). The response time for the simulated SW1 should be placed in bits 15-8, while the response time of a simulated SW2 should be put in bits 7-0.

BIT 15 SW1 Response time bit 7
BIT 14 SW1 Response time bit 6
BIT 13 SW1 Response time bit 5
BIT 12 SW1 Response time bit 4

BIT 11 SW1 Response time bit 3
BIT 10 SW1 Response time bit 2
BIT 9 SW1 Response time bit 1
BIT 8 SW1 Response time bit 0

BIT 7 SW2 Response time bit 7
BIT 6 SW2 Response time bit 6
BIT 5 SW2 Response time bit 5
BIT 4 SW2 Response time bit 4

BIT 3 SW2 Response time bit 3
BIT 2 SW2 Response time bit 2
BIT 1 SW2 Response time bit 1
BIT 0 SW2 Response time bit 0

XIO REGISTERS
INTERNAL ALU

Name: **BC Intermessage Gap**
Address: **0136 (Hex)**
Address Space: **XIO**
Type **Read/Write**

Description: In BC/SIM MODE, this register is programmed by the host if the gap time DMA is disabled in the DMA Disable register. The time (in microseconds) from the completion of the previous message to the start of the next message required by the host should be loaded into the register.

BIT 15 Gap time bit 15
BIT 14 Gap time bit 14
BIT 13 Gap time bit 13
BIT 12 Gap time bit 12

BIT 11 Gap time bit 11
BIT 10 Gap time bit 10
BIT 9 Gap time bit 9
BIT 8 Gap time bit 8

BIT 7 Gap time bit 7
BIT 6 Gap time bit 6
BIT 5 Gap time bit 5
BIT 4 Gap time bit 4

BIT 3 Gap time bit 3
BIT 2 Gap time bit 2
BIT 1 Gap time bit 1
BIT 0 Gap time bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Ring Buffer Address**
Address: **0138 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This register contains the current 16-bit Ring Buffer Address. It is used internally by the VMIVME-6000 and is normally not accessed by the host.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Ring Buffer Map**
Address: **013A (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: This register contains the current 4-bit Ring Buffer Map. It is used internally by the VMIVME-6000 and is normally not accessed by the host.

BIT 15 Don't Care, set to logic "zero"
BIT 14 Don't Care, set to logic "zero"
BIT 13 Don't Care, set to logic "zero"
BIT 12 Don't Care, set to logic "zero"

BIT 11 Don't Care, set to logic "zero"
BIT 10 Don't Care, set to logic "zero"
BIT 9 Don't Care, set to logic "zero"
BIT 8 Don't Care, set to logic "zero"

BIT 7 Don't Care, set to logic "zero"
BIT 6 Don't Care, set to logic "zero"
BIT 5 Don't Care, set to logic "zero"
BIT 4 Don't Care, set to logic "zero"

BIT 3 Address bit 19
BIT 2 Address bit 18
BIT 1 Address bit 17
BIT 0 Address bit 16

XIO REGISTERS
INTERNAL ALU

Name: **Status Word 1 (SW1) Mask**
Address: **013C (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: In Bus Controller Mode, if the SW1 mask is disabled in the DMA Disable register, the host may program a master SW1 mask in this register. If a bit set in the SW1 mask corresponds to a bit set in the received SW, then bit 10 of the ISR will be set. If the A or B interrupt masks are set up for bit 10, then a corresponding A or B interrupt would be generated.

BIT 15 Don't Care, set to "zero"
BIT 14 Don't Care, set to "zero"
BIT 13 Don't Care, set to "zero"
BIT 12 Don't Care, set to "zero"

BIT 11 Don't Care, set to "zero"
BIT 10 Status Word bit 10
BIT 9 Status Word bit 9
BIT 8 Status Word bit 8

BIT 7 Status Word bit 7
BIT 6 Status Word bit 6
BIT 5 Status Word bit 5
BIT 4 Status Word bit 4

BIT 3 Status Word bit 3
BIT 2 Status Word bit 2
BIT 1 Status Word bit 1
BIT 0 Status Word bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Status Word 2 (SW2) Mask**
Address: **013E (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: In Bus Controller Mode, if the SW2 mask is disabled in the DMA Disable register, the host may program a master SW2 mask in this register. If a bit set in the SW2 mask corresponds to a bit set in the received SW, then bit 10 of the ISR will be set. If the A or B interrupt masks are set up for bit 10, then a corresponding A or B interrupt would be generated.

BIT 15 Don't Care, set to "zero"
BIT 14 Don't Care, set to "zero"
BIT 13 Don't Care, set to "zero"
BIT 12 Don't Care, set to "zero"

BIT 11 Don't Care, set to "zero"
BIT 10 Status Word bit 10
BIT 9 Status Word bit 9
BIT 8 Status Word bit 8

BIT 7 Status Word bit 7
BIT 6 Status Word bit 6
BIT 5 Status Word bit 5
BIT 4 Status Word bit 4

BIT 3 Status Word bit 3
BIT 2 Status Word bit 2
BIT 1 Status Word bit 1
BIT 0 Status Word bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Word Count Error Plus**
Address: **0144 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Word Count Error Plus location is programmed by the host to select the number of extra words to be included when the VMIVME-6000 is injecting a +word count error in MRT mode. Default is one extra word. (MRT mode only, does not apply to mode codes). Note that, in BC mode, a Word Count Error Plus is generated by programming the word count location of the Control Block to be greater than the word count specified by the Command Word of that Control Block.

BIT 15 Don't Care, set to logic "zero"
BIT 14 Don't Care, set to logic "zero"
BIT 13 Don't Care, set to logic "zero"
BIT 12 Don't Care, set to logic "zero"

BIT 11 Don't Care, set to logic "zero"
BIT 10 Don't Care, set to logic "zero"
BIT 9 Don't Care, set to logic "zero"
BIT 8 Don't Care, set to logic "zero"

BIT 7 Don't Care, set to logic "zero"
BIT 6 Don't Care, set to logic "zero"
BIT 5 Don't Care, set to logic "zero"
BIT 4 Extra Word Count 4

BIT 3 Extra Word Count 3
BIT 2 Extra Word Count 2
BIT 1 Extra Word Count 1
BIT 0 Extra Word Count 0

XIO REGISTERS
INTERNAL ALU

Name: **Word Count Error Minus**
Address: **0146 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Word Count Error Minus location is programmed by the host to select the number of words in a message that will be deleted from the message transmission when the VMIVME-6000 is injecting a Word Count Error Minus in MRT mode. Default is minus one word. (MRT only, does not apply to mode codes). Note that, in BC mode, a Word Count Error Minus is generated by programming the word count location of the Control Block to be less that the word count specified by the Command Word of that Control Block.

BIT 15 Don't Care, set to logic "zero"
BIT 14 Don't Care, set to logic "zero"
BIT 13 Don't Care, set to logic "zero"
BIT 12 Don't Care, set to logic "zero"

BIT 11 Don't Care, set to logic "zero"
BIT 10 Don't Care, set to logic "zero"
BIT 9 Don't Care, set to logic "zero"
BIT 8 Don't Care, set to logic "zero"

BIT 7 Don't Care, set to logic "zero"
BIT 6 Don't Care, set to logic "zero"
BIT 5 Don't Care, set to logic "zero"
BIT 4 Don't Care, set to logic "zero"

BIT 3 Don't Care, set to logic "zero"
BIT 2 Don't Care, set to logic "zero"
BIT 1 Don't Care, set to logic "zero"
BIT 0 Don't Care, set to logic "zero"

XIO REGISTERS
INTERNAL ALU

Name: **Major Frame Time LSW**
Address: **0148 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The time it takes from start of the execution of one entire control block list (in BC mode) to the start of the next Control Block list is termed the Major Time Frame. The host may vary the Major frame time (in microseconds) by writing a nonzero value to the 32-bit major time frame registers (MSW and LSW). If enabled in Control Word 2, the board will wait the time specified by the 32-bit major time register before restarting the list. Bit 7 of Control Word 2 should be set in the last Control Block of the list.

BIT 15 Major Frame Time bit 15
BIT 14 Major Frame Time bit 14
BIT 13 Major Frame Time bit 13
BIT 12 Major Frame Time bit 12

BIT 11 Major Frame Time bit 11
BIT 10 Major Frame Time bit 10
BIT 9 Major Frame Time bit 9
BIT 8 Major Frame Time bit 8

BIT 7 Major Frame Time bit 7
BIT 6 Major Frame Time bit 6
BIT 5 Major Frame Time bit 5
BIT 4 Major Frame Time bit 4

BIT 3 Major Frame Time bit 3
BIT 2 Major Frame Time bit 2
BIT 1 Major Frame Time bit 1
BIT 0 Major Frame Time bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Major Frame Time MSW**
Address: **014A (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: See Major Frame Time LSW above.

BIT 15 Major Frame Time bit 32
BIT 14 Major Frame Time bit 31
BIT 13 Major Frame Time bit 30
BIT 12 Major Frame Time bit 29

BIT 11 Major Frame Time bit 28
BIT 10 Major Frame Time bit 27
BIT 9 Major Frame Time bit 26
BIT 8 Major Frame Time bit 25

BIT 7 Major Frame Time bit 24
BIT 6 Major Frame Time bit 23
BIT 5 Major Frame Time bit 22
BIT 4 Major Frame Time bit 21

BIT 3 Major Frame Time bit 20
BIT 2 Major Frame Time bit 19
BIT 1 Major Frame Time bit 18
BIT 0 Major Frame Time bit 17

XIO REGISTERS
INTERNAL ALU

Name: Minor Frame Time LSW
Address: 014C (Hex)
Address Space: XIO
Type: Read/Write

Description: The Minor Frame Time is controlled by a 32-bit counter that may be programmed to set up minor time frames (in microseconds) within or excluding a major time frame. Bit 6 of Control Word 2 should be set in the last Control Block of the Minor Frame.

BIT 15 Minor Frame Time 15
BIT 14 Minor Frame Time 14
BIT 13 Minor Frame Time 13
BIT 12 Minor Frame Time 12

BIT 11 Minor Frame Time 11
BIT 10 Minor Frame Time 10
BIT 9 Minor Frame Time 9
BIT 8 Minor Frame Time 8

BIT 7 Minor Frame Time 7
BIT 6 Minor Frame Time 6
BIT 5 Minor Frame Time 5
BIT 4 Minor Frame Time 4

BIT 3 Minor Frame Time 3
BIT 2 Minor Frame Time 2
BIT 1 Minor Frame Time 1
BIT 0 Minor Frame Time 0

XIO REGISTERS
INTERNAL ALU

Name: Minor Frame Time MSW
Address: 014E (Hex)
Address Space: XIO
Type: Read/Write

Description: See Minor Frame Time LSW above.

BIT 15 Minor Frame Time 31
BIT 14 Minor Frame Time 30
BIT 13 Minor Frame Time 29
BIT 12 Minor Frame Time 28

BIT 11 Minor Frame Time 27
BIT 10 Minor Frame Time 26
BIT 9 Minor Frame Time 25
BIT 8 Minor Frame Time 24

BIT 7 Minor Frame Time 23
BIT 6 Minor Frame Time 22
BIT 5 Minor Frame Time 21
BIT 4 Minor Frame Time 20

BIT 3 Minor Frame Time 19
BIT 2 Minor Frame Time 18
BIT 1 Minor Frame Time 17
BIT 0 Minor Frame Time 16

XIO REGISTERS
INTERNAL ALU

Name: **Programming Error Register**
Address: **0150 (Hex)**
Address Space: **XIO**
Type **Read/Write**

Description: The Programming Error Register provides information as to the cause of the programming error bit being set in the ISR (Bit 11). Bit 15-0 below identifies the contents of the Programming Error Register.

BIT 15 **Invalid Mode -** The user attempted to enter an invalid mode.
BIT 14 **Invalid Gap -** Intermessage gap less than the allowable 30 sec (Bus Controller).
BIT 13 **Invalid Response Timeout -** Has to be "0" (default) or 7 or greater.
BIT 12 **Data Word Count -** Data Word Count of control block and word count of the command word do not agree, or the word counts of both command words of an RT-RT message do not agree.
BIT 11 **Invalid XIO -** Invalid XIO Command was attempted.
BIT 10 **Inconsistent Control Word -** An inconsistent control word such as RT to BC (bit 15) and RT to RT (bit 14) "set" in the same message (Bus Controller).
BIT 9 **SA Flags/Option Inconsistent -** Inconsistent bits set in the SA flags or SA options such as both start and stop record.
BIT 8 **BC Pointer/Conditional Branch Count = 0 -** The BC pointer table or a conditional branch was enable but the count was "0".
BIT 7 **Major Time Frame -** Major time frame is enabled but the counters are LESS than the time to executed the list.
BIT 6 **Dynamic Bus Allocation Error -** A CBADDR (Control Block Address) for the new mode wasn`t given.
BIT 5 **Invalid CBADDR -** CBADDR was "0" during START XIO. The board will still attempted to start.
BIT 4 **RT Count = 0 -** If a START initialization is executed there should have been at least 1 RT (MRT/MON).
BIT 3 **Invalid Pointer -** Initial Ring Buffer Pointer are invalid.
BIT 2 **RT Control Word -** BIT 9 (simulate) or 8 (monitor) has to be set in the RT Control Word.
BIT 1 **Both Simulate and Broadcast Enabled in same MESSAGE.**
BIT 0 **DMA Latency -** Caused Programmed Gap Time to be exceeded.

XIO REGISTERS
INTERNAL ALU

Name: **Data Word Gap**
Address: **0152 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description : The Data Word Gap register is used by the host to program the amount of extra gap (in microseconds) to include between data words when the VMIVME-6000 is injecting a Gap Error. Default is 1 µsec.

BIT 15 Data Gap Time bit 15
BIT 14 Data Gap Time bit 14
BIT 13 Data Gap Time bit 13
BIT 12 Data Gap Time bit 12

BIT 11 Data Gap Time bit 11
BIT 10 Data Gap Time bit 10
BIT 9 Data Gap Time bit 9
BIT 8 Data Gap Time bit 8

BIT 7 Data Gap Time bit 7
BIT 6 Data Gap Time bit 6
BIT 5 Data Gap Time bit 5
BIT 4 Data Gap Time bit 4

BIT 3 Data Gap Time bit 3
BIT 2 Data Gap Time bit 2
BIT 1 Data Gap Time bit 1
BIT 0 Data Gap Time bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Dynamic Bus Control RT Map**
Address: **0154 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Dynamic Bus Control RT Map may be programmed by the host with the map address of the MRT header block to use in configuring the VMIVME-6000 from a BC-to-MRT after Dynamic Bus Control has been accepted by an RT.

BIT 15 Don't Care, set to "zero"
BIT 14 Don't Care, set to "zero"
BIT 13 Don't Care, set to "zero"
BIT 12 Don't Care, set to "zero"

BIT 11 Don't Care, set to "zero"
BIT 10 Don't Care, set to "zero"
BIT 9 Don't Care, set to "zero"
BIT 8 Don't Care, set to "zero"

BIT 7 Don't Care, set to "zero"
BIT 6 Don't Care, set to "zero"
BIT 5 Don't Care, set to "zero"
BIT 4 Don't Care, set to "zero"

BIT 3 Address bit 19
BIT 2 Address bit 18
BIT 1 Address bit 17
BIT 0 Address bit 16

XIO REGISTERS
INTERNAL ALU

Name: **Dynamic Bus Control RT Address**
Address: **0156 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Dynamic Bus Control RT Address may be programmed by the host with the address of the MRT header block to use in configuring the VMIVME-6000 from a BC-to-MRT after Dynamic Bus Control has been accepted by an RT.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Dynamic Bus Control Map**
Address: **0158 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Dynamic Bus Control Map may be programmed by the host with the map address of the Bus Control CB to use in configuring the VMIVME-6000 from a RT-to-BC after Dynamic Bus Control has been accepted by an RT.

BIT 15 Don't Care, set to "zero"
BIT 14 Don't Care, set to "zero"
BIT 13 Don't Care, set to "zero"
BIT 12 Don't Care, set to "zero"

BIT 11 Don't Care, set to "zero"
BIT 10 Don't Care, set to "zero"
BIT 9 Don't Care, set to "zero"
BIT 8 Don't Care, set to "zero"

BIT 7 Don't Care, set to "zero"
BIT 6 Don't Care, set to "zero"
BIT 5 Don't Care, set to "zero"
BIT 4 Don't Care, set to "zero"

BIT 3 Address bit 19
BIT 2 Address bit 18
BIT 1 Address bit 17
BIT 0 Address bit 16

XIO REGISTERS
INTERNAL ALU

Name: Dynamic Bus Control Address
Address: 015A (Hex)
Address Space: XIO
Type: Read/Write

Description: The Dynamic Bus Control address may be programmed by the host with the address of the Bus Control CB to use in configuring the VMIVME-6000 from a RT-to-BC after Dynamic Bus Control has been accepted by an RT.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Dynamic Bus Control Disable**
Address: **015C (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Dynamic Bus Control address may be programmed by the host with the address of the Bus Control (CB) to use in configuring the VMIVME-6000 from a RT-to-BC after Dynamic Bus Control has been accepted by an RT.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Dynamic Bus Control Status Word Mask**
Address: **015E (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Dynamic Bus Control Status Word Mask may be programmed by the host to determine if the dynamic bus allocation should be accepted in MRT mode based on bits in the Status Word.

BIT 15 Don't care, set to "zero"
BIT 14 Don't care, set to "zero"
BIT 13 Don't care, set to "zero"
BIT 12 Don't care, set to "zero"

BIT 11 Don't care, set to "zero"
BIT 10 Status Word bit 10
BIT 9 Status Word bit 9
BIT 8 Status Word bit 8

BIT 7 Status Word bit 7
BIT 6 Status Word bit 6
BIT 5 Status Word bit 5
BIT 4 Status Word bit 4

BIT 3 Status Word bit 3
BIT 2 Status Word bit 2
BIT 1 Status Word bit 1
BIT 0 Status Word bit 0

XIO REGISTERS
INTERNAL ALU

Name: Revision Register
Address: 0180 (HEX)
Address Space: XIO
Type: Read

Description: This Register contains the current revision of microcode for the VMIVME-6000.

BIT 15 Revision bit 15
BIT 14 Revision bit 14
BIT 13 Revision bit 13
BIT 12 Revision bit 12

BIT 11 Revision bit 11
BIT 10 Revision bit 10
BIT 9 Revision bit 9
BIT 8 Revision bit 8

BIT 7 Revision bit 7
BIT 6 Revision bit 6
BIT 5 Revision bit 5
BIT 4 Revision bit 4

BIT 3 Revision bit 3
BIT 2 Revision bit 2
BIT 1 Revision bit 1
BIT 0 Revision bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Lost B Interrupt Counter**
Address: **0198 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Lost B Interrupt Counter register contains the number of times the board has asserted a new B Interrupt before the previous B interrupt was serviced.

BIT 15 Count bit 15
BIT 14 Count bit 14
BIT 13 Count bit 13
BIT 12 Count bit 12

BIT 11 Count bit 11
BIT 10 Count bit 10
BIT 9 Count bit 9
BIT 8 Count bit 8

BIT 7 Count bit 7
BIT 6 Count bit 6
BIT 5 Count bit 5
BIT 4 Count bit 4

BIT 3 Count bit 3
BIT 2 Count bit 2
BIT 1 Count bit 1
BIT 0 Count bit 0

XIO REGISTERS
INTERNAL ALU

Name: **Lost B Interrupt Pointer**
Address: **019A (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The Lost B Interrupt pointer contains the address in MRT/MON RAM where the next Lost B Interrupt Pointer will be stored.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

4.2.4 Active XIO

When the VMIVME-6000 is processing a Command Word or Control Block, and the "Board Active" bit (bit 15) is set in the Active Status Register (ASR), the firmware is **not** readily available to process XIOs. During processing of 1553 messages or Control Blocks, the firmware may not service the pending XIO for up to 1 msec. The Host must follow the guidelines for processing a Special Function XIO and an access to the Internal ALU registers to ensure that the data transfer is successful (see Sections 4.2.2.2 and 4.2.2.3 for details on processing XIOs).

If "Active XIOs" are being used, an interrupt may be programmed in the Control Register (bit 12) to signal the host on the completion of the Active XIO, so that polling of the ASR would not be needed.

Note that, normally, the host will **not** be accessing registers that require firmware intervention while the VMIVME-6000 is "Active".

4.3 OPERATIONAL MODES

The following section describes the operating modes and control block structures of the VMIVME-6000. The control block information is constructed by the host in the on-board RAM. Note that, before the host may access the on-board RAM to construct control blocks, the memory enable bit (bit 15) of the Control and Status register (Section 4.2.1.1) must be set to a logic "one".

There are three basic active modes of the VMIVME-6000: Self-Test/Diagmode, Bus Controller/Simulator, and Multiple Remote Terminal/Monitor. OFF Mode is not a host-selected mode, but is the state of the board after power-up, reset, or a host-initiated CLEAR or SHUTDOWN command. The current mode of the VMIVME-6000 is available to the host in the ASR as shown in the description in Section 4.2.2.1. Figure 4.3-1 lists the operational modes and their numerical assignments.

Table 4.3-1. VMIVME-6000 Mode Assignments

Value	Mode Assignment
0	Off Mode
1	Bus Controller/Simulator Mode
2	Diagmode
3	MRT/Monitor Mode with Initialization
4	MRT/Monitor Mode without Initialization (Quick Start)
5 - FFFF	Invalid Mode

M6000/T4.3-1

Note

MRT/MON with, and without, initialization will have a mode value of 4 in the ASR.

4.3.1 Self-Test

The board has two types of Self-Test. The power-up self-test is self-contained within the board and requires no host interaction. The Diagmode is a self-test in which the host has control.

4.3.1.1 Power-Up Self-Test

The Power-Up Self-Test is automatically executed upon:

a. Power-Up
b. Reception of "Execute Self-Test Mode Code"
c. Release of the Reset signal

It executes an internal VMIVME-6000 ALU, sequencer, RAM, and internal bus test. The results are provided through the ASR and BIT word. The ISR and TSR (internal RAM registers) are cleared and updated also.

4.3.1.2 Diagmode

Diagmode is the host-controlled self-test. The host initiates Diagmode via the "START" Special Function XIO. It updates the Built-In-Test word and ASR based on the results. Diagmode allows the host to test the board's ability to access on-board memory, and also test both the A and B 1553 bus logic.

The memory test, or DMA test as it is also called, reads a host-supplied test word from on-board memory, and echos or writes back the word to the next address (echo location). The board will then read the echo word and compare the actual data with the test word. Errors will be shown globally in the ASR, and in each individual Diagmode Control Block.

The 1553 bus test is a loopback test where the board will transmit a host-supplied word through the 1553 transmit logic, and receive/validate the word in the 1553 receiver logic. The host may select whether the loopback is internal to the 1553 encoder/decoder, or external on the actual 1553 bus. If the test is external, the bus must be properly configured and terminated for correct operation.

4.3.1.3 Diagmode Control Block

The Diagmode Control Block format is shown in Figure 4.3.1.3-1. The Diagmode Control Blocks are constructed by the host in on-board memory and are accessed by the VMIVME-6000 via DMA.

Table 4.3.1.3-1. Diagmode Control Block

Byte Address	
0	Control Word
2	Link
4	DMA Test Count N
6	Bus Test Count N
8	DMA Word 1
A	DMA Echo Word 1
	:
	DMA Word N
	DMA Echo Word N
	1553 Bus Test Word 1 Positive SYNC
	1553 Bus Test Word 1 ECHO
	ISR 1
	TSR 1
	1553 Bus Test Word 1 Negative SYNC
	1553 Bus Test Word 1 ECHO
	ISR 1
	TSR 1
	:
	1553 Bus Test Word N - Positive SYNC
	1553 Bus Test Word ECHO
	ISR N
	TSR N
	1553 Bus Test Word N - Negative SYNC
	1553 Bus Test Word ECHO
	ISR N
	TSR N

M6000/T 4.3.1.3.1

DIAGMODE
DIAGMODE CONTROL BLOCK

Name: **Diagmode Control Word**
Address: **Base Address + 0000 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The control word is shown below. Having bit 15 set causes the board to return to OFF mode after completion of the block. Bit 12 set causes an interrupt after the completion of the Diagmode block. A "one" in bit 4 causes a 50 nsec pulse at the scope sync output before the bus test begins. Bit 1 determines if the 1553 bus tests are internal or external wraparound. Bit 0 determines which bus (A or B) the test will be on.

BIT 15 **Stop** - VMIVME-6000 will stop (return to OFF mode) after this control block is executed.
BIT 14 **Reserved, set to logic "zero"**
BIT 13 **Reserved, set to logic "zero"**
BIT 12 **Interrupt at End of Message** - The VMIVME-6000 will generate an interrupt at the completion of this Diagmode block.

BIT 11 **Reserved, set to logic "zero"**
BIT 10 **Reserved, set to logic "zero"**
BIT 9 **Reserved, set to logic "zero"**
BIT 8 **Reserved, set to logic "zero"**

BIT 7 **Reserved, set to logic "zero"**
BIT 6 **Reserved, set to logic "zero"**
BIT 5 **Reserved, set to logic "zero"**
BIT 4 **Scope Sync Enable**

BIT 3 **Reserved, set to logic "zero"**
BIT 2 **Reserved, set to logic "zero"**
BIT 1 **Internal Wraparound** - A "one" will cause transmitter inhibit to be active suppressing transmission on the 1553 bus.
BIT 0 **Bus Select**
0 A Bus
1 B Bus

DIAGMODE
DIAGMODE CONTROL BLOCK

Name: **Link**
Address: **Base Address + 0002 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The next word in the Control Block is the Link. It should point to the next Control Block to be executed. If no other Control Blocks are to be executed (i.e., the "STOP" bit is set in the Control Word), this location is a "don't care".

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

DIAGMODE
DIAGMODE CONTROL BLOCK

Name: **Test Counts**
Address: **Base Address + 0004 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The test counts determine the number of times the tests will be performed. The actual format of the control block is determined by the test count and allowances must be made to that effect.

BIT 15 Count bit 15
BIT 14 Count bit 14
BIT 13 Count bit 13
BIT 12 Count bit 12

BIT 11 Count bit 11
BIT 10 Count bit 10
BIT 9 Count bit 9
BIT 8 Count bit 8

BIT 7 Count bit 7
BIT 6 Count bit 6
BIT 5 Count bit 5
BIT 4 Count bit 4

BIT 3 Count bit 3
BIT 2 Count bit 2
BIT 1 Count bit 1
BIT 0 Count bit 0

Diagmode Test Verification: The next location should contain the first DMA test word. The VMIVME-6000 will read the first test word from on-board memory via DMA. Then the test word will be written via DMA to the next on-board memory location. After this the echo word is read back and compared to the test word to see if the test was successful, or if it failed. A failure will cause bit 2 of the ISR to be set. The board continues until the test count has decremented to "zero".

The bus test is composed of two parts; a positive and negative sync test. This two-part test is considered one test to the bus test count. The VMIVME-6000 gets the test word and routes it through the transmitter/receiver. It checks for data compare and all the usual word validation criteria, and posts the resulting status accordingly. Eight locations per bus test count should be allocated to the Control Block.

4.3.2 Bus Controller/Simulator Mode

Bus Controller/Simulator is based on a flexible Control Block (CB) structure that, along with internal host programmable registers, allows the VMIVME-6000 to initiate all ten defined MIL-STD-1553B message formats. The board will execute the Control Blocks independent of the host until an A interrupt occurs or the STOP bit (bit 15 of the Control Word 2 in the CB) is detected.

In addition to being the bus controller, the Status Response to any of the message formats may be simulated by the VMIVME-6000, allowing the board to simulate an entire 1553 system. Enabling of Status Response simulation is programmable in Control Word 1 of the Bus Controller/Control Block. The Status Word to be transmitted in response to CW1 should be written into the SW1 location of the Bus Controller/Control Block. The Status Word transmitted in response to CW2 should be written into the SW2 location of the Control Block. Any data to be transmitted as a response to a transmit command should be loaded into the data buffer pointed to by the BC Control Block data pointer and map.

Bus Controller/Control Block: The Bus Controller/Control Block is shown in Table 4.3.3-1. There should be one Control Block per message. The basic BC Control Block consists of only the first 22-words . The remaining locations provide inputs for optional Auto Retry and Branching features of the VMIVME-6000, and need be allocated only up to the last location used. Some of the features of this mode include: programmable intermessage gaps, programmable response timeout, message level interrupts, 1553 status response simulation, broadcast, and programmable Scope SYNC. In cases where these options are not used, the board will default to a predefined protocol.

Branch Programming: Bus Controller is capable of executing conditional branches (links) to different control blocks. Bits 11 to 8 of Control Word 2 constitute the Branch Count. The board has up to 15 conditional links and corresponding masks. The number of conditional links is programmable through the Branch Count. If the Branch Count is nonzero, the board will acquire Branch Mask 1 and compare it to the ISR for the just completed message. If the logical AND has a nonzero result, the board will use the contents of Branch Address 1 as the link to the next Control Block. If the result is "zero", the branch count will be decremented and the same procedure will occur for Branch Mask 2. The board will continue the process until a conditional branch occurs, or the branch count is decremented to "zero". If the count reaches "zero" before a branch occurs, the board will use the contents of the Link location (word 2 of the Control Block) as the default link.

Major Time Frame: The Major Time Frame counter is a 32-bit counter that should be programmed to what the Major Time Frame should be. The increments of the counter are 1 μsec. If bit 7 of Bus Controller Control Word 2 is set, the VMIVME-6000 treats the control block as the last control block in the Major Time Frame. It will wait until the Major Time Frame counter has reached "zero" before continuing to the next Control Block.

Minor Time Frame: The Minor Time Frame counter is a 32-bit counter that should be programmed to what the Minor Time Frame should be. The increments of the counter are 1 μsec. If bit 6 of Control Word 2 is set, the VMIVME-6000 will treat the control block as the last control block within a Minor time Frame. The board will wait until the minor time frame counters have reached "zero" before continuing to the next Control Block.

Automatic Retry: An Automatic Retry of the previous BC message will occur if bits 2, 1, and 0 of Control Word 2 are nonzero, and if any of the following conditions exist:

a. The AUTO TSR MASK is nonzero and has a bit set that corresponds to a bit set in the Transmission Status Register.

b. The status response has a bit set that corresponds to a bit set in the AUTO SW Mask.

Bits 2, 1, and 0 of BC Control Word 2 must be nonzero in order for an automatic retry to occur. The board executes automatic retries independent of the host CPU (of course, the host may interrupt and execute its own automatic retry if desired). The following automatic retry parameters are programmable:

a. Number of retries
b. The 1553 Bus on which the retry will occur
c. Transmission errors that initiate automatic retry (via Control Block and Auto Retry TSR Mask)
d. Status word response bits that, when set, initiate automatic retry (in control block, Auto Retry SW Mask) (default is that no SW bits initiate automatic retry)

Bus Controller Data Buffer: The Bus Controller Data Buffer format is shown in Table 4.3.2-1. The locations starting at word 0 of the Data Buffer is reserved for the data words of the associated message. Actual size of the data buffer is determined by the data word count of the Bus Controller/Control Block. The locations may hold transmitted or received data as specified by the message type of the corresponding Control Block.

Table 4.3.2-1. Bus Controller/Simulator Data Buffer

Byte Address	Description
0 -	Data Word 1
2 -	Data Word 2
.	
.	
N -	Last Data Word

M6000/T4.3.2-1

Table 4.3.2-2. Bus Controller Control Block

Byte Address	
0	Control Word 1
2	Control Word 2
4	Link (Default Branch)
6	Data Map
8	Data Pointer
A	Response Timeout/Data Word Count
C	Intermessage Gap Time
E	Reserved
10	Interrupt Status (ISR)
12	Transmission Status (TSR)
14	Command Word 1 (CW1)
16	Status Word 1 (SW1)
18	Command Word 2 (CW2 RT-RT Only)
1A	Status Word 2 (SW2-RT-RT Only)
1C	Response Time SW2/SW1
1E	SW1 Interrupt Mask
20	SW2 Interrupt Mask
22	A Interrupt Mask
24	B Interrupt Mask
26	Error Generation Selects
28	Error Word Selects 1-16
2A	Error Word Selects 17-32
2C	Auto Retry TSR Mask
2E	Auto Retry SW Mask
30	Reserved
32	Reserved
34	Reserved
36	Reserved
38	Branch Mask 1
3A	Branch Address 1

	Branch Mask 15
	Branch Address 15

M6000/T4.3.2-2

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Bus Controller/Control Word 1**
Address: **CB Base Address + 0000 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: Bus Controller/Control Word 1 provides the following information:

BIT 15 **BC-to-RT/RT-to-BC -** If low, the Bus Controller will transmit data (BC-to-RT). If high, the board will expect to receive data (RT-to-BC).
BIT 14 **Enable RT-RT-** Causes the Controller to initiate an RT - to - RT transfer. The board will copy the data if bit 6 is not set.
BIT 13 **Mode Code w/o Data -** Mode Code without data. Entire message will be a single command word and status response. (Unless Broadcast is selected).
BIT 12 **Broadcast Message -** This message is a broadcast message. Set in addition to message type selected in bits 15,14,13.
BIT 11 **Mode Code with Data -** The message is a mode code with data. Set in addition to the basic message types of bits 14,15.
BIT 10 **Skip CB -** Causes the board to NOT execute the control block (voids the programmable intermessage gap).
BIT 9 **Reserved, set to logic "zero"**
BIT 8 **Reserved, set to logic "zero"**
BIT 7 **Enable Dynamic bus Allocation**
BIT 6 **Enable Conditional Branching**
BIT 5 **Transmit Select :**
0 - A Bus
1 - B Bus
BIT 4 **Enable Scope Sync -** is a pulse of approximately 50 nsec (active low) that occurs approximately 2 μsec before the 1553 command word.
BIT 3 **Inhibit Data Word to Host -** Primarily for RT-to-RT messages, but applicable to RT to BC also.
BIT 2 **Reserved, set to logic "zero"**
BIT 1 **Simulate Receive Status Word**
BIT 0 **Simulate Transmit Status Word**

NOTE

If conflicting bits are set in Control Word 1, A bit will be set in the Programming Error Register, and the VMIVME-6000 will correct the Control Word according to internal priorities.

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Bus Controller/Control Word 2**
Address: **CB Base Address + 0002 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: Bus Controller/Control Word 2 provides enables for the various options of the BC Control Blocks. An option is enabled by setting its corresponding bit in the BC Control Word 2 to a logic "one", and is disabled when the bit is set to a logic "zero". If bit 15 of Control Word 2 is set in a BC Control Block, that particular control block will be the last control block to be executed. After completion of the block, the board will return to OFF mode. If an interrupt on detection of the "STOP" bit is desired, the Host should set bit 9 of the A or B interrupt mask (See A and B Interrupt Masks, Section 4.2.3. Internal ALU Registers). The bit definitions of Control Word 2 are shown below.

BIT 15 **Stop** - The board will stop executing control blocks and return to OFF mode after completing the present block.
BIT 14 **Reserved, set to logic "zero"**
BIT 13 **Reserved, set to logic "zero"**
BIT 12 **EOM Interrupt** - This bit set to "one" enables an end-of-message interrupt.
BITS11-8 **Branch Count** - These bits determine the number conditional branch masks the VMIVME-6000 will test before taking the default link. Appropriate masks and addresses should be programmed in the control block.
BIT 7 **End Of Major Time Frame** - This control block is the last in a major time frame
BIT 6 **End Of Minor Time Frame** - This control block is the last in a minor time frame
BIT 5 **Retry A Bus Only**
BIT 4 **Retry B Bus Only**
BIT 3 **Retry Bus Select (0 = Opposite Bus, 1 = Same Bus)**
BITS2-0 **Auto Retry Count** - Selects the number of retries the board will execute. The board will stop retries when a successful message is transferred or the count decrements to zero. A value of zero disables automatic retries.

Note

All Reserved bits should be set to "zero".

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **LINK (Default Branch)**
Address: **CB Base Address + 0004 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Link (or default branch) is the address in on-board memory where the next Control Block is located. It is programmed by the host during construction of the Control Block, and is read by the board from the third word of the BC Control Block during normal operation. Some applications require the same message be repeatedly transmitted in a list of messages. To simplify the task of having to reproduce the same Control Block multiple times within a chain, the host may use the Bus Controller Pointer Table to link messages. The same message may be repeated by including the Control Block address multiple times in the table.

If the table is enable in the option register, the host must also program the starting address of the table in the BC Pointer Table Orgin along with the length of the table in the BC Pointer Table Length, both which are located in the Internal ALU registers. The VMIVME-6000 will get the link address for the next Control Blocks and the pointer table must be in the same 64 k page of memory.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **DATA MAP**
Address: **CB Base Address + 0006 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The data pointer is the least significant 16-bits, and the map is the most significant 4-bits of address of the memory location from which data is to be received or transmitted from. There are 20-bits of on-board addressing available (only 18-bits are used), with the most significant 4-bits being the same as the most signifcant 4-bits of the Control Block Map programmed in the Internal ALU register.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Address bit 19
BIT 2 Address bit 18
BIT 1 Address bit 17
BIT 0 Address bit 16

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **DATA POINTER**
Address: **CB Base Address + 0008 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The data pointer is the least significant 16-bits, and the map is the most significant 4-bits of address of the memory location from which data is to be received or transmitted from. There are 20-bits of on-board addressing available (only 18-bits are used), with the most significant 4-bits being the same as the most signifcant 4-bits of the Control Block Map programmed in the Internal ALU register.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Response Timout/Data Count**
Address: **CB Base Address + 000A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The six LSB of the upper byte (bits 15 to 8) of this word is the amount of time (in microseconds) the Bus Controller will wait before declaring a response timeout. This is useful where different protocols are used by the same Bus Controller (i.e.,1553A, 1553B etc.). If the value is "zero", the board will default to 14 sec. The time is measured from the middle of the parity bit to the middle of the sync as per MIL-STD-1553B.

The six LSB of the lower byte (bits 7 to 0) of this word configure the actual word count for the message. As an example, if 62 (dec) is loaded in this field, the board will transmit or expect to receive 62-data words. The board checks this word count against the command word and if they don't agree, will set the " Programming Error" bit in the ISR. If a word count error is needed, the number of words that will actually be transmitted should be put into this location.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Timeout bit 5
BIT 12 Timeout bit 4

BIT 11 Timeout bit 3
BIT 10 Timeout bit 2
BIT 9 Timeout bit 1
BIT 8 Timeout bit 0

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Word Count bit 5
BIT 4 Word Count bit 4

BIT 3 Word Count bit 3
BIT 2 Word Count bit 2
BIT 1 Word Count bit 1
BIT 0 Word Count bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Intermessage Gap Time**
Address: **CB Base Address + 000C (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The gap time is the time from the completion of the previous message to the start of the command word for the current Control Block and is specified in microseconds. The default IGAP is 30 µsec. It is measured from the middle of the parity to the middle of the SYNC. Errors detected such as positive and negative word count, bit count, no response, and bus busy will cause the Intermessage Gap for the next message to be invalid. Automatic retries ignore the Intermessage Gap time.

BIT 15 Gap Time bit 15
BIT 14 Gap Time bit 14
BIT 13 Gap Time bit 13
BIT 12 Gap Time bit 12

BIT 11 Gap Time bit 11
BIT 10 Gap Time bit 10
BIT 9 Gap Time bit 9
BIT 8 Gap Time bit 8

BIT 7 Gap Time bit 7
BIT 6 Gap Time bit 6
BIT 5 Gap Time bit 5
BIT 4 Gap Time bit 4

BIT 3 Gap Time bit 3
BIT 2 Gap Time bit 2
BIT 1 Gap Time bit 1
BIT 0 Gap Time bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Interrupt Status Register (ISR)**
Address: **CB Base Address + 0010 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location is where ISR values are posted. The ISR bit descriptions are located in Section 4.2.3. Only nonzero IRSs are posted to the Control Block unless selected in the Option register. Note that Control Blocks that are executed several times before the ISR is checked could have an ISR combination that results from a previous message. Posting of the Status register is programmable through the ISR Mask and Option registers.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Transmission Status Register (TSR)**
Address: **CB Base Address + 0012 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location is where TSR values are posted. The TSR bit descriptions are located in Section 4.2.3. Only nonzero and TSRs are posted to the Control Block unless selected in the Option register. Note that Control Blocks that are executed several times before the TSR is checked could have a TSR combination that resulted from a previous message. Posting of the Status registers is programmable through the ISR Mask and Option registers.

BIT 15 Invalid Message Type
BIT 14 Mode Code Error
BIT 13 Bus Busy
BIT 12 Transmitter Timeout

BIT 11 TA Compare
BIT 10 Instrumentation Bit Error
BIT 9 -Word Count Error
BIT 8 +Word Count Error

BIT 7 Reserved, set to logic "zero"
BIT 6 Gap Error
BIT 5 -Bit Count Error
BIT 4 +Bit Count Error

BIT 3 Response Error
BIT 2 Sync Error
BIT 1 Parity
BIT 0 Manchester Error

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Command Word 1 (CW1)**
Address: **CB Base Address + 0014 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: Command Word 1 (CW1) is the first Command Word transmitted by the Bus Controller regardless of the message format. If the RT-RT bit is set in the Control Word 1, the board will transmit Command Word 2 (CW2) as the second command word (transmit command). The board transmits CW1 and CW2 exactly as they are in on-board memory. The word count, mode code, transmit/receive, and RT-to-RT aspects used by the BC are determined by the control word and data word count locations of the Control Block, and not the Command Words (CW1 and/or CW2).

BIT 15 CW1 bit 15
BIT 14 CW1 bit 14
BIT 13 CW1 bit 13
BIT 12 CW1 bit 12

BIT 11 CW1 bit 11
BIT 10 CW1 bit 10
BIT 9 CW1 bit 9
BIT 8 CW1 bit 8

BIT 7 CW1 bit 7
BIT 6 CW1 bit 6
BIT 5 CW1 bit 5
BIT 4 CW1 bit 4

BIT 3 CW1 bit 3
BIT 2 CW1 bit 2
BIT 1 CW1 bit 1
BIT 0 CW1 bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Status Word 1 (SW1)**
Address: **CB Base Address + 0016 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: Remote Terminal SW1/SW2-The Remote Terminal Status Word response is stored in these locations with Status Word 1 (SW1) corresponding to CW1 and Status Word 2 (SW2) corresponding to CW2 (transmit RT in an RT-RT message). The status words are stored exactly as they are received from the 1553 bus. If there is no response from the RT, nothing will be posted to these locations.

Bus Controller Simulation of SW1/SW2- When the board is simulating a Remote Terminal Status Response While also acting as the Bus Controller, the status word to be transmitted in response to a CW1 should be loaded into SW1 location of the control block. The simulated status word for CW2 should be loaded into the SW2 location. Enabling of either, or both, of the status response is done in CW1 of the control block. Note that either, or both, of the status responses in an RT-RT message may be simulated by the board. The data to be transmitted/received as part of the status response will be located at the address given by the control block data pointer and map locations.

BIT 15	**SW1 bit 15**	**BIT 7**	**SW1 bit 7**
BIT 14	**SW1 bit 14**	**BIT 6**	**SW1 bit 6**
BIT 13	**SW1 bit 13**	**BIT 5**	**SW1 bit 5**
BIT 12	**SW1 bit 12**	**BIT 4**	**SW1 bit 4**
BIT 11	**SW1 bit 11**	**BIT 3**	**SW1 bit 3**
BIT 10	**SW1 bit 10**	**BIT 2**	**SW1 bit 2**
BIT 9	**SW1 bit 9**	**BIT 1**	**SW1 bit 1**
BIT 8	**SW1 bit 8**	**BIT 0**	**SW1 bit 0**

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Command Word 2 (CW2)**
Address: **CB Address + 0018 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: If the RT-RT bit is set in the Control Word 1, the board will transmit Command Word 2 (CW2) as the second command word (transmit command). The board transmits CW1 and CW2 exactly as they are in on-board memory. The word count, mode code, transmit/receive, and RT-to-RT aspects used by the BC are determined by the control word and data word count locations of the Control Block, and not the Command Words (CW1 and/or CW2).

BIT 15 CW2 bit 15
BIT 14 CW2 bit 14
BIT 13 CW2 bit 13
BIT 12 CW2 bit 12

BIT 11 CW2 bit 11
BIT 10 CW2 bit 10
BIT 9 CW2 bit 9
BIT 8 CW2 bit 8

BIT 7 CW2 bit 7
BIT 6 CW2 bit 6
BIT 5 CW2 bit 5
BIT 4 CW2 bit 4

BIT 3 CW2 bit 3
BIT 2 CW2 bit 2
BIT 1 CW2 bit 1
BIT 0 CW2 bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Status Word 2 (SW2)**
Address: **CB Base Address + 001A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: Remote Terminal SW1/SW2-The Remote Terminal Status Word response is stored in these locations with Status Word 1 (SW1) corresponding to CW1 and Sataus Word 2 (SW2) corresponding to CW2 (transmit RT in an RT-RT message). The status words are stored exactly as they are received from the 1553 bus. If there is no response from the RT, nothing will be posted to these locations.

Bus Controller Simulation of SW1/SW2- When the board is simulating a Remote Terminal Status Response While also acting as the Bus Controller, the status word to be transmitted in response to a CW1 should be loaded into SW1 location of the control block. The simulated status word for CW2 should be loaded into the SW2 location. Enabling of either, or both, of the status response is done in control work 1 of the control block. Note that either, or both, of the status responses in an RT-RT message may be simulated by the board. The data to be transmitted/received as part of the status response will be located at the address given by the control block data pointer and map locations.

BIT 15	**SW2 bit 15**	**BIT 7**	**SW2 bit 7**
BIT 14	**SW2 bit 14**	**BIT 6**	**SW2 bit 6**
BIT 13	**SW2 bit 13**	**BIT 5**	**SW2 bit 5**
BIT 12	**SW2 bit 12**	**BIT 4**	**SW2 bit 4**
BIT 11	**SW2 bit 11**	**BIT 3**	**SW2 bit 3**
BIT 10	**SW2 bit 10**	**BIT 2**	**SW2 bit 2**
BIT 9	**SW2 bit 9**	**BIT 1**	**SW2 bit 1**
BIT 8	**SW2 bit 8**	**BIT 0**	**SW2 bit 0**

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Response Time SW1/SW2**
Address: **CB Base Address + 001C (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The upper byte (bits 15 to 8) of this word contains the response time of the SW2 (transmit status word in an RT-RT transfer). The lower byte (bits 7 to 0) contains the response time of SW1. If the SW1 and/or SW2 responses are being simulated by the Bus Controller, the host should program the needed response time of the simulated status responses in the SW1 and/or SW2 response time bytes. Response time is measured from mid parity to mid SYNC. The default simulator response times shall be 4 μsec. Any programmed response time should be 5 μsec or greater.

BIT 15 SW2 Response bit 15
BIT 14 SW2 Response bit 14
BIT 13 SW2 Response bit 13
BIT 12 SW2 Response bit 12

BIT 11 SW2 Response bit 11
BIT 10 SW2 Response bit 10
BIT 9 SW2 Response bit 9
BIT 8 SW2 Response bit 8

BIT 7 SW2 Response bit 7
BIT 6 SW2 Response bit 6
BIT 5 SW2 Response bit 5
BIT 4 SW2 Response bit 4

BIT 3 SW2 Response bit 3
BIT 2 SW2 Response bit 2
BIT 1 SW2 Response bit 1
BIT 0 SW2 Response bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Status Word 1 (SW1) Interrupt Mask**
Address: **CB Base Address + 001E (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The board provides a means of interrupting based on the received 1553 SW. Any bit positions in the mask that are set to a logic "one" and correspond to a bit set in the SW will cause an interrupt (if interrupts are enable).

BIT 15 SW1 bit 15
BIT 14 SW1 bit 14
BIT 13 SW1 bit 13
BIT 12 SW1 bit 12

BIT 11 SW1 bit 11
BIT 10 SW1 bit 10
BIT 9 SW1 bit 9
BIT 8 SW1 bit 8

BIT 7 SW1 bit 7
BIT 6 SW1 bit 6
BIT 5 SW1 bit 5
BIT 4 SW1 bit 4

BIT 3 SW1 bit 3
BIT 2 SW1 bit 2
BIT 1 SW1 bit 1
BIT 0 SW1 bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: Status Word 2 (SW2) Interrupt Mask
Address: CB Base Address + 0020 (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: The board provides a means of interrupting based on the received 1553 SW. Any bit positions in the mask that are set to a logic "one" and correspond to a bit set in the SW will cause an interrupt (if interrupts are enable).

BIT 15 SW2 bit 15
BIT 14 SW2 bit 14
BIT 13 SW2 bit 13
BIT 12 SW2 bit 12

BIT 11 SW2 bit 11
BIT 10 SW2 bit 10
BIT 9 SW2 bit 9
BIT 8 SW2 bit 8

BIT 7 SW2 bit 7
BIT 6 SW2 bit 6
BIT 5 SW2 bit 5
BIT 4 SW2 bit 4

BIT 3 SW2 bit 3
BIT 2 SW2 bit 2
BIT 1 SW2 bit 1
BIT 0 SW2 bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: "A" Interrupt Mask
Address: CB Base Address + 0022 (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: The A and B Interrupt Mask are a mirror image of the ISR. At the end of each message each mask is logically "ANDed" to the ISR and, if a match occurs, an interrupt is executed. The hardware interrupt may be enabled/disabled in the Control register. (See Hardware XIO Registers, Section 4.2.2.1)

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **"B" Interrupt Mask**
Address: **CB Base Address + 0024 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The A and B Interrupt Mask are a mirror image of the ISR. At the end of each message each mask is logically "ANDed" to the ISR and, if a match occurs, an interrupt is executed. The hardware interrupt may be enabled/disabled in the Control Register. (See Hardware XIO Registers, Section 4.2.2.1)

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Error Generation Select**
Address: **CB Base Address + 0026 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location selects the type of error (if any) the BC will generate on the message defined by the Control Block. A detailed discussion of error generation is included in Section 4.6.

BIT 15 MANCHESTER - The particular bit time is programmable.
BIT 14 PARITY
BIT 13 SYNC
BIT 12 BIT COUNT ERROR - Word length programmable in Frame Register.
BIT 11 RESERVED
BIT 10 +WORD COUNT
BIT 9 - WORD COUNT
BIT 8 RESPOND ON WRONG BUS
BIT 7 GAP BETWEEN DATA WORDS
BIT 6 RESERVED
BIT 5 RESERVED
BIT 4 RESERVED
BIT 3 ERROR IN SW1
BIT 2 ERROR IN SW2
BIT 1 ERROR IN CW1
BIT 0 ERROR IN CW2

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Error Word Select 1-16**
Address: **CB Base Address + 0028 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The two error word select locations define the particular data word (s) where the error will be generated. See Section 4.6 for complete details on error generation.

BIT 15 Data Word 16
BIT 14 Data Word 15
BIT 13 Data Word 14
BIT 12 Data Word 13

BIT 11 Data Word 12
BIT 10 Data Word 11
BIT 9 Data Word 10
BIT 8 Data Word 9

BIT 7 Data Word 8
BIT 6 Data Word 7
BIT 5 Data Word 6
BIT 4 Data Word 5

BIT 3 Data Word 4
BIT 2 Data Word 3
BIT 1 Data Word 2
BIT 0 Data Word 1

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Error Word Select 17- 32**
Address: **CB Base Address + 002A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The two error word select locations define the particular data word(s) where the error will be generated. See Section 4.6 for complete details on error generation.

BIT 15 Data Word 32
BIT 14 Data Word 31
BIT 13 Data Word 30
BIT 12 Data Word 29

BIT 11 Data Word 28
BIT 10 Data Word 27
BIT 9 Data Word 26
BIT 8 Data Word 25

BIT 7 Data Word 24
BIT 6 Data Word 23
BIT 5 Data Word 22
BIT 4 Data Word 21

BIT 3 Data Word 20
BIT 2 Data Word 19
BIT 1 Data Word 18
BIT 0 Data Word 17

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Auto Retry TSR Mask**
Address: **CB Base Address + 002C (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location is programmed by the host if Automatic Retry is needed. Corresponding bits set in the Auto Retry TSR Mask and the TSR will cause an automatic retry to be executed based on the retry parameters set in the BC Control Word 2.

BIT 15 Invalid Message Type
BIT 14 Mode Code Error
BIT 13 Bus Busy
BIT 12 Transmitter Timeout

BIT 11 TA Compare
BIT 10 Instrumentation Bit Error
BIT 9 -Word Count Error
BIT 8 +Word Count Error

BIT 7 Reserved, set to logic "zero"
BIT 6 Gap Error
BIT 5 -Bit Count Error
BIT 4 +Bit Count Error

BIT 3 Response Error
BIT 2 Sync Error
BIT 1 Parity
BIT 0 Manchester Error

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Auto Retry Status Word Mask**
Address: **CB Base Address + 002E (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location is programmed by the host if Automatic Retry is needed. Corresponding bits set in the Auto Retry SW Mask and the received 1553 SW will cause an automatic retry to be executed based on the retry parameters set in the BC Control Word 2.

BIT 15 SW bit 15
BIT 14 SW bit 14
BIT 13 SW bit 13
BIT 12 SW bit 12

BIT 11 SW bit 11
BIT 10 SW bit 10
BIT 9 SW bit 9
BIT 8 SW bit 8

BIT 7 SW bit 7
BIT 6 SW bit 6
BIT 5 SW bit 5
BIT 4 SW bit 4

BIT 3 SW bit 3
BIT 2 SW bit 2
BIT 1 SW bit 1
BIT 0 SW bit 0

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Branch Mask 1 thur 15**
Address: **CB Base Address + 0038 (Hex), 003C, ... , 0070**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The remaining 30 locations of the BC Control Block are used for programmable branching. The locations contain 15 Branch Masks and Branch Addresses. Branching is enabled by programming a branch count in Control Word 2, and setting bit 6 of Control Word 1. Programmable branching is described in detail at the beginning of Section 4.3.2 under the heading "Branch Programming".

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

SIMULATOR (BC) MODE
BUS CONTROLLER CONTROL BLOCK

Name: **Branch Address 1 thur 15**
Address: **CB Base Address 003A (Hex), 003E, ... , 0072**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The remaining 30 locations of the BC Control Block are used for programmable branching. The locations contain 15 Branch Masks and Branch Addresses. Branching is enabled by programming a branch count in Control Word 2, and setting bit 6 of Control Word 1. Programmable branching is described in detail at the beginning of Section 4.3.2 under the heading "Branch Programming".

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

4.3.3 Multiple Remote Terminal (MRT)/Monitor Mode

In MRT/Monitor mode, the VMIVME-6000 will simulate and/or monitor up to 32-remote terminals. The board can simulate selected RTs while monitoring messages addressed to other RTs, and is capable of handling the 1553B, 1553A, F-16, and F-18 protocols. It can be programmed to be compliant with any of the four protocols with any combination of simulated and/or monitored RTs. The VMIVME-6000 can simulate intermixed protocols with some RTs simulating 1553B and other RTs simulating any of the other three protocols.

The VMIVME-6000 is capable of generating word selected errors at the RT level. It will also detect and report errors in the ISR and TSR for each message. Two levels of Interrupt, (A and B), are available for each RT whether it is being simulated or monitored.

4.3.3.1 Multiple Remote Terminal (MRT)

Multiple Remote Terminal (MRT) mode is the mode in which the VMIVME-6000 actually simulates an RT(s). It will transmit or receive data and provide the status response. It is capable of handling all 10 defined 1553B message formats.

The VMIVME-6000 can simulate both or either RT in an RT-to-RT transfer. It can also simulate one RT and monitor the other, and the VMIVME-6000 can do all combinations involving an RT-to-RT broadcast.

In MRT Mode, there are 64-subaddress blocks (32-receive, 32-transmit). Each subaddress (SA) block has a data pointer that points to the location in memory where data will be transmitted to or from. While each RT can have a different map for its data buffers, all data buffers for a particular RT must be within the same map block.

4.3.3.2 Monitor (Mon)

Monitor Mode is a pure record mode. It records all 1553 bus traffic and stores it in a ring buffer structure. Monitor options are at the RT Address and Subaddress level. Options in this mode include Stop/Start Record, programmable ring buffer position and length, 32-bit time tag, interrupts, and illegalization of selected commands.

Monitor Mode "monitors" the 1553 bus and stores the host selected information in the same data buffer format as the MRT Mode. The MRT/MON Mode is capable of handling all ten defined message formats including broadcast and mode codes.

4.3.3.3 MRT/Monitor Setup

Before operating as a Remote Terminal (s) or Monitor, the VMIVME-6000 must be properly initialized. This requires that the Header Block, RT Control Blocks, and Subaddress Blocks be constructed in on-board memory, and the board be started by an XIO Start Command. The following paragraphs describe in detail the initialization procedure and control block structures.

NOTE

MONITOR SHOULD BE STARTED BEFORE ANY BUS ACTIVITY SO THE VMIVME-6000 WILL BE ON-LINE WHEN THE FIRST ACTIVITY DOES OCCUR. IF THE BOARD (AS MONITOR) IS STARTED DURING BUS ACTIVITY, SOME CONSIDERATION SHOULD BE GIVEN TO THE POSSIBILITY OF THE VMIVME-6000 COMING ON-LINE IN THE MIDDLE OF AN ON-GOING MESSAGE AND THEN TREATING THE STATUS RESPONSE AS A COMMAND WORD.

4.3.3.4 Initialization

The VMIVME-6000 keeps all the information about the 32 RTs in MRT/MON RAM. The information stored in the RAM is unchanged by the VMIVME-6000 until the power is turned off or a CLEAR operation command is executed. The VMIVME-6000 must be initialized at least once for MRT/MON mode before it can perform properly. A CLEAR operation command should be executed after power-up regardless of the mode. The VMIVME-6000 treats all unwritten locations (zeroes) of the MRT/MON RAM as default to some predefined value.

In some applications, the host may wish to change some of the data which was loaded into the MRT/MON RAM by the VMIVME-6000 during initialization. Using the Special Function XIO Commands to access the MRT/MON RAM, the host may selectively enable or disable simulation, monitoring, and many other options of Remote Terminals while the board is Active. The MRT/MON RAM is discussed in detail in Section 4.4.

4.3.3.5 Quick Start MRT/MON

This is the quickest method of entering into MRT/MON MODE. It does not re-initialize the MRT/MON RAM. When the VMIVME-6000 is started, it skips over the RAM initialization and immediately enters into the routine for checking 1553 bus traffic. This method should ONLY be used AFTER the first initialization, when a re-entry into MRT/MON is desired.

4.3.3.6 MRT/MON Control Blocks

MRT/MON mode of the VMIVME-6000 is based on a flexible control block structure that, along with host-programmed XIO registers, allows the board to simulate/monitor an entire 1553 bus system. A high-level diagram of the MRT/MON control block structure is shown below.

Table 4.3.3.6-1. MRT/MON Control Block Structure

Byte Address	
0 : 20	MRT/MON Header Block
22 : 42	RT Control Block 1
44	RT 1 Receive Subaddress Block 0
:	:
FE	RT 1 Receive Subaddress Block 31
104	RT 1 Transmit Subaddress Block 0
:	:
1C4	RT 1 Transmit Subaddress Block 31

RT Control Block N
RT N Receive Subaddress Block 0
:
RT N Receive Subaddress Block 31
RT N Transmit Subaddress Block 0
:
RT N Transmit Subaddress Block 31

4.3.3.6.1 MRT/MON Header

When operating in MRT/MON MODE, one MRT/MON header is required. It must be the first 17 (dec) word locations in the control block list, and the master control word of the header must be located at the address pointed to by the Control Block Address and Control Block Map registers. The header locations with "MASTER" as a descriptor have information that is logically "ORed" to all RT Control Blocks to formulate the final selections. This allows the host to "globally" select an option or parameter for all RTs. For example, if a bit is set in the "MASTER A INT MASK", that bit will be set in all the RTs (simulated and monitored) A INT masks.

Table 4.3.3.6.1-1. MRT/MON Header Control Block

Byte Address	
0	Master Control Word
2	RT Count
4	Not Used
6	Master Error Generation Selects
8	Master Error GEN Words 16 - 1
A	Master Error GEN Words 32 - 17
C	Not Used
E	Ring Buffer Begin Pointer
10	Ring Buffer End Pointer
12	Ring Buffer Begin Map
14	Ring Buffer End Map
16	Master A Interrupt Mask
18	Master B Interrupt Mask
1A	Master DMA Disable Register
1C	Master Mode Code Enables 15 - 0
1E	Master Mode Code Enables 31 - 16
20	Not Used

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **MRT/MON Master Control Word**
Address: **CB Base Address + 0000 (Hex)**
Address Space: **XIO**
Type: **Read/Write**

Description: The "Master Control Word" and the individual RT Control Words are not identical. The bits that are the same are "ORed" to formulate the final RT Control Word. If the RTs have different characteristics and options from other RTs then the bits of the "Master Words" controlling those characteristics and options should be left "zero", and the characteristics or options should be selected in the individual RT Control Words. The Master Control Word format is shown below.

BITS 15-14 Bits 15 and 14 eliminate the respective subaddress (0 and 31) from being declared as a mode code. Once a subaddress is disabled, it becomes a normal valid subaddress like all other subaddress.

BIT 13 **A Bus Disable** - totally disables A bus

BIT 12 **B Bus Disable** - totally disables B bus

BIT 11 **Switchover Disable** - Don't do bus switchover at all. This bit may be set to logic "one" to eliminate possibility of bus switchover occurring. Conditions that possibly would warrant disabling bus switchover would be monitor, or simulating a specification that does not provide for bus switchover.

BIT 10 **Broadcast Enable** - An RT control Block with TA=31 and bit 9 set must be provided.

BITS9-8 **Rt Simulate Master/Rt Monitor Master-** The VMIVME-6000 distinguishes simulated RTs from monitored RTs via bits 9 and 8 of the control words. Bit 9 should be set if the RT is to be simulated and bit 8 if the RT is to be monitored. If bit 9 or 8 is not set, then "programming Error" will be set, and the RT will be ignored.

BIT 7 **Reserved, set to logic "zero"**

BIT 6 **Broadcast Mode Code Processing Disable** - The board will NOT execute a Broadcast Mode Code. The Broadcast Received bit will still be set.

BITS5-2 **Reserved, set to logic "zero"**

BIT 1 **F18-1553A** - Obey protocol of 1553A and F18 (refer to respective specifications for more details).

BIT 0 **F16** - Follow the protocol and configure the status word based on F16.

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **RT Count**
Address: **CB Base Address + 0002 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The 6 LSB tell the VMIVME-6000 how many RT Control Blocks there are for initialization (must include the broadcast control blocks also). An RT count of "zero" will cause "Programming Error to be set in the ASR, and the board to be inoperable unless the "32 RT initialization" bit is set in the Option Register.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 RT Count bit 5
BIT 4 RT Count bit 4

BIT 3 RT Count bit 3
BIT 2 RT Count bit 2
BIT 1 RT Count bit 1
BIT 0 RT Count bit 0

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Master Error Generation Select**
Address: **CB Base Address + 0006 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Error Generation Selects are described in Section 4.6. All the errors selected in the "Master Error Generation Selects" are selected for all RTs. The same is true for the "Master Generation Words". They are discussed in Section 4.6.

BIT 15 MANCHESTER - The particular bit time is programmable.

BIT 14 PARITY

BIT 13 SYNC

BIT 12 BIT COUNT ERROR - Word length programmable in Frame Register.

BIT 11 TA ERROR - Will force an erroneous +1 TA into status word.

BIT 10 + WORD COUNT

BIT 9 - WORD COUNT

BIT 8 RESPOND ON WRONG BUS

BIT 7 GAP BETWEEN DATA WORDS

BIT 6 RESERVED

BIT 5 RESERVED

BIT 4 RESERVED

BIT 3 ERROR IN SW1

BIT 2 RESERVED

BIT 1 RESERVED

BIT 0 RESERVED

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: Master Error Generation Word 1-16
Address: CB Base Address + 0008 (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: The Error Generation Selects are described in Section 4.6. All the errors selected in the "Master Error Generation Selects" are selected for all RTs. The same is true for the "Master Generation Words." They are discussed in Section 4.6.

BIT 15 Data Word 16
BIT 14 Data Word 15
BIT 13 Data Word 14
BIT 12 Data Word 13

BIT 11 Data Word 12
BIT 10 Data Word 11
BIT 9 Data Word 10
BIT 8 Data Word 9

BIT 7 Data Word 8
BIT 6 Data Word 7
BIT 5 Data Word 6
BIT 4 Data Word 5

BIT 3 Data Word 4
BIT 2 Data Word 3
BIT 1 Data Word 2
BIT 0 Data Word 1

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Master Error generation Word 17- 32**
Address: **CB Base Address + 000A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Error Generation Selects are described in Section 4.6. All the errors selected in the "Master Error Generation Selects" are selected for all RTs. The same is true for the "Master Generation Words." They are discussed in Section 4.6.

BIT 15 Data Word 32
BIT 14 Data Word 31
BIT 13 Data Word 30
BIT 12 Data Word 29

BIT 11 Data Word 28
BIT 10 Data Word 27
BIT 9 Data Word 26
BIT 8 Data Word 25

BIT 7 Data Word 24
BIT 6 Data Word 23
BIT 5 Data Word 22
BIT 4 Data Word 21

BIT 3 Data Word 20
BIT 2 Data Word 19
BIT 1 Data Word 18
BIT 0 Data Word 17

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Ring Buffer Begin Pointer**
Address: **CB Base Address + 000E (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Ring Buffer Begin/End Pointer and maps are used for determining the starting and ending addresses of the Monitor Ring Buffer. These locations are only used when the board is in Monitor mode.

BIT 15 Begin Address bit 15
BIT 14 Begin Address bit 14
BIT 13 Begin Address bit 13
BIT 12 Begin Address bit 12

BIT 11 Begin Address bit 11
BIT 10 Begin Address bit 10
BIT 9 Begin Address bit 9
BIT 8 Begin Address bit 8

BIT 7 Begin Address bit 7
BIT 6 Begin Address bit 6
BIT 5 Begin Address bit 5
BIT 4 Begin Address bit 4

BIT 3 Begin Address bit 3
BIT 2 Begin Address bit 2
BIT 1 Begin Address bit 1
BIT 0 Begin Address bit 0

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Ring Buffer End Pointer**
Address: **CB Base Address + 0010 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Ring Buffer Begin/End Pointer and maps are used for determining the starting and ending addresses of the Monitor Ring Buffer. These locations are only used when the board is in Monitor mode.

BIT 15 End Address bit 15
BIT 14 End Address bit 14
BIT 13 End Address bit 13
BIT 12 End Address bit 12

BIT 11 End Address bit 11
BIT 10 End Address bit 10
BIT 9 End Address bit 9
BIT 8 End Address bit 8

BIT 7 End Address bit 7
BIT 6 End Address bit 6
BIT 5 End Address bit 5
BIT 4 End Address bit 4

BIT 3 End Address bit 3
BIT 2 End Address bit 2
BIT 1 End Address bit 1
BIT 0 End Address bit 0

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Ring Buffer Begin Map**
Address: **CB Base Address + 0012 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Ring Buffer Begin/End Pointer and Maps are used for determining the starting and ending addresses of the Monitor Ring Buffer. These locations are only used when the board is in Monitor mode.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Begin Address bit 19
BIT 2 Begin Address bit 18
BIT 1 Begin Address bit 17
BIT 0 Begin Address bit 16

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Ring Buffer End Map**
Address: **CB Base Address + 0014 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Ring Buffer Begin/End Pointer and maps are used for determining the starting and ending addresses of the Monitor Ring Buffer. These locations are only used when the board is in Monitor mode.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 End Address bit 19
BIT 2 End Address bit 18
BIT 1 End Address bit 17
BIT 0 End Address bit 16

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: Master A Interrupt Mask
Address: CB Base Address + 0016 (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: The Master A and B Interrupt Masks are logically "ORed" to each individual RT interrupt mask so that any bit selected in the MRT header is selected for all the RTs.This mask is compared to the ISR of each simulated or monitored RT. If corresponding bits are set in the mask and the ISR, an interrupt will be generated by the firmware.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Master B Interrupt Mask**
Address: **CB Base Address + 0018 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Master A and B Interrupt Masks are logically "ORed" to each individual RT interrupt mask so that any bit selected in the MRT header is selected for all the RTs.This mask is compared to the ISR of each simulated or monitored RT. If corresponding bits are set in the mask and the ISR, an interrupt will be generated by the firmware.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: **Master DMA Disable Register**
Address: **CB Base Address + 001A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location of the Header Control Block will disable DMAs for all simulated and/or monitored RTs as shown below.

BIT 15 Reserved, set to logic "zero"
BIT 14 Gap Time - Measured intermessage gap in MRT/MON, selected intermessage gap in BC.
BIT 13 LS Time Tag - MRT/MON mode
BIT 12 MS Time Tag - MRT/MON mode

BIT 11 Auto Retry TSR Mask - BC mode
BIT 10 Auto Retry ISR Mask - BC mode
BIT 9 A Interrupt Mask - BC mode
BIT 8 B Interrupt Mask - BC mode

BIT 7 Response Time - BC, MON mode
BIT 6 Status Word 2 - BC, MON mode
BIT 5 Status Word 1 - BC, MON mode
BIT 4 New Data Pointer - MRT mode

BIT 3 Status Word 2 Mask - BC mode
BIT 2 Status Word 1 Mask - BC mode
BIT 1 Error Word Selects - BC mode
BIT 0 Error Generation - BC mode

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: Master Mode Code Enables 15-0
Address: CB Base Address + (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: This location in the Master RT Control Block is used to enable particular Mode Codes for all simulated RTs.

BIT 15 Mode Code 15
BIT 14 Mode Code 14
BIT 13 Mode Code 13
BIT 12 Mode Code 12

BIT 11 Mode Code 11
BIT 10 Mode Code 10
BIT 9 Mode Code 9
BIT 8 Mode Code 8

BIT 7 Mode Code 7
BIT 6 Mode Code 6
BIT 5 Mode Code 5
BIT 4 Mode Code 4

BIT 3 Mode Code 3
BIT 2 Mode Code 2
BIT 1 Mode Code 1
BIT 0 Mode Code 0

MRT/MON MODE
MRT/MON HEADER BLOCK

Name: Master Mode Code Enables 31- 16
Address: CB Base Address + (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: This location in the Master RT Control Block is used to enable particular Mode Codes for all simulated RTs.

BIT 15 Mode Code 31
BIT 14 Mode Code 30
BIT 13 Mode Code 29
BIT 12 Mode Code 28

BIT 11 Mode Code 27
BIT 10 Mode Code 26
BIT 9 Mode Code 25
BIT 8 Mode Code 24

BIT 7 Mode Code 23
BIT 6 Mode Code 22
BIT 5 Mode Code 21
BIT 4 Mode Code 20

BIT 3 Mode Code 19
BIT 2 Mode Code 18
BIT 1 Mode Code 17
BIT 0 Mode Code 16

4.3.3.6.2 RT Control Blocks

The individual RT Control Blocks (CB's) allow the host to program different parameters or options for each RT being simulated or monitored. There must be one RT Control Block for each RT simulated or monitored, unless bit 8 of the Option Register is set to a logic "one". (In that case, the VMIVME-6000 will use one set of RT/SA blocks, and configure all 32-RTs using the information from that block.). The information in each RT CB applies to the RT with the TA specified in the second word. The RT Control Blocks do not have to be in any particular order. There can be any combination of terminal addresses, monitored, and simulated RTs. The entire MRT/MON Control Block structure must be contiguous. The RT Control Block format is shown in Table 4.3.3.6.2-1.

NOTE

THERE MUST BE ONE (1) OF THESE RT CONTROL BLOCKS FOR EACH RT SIMULATED OR MONITORED. THEY MUST BE CONTIGUOUS, ALONG WITH THEIR SUBADDRESS CONTROL BLOCKS.

Table 4.3.3.6.2-1. MRT/MON RT Control Block

Byte Address	
0	Control Word
2	Terminal Address
4	Status Word Skeleton
6	Error Generation Selects
8	Error Generation Words 16 -1
A	Error Generation Words 32 - 17
C	Not Used
E	Data Map
10	Not Used
12	Not Used
14	Not Used
16	A Interrupt Mask
18	B Interrupt Mask
1A	DMA Disable Register
1C	Mode Code Enables 15 - 0
1E	Mode Code Enables 31 - 16
20	Not Used

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Control Block**
Address: **CB Base Address + 0000 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The bit location's of the control word, which are defined in the MRT/MON Header Block, are used in the same manner in the RT Control Blocks, with the exception that the RT Control Word is applicable only to the RT with a corresponding Terminal Address (TA).

BITS 15-14 Bits 15 and 14 eliminate the respective subaddress (0 and 31) from being declared as a mode code. Once a subaddress is disabled, it becomes a normal valid subaddress like all other subaddress.

BIT 13 **A Bus Disable** - totally disables A bus

BIT 12 **B Bus Disable** - totally disables B bus

BIT 11 **Switchover Disable** - Don't do bus switchover at all. This bit may be set to logic "one" to eliminate possibility of bus switchover occurring. Conditions that possibly would warrant disabling bus switchover would be monitor, or simulating a specification that does not provide for bus switchover.

BIT 10 **Broadcast Enable** - An RT control Block with TA=31 and bit 9 set must be provided.

BITS 9-8 **Rt Simulate Master/Rt Monitor Master-** The VMIVME-6000 distinguishes simulated RTs from monitored RTs via bits 9 and 8 of the control words. Bit 9 should be set if the RT is to be simulated and bit 8 if the RT is to be monitored. If bit 9 or 8 is not set, then "programming Error" will be set, and the RT will be ignored.

BIT 7 **Reserved, set to logic "zero"**

BIT 6 **Broadcast Mode Code Processing Disable** - The board will NOT execute a Broadcast Mode Code. The Broadcast Received bit will still be set.

BITS 5-2 **Reserved, set to logic "zero"**

BIT 1 **F18-1553A** - Obey protocol of 1553A and F18 (refer to respective specifications for more details).

BIT 0 **F16** - Follow the protocol and configure the status word based on F16.

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Terminal Address (TA)**
Address: **CB Base Address + 0002 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The 5-LSB's of this location should be programmed by the host to determine each RT's terminal address the upper 11-bits are unused and should be set to "zero".

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 TA bit 4

BIT 3 TA bit 3
BIT 2 TA bit 2
BIT 1 TA bit 1
BIT 0 TA bit 0

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: RT Status Word Skeleton
Address: CB Base Address + 0004 (Hex)
Address Space: VMEbus Standard Address Space
Type: Read/Write

Description: The 11-LSB's of the Status Word Skeleton are used to create the status word for the response by this RT. It may be dynamically changed.

BIT 15 Reserved, set to "zero"
BIT 14 Reserved, set to "zero"
BIT 13 Reserved, set to "zero"
BIT 12 Reserved, set to "zero"

BIT 11 Reserved, set to "zero"
BIT 10 SW bit 10
BIT 9 SW bit 9
BIT 8 SW bit 8

BIT 7 SW bit 7
BIT 6 SW bit 6
BIT 5 SW bit 5
BIT 4 SW bit 4

BIT 3 SW bit 3
BIT 2 SW bit 2
BIT 1 SW bit 1
BIT 0 SW bit 0

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Error Generation Selects**
Address: **CB Base Address + 0006 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: Error Generation is described in Section 4.6. These particular selects apply only to this RT and are logically "ORed" to the MRT/MON Header Selects for the final Error Generation Selects for this RT.

BIT 15 MANCHESTER - The particular bit time is programmable.

BIT 14 PARITY

BIT 13 SYNC

BIT 12 BIT COUNT ERROR - Word length programmable in Frame Register.

BIT 11 TA ERROR - Will force an erroneous +1 TA into status word.

BIT 10 + WORD COUNT

BIT 9 - WORD COUNT

BIT 8 RESPOND ON WRONG BUS

BIT 7 GAP BETWEEN DATA WORDS

BIT 6 RESERVED

BIT 5 RESERVED

BIT 4 RESERVED

BIT 3 ERROR IN SW1

BIT 2 RESERVED

BIT 1 RESERVED

BIT 0 RESERVED

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Error Generation Words 16-1**
Address: **CB Base Address + 0008 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Error Generation Words define the particular words in which errors will be generated. These are at the RT level and are described in Section 4.6

BIT 15 Data Word 16
BIT 14 Data Word 15
BIT 13 Data Word 14
BIT 12 Data Word 13

BIT 11 Data Word 12
BIT 10 Data Word 11
BIT 9 Data Word 10
BIT 8 Data Word 9

BIT 7 Data Word 8
BIT 6 Data Word 7
BIT 5 Data Word 6
BIT 4 Data Word 5

BIT 3 Data Word 4
BIT 2 Data Word 3
BIT 1 Data Word 2
BIT 0 Data Word 1

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Error Generation Words 32-17**
Address: **CB Base Address + 000A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The Error Generation Words define the particular words in which errors will be generated. These are at the RT level and are described in Section 4.6

BIT 15 Data Word 32
BIT 14 Data Word 31
BIT 13 Data Word 30
BIT 12 Data Word 29

BIT 11 Data Word 28
BIT 10 Data Word 27
BIT 9 Data Word 26
BIT 8 Data Word 25

BIT 7 Data Word 24
BIT 6 Data Word 23
BIT 5 Data Word 22
BIT 4 Data Word 21

BIT 3 Data Word 20
BIT 2 Data Word 19
BIT 1 Data Word 18
BIT 0 Data Word 17

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Data Buffer Map**
Address: **CB Base Address + 000E (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The data map applies to all the subaddress data pointers within a single RT Control Block List. It provides 4-bits of mapping and gives the VMIVME-6000 20-bits of addressing. All data buffers for a particular RT must be in the same 64 kbytes of memory.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Reserved, set to logic "zero"
BIT 9 Reserved, set to logic "zero"
BIT 8 Reserved, set to logic "zero"

BIT 7 Reserved, set to logic "zero"
BIT 6 Reserved, set to logic "zero"
BIT 5 Reserved, set to logic "zero"
BIT 4 Reserved, set to logic "zero"

BIT 3 Map Bit 3
BIT 2 Map Bit 2
BIT 1 Map Bit 1
BIT 0 Map Bit 0

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **"A" Interrupt Mask**
Address: **CB Base Address + 0016 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The A and B Interrupt Masks are applicable at the RT level and are "ORed" to the MRT/MON Header masks to configure the final masks. Section 4.5 describe the Interrupt Masks.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **"B" Interrupt Mask**
Address: **CB Base Address + 0018 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The A and B Interrupt Masks are applicable at the RT level and are "ORed" to the MRT/MON Header masks to configure the final masks. Section 4.5 describe the interrupt Masks.

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **DMA Disable Registers**
Address: **CB Base Address + 001A (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location of the RT Control Block will disable DMA for the simulated and/or monitored RT as shown below.

BIT 15 **Reserved, set to logic "zero"**
BIT 14 **Gap Time -** Measured intermessage gap in MRT/MON, selected intermessage gap in BC.
BIT 13 **LS Time Tag -** MRT/MON mode
BIT 12 **MS Time Tag -** MRT/MON mode

BIT 11 **Auto Retry TSR Mask -** BC mode
BIT 10 **Auto Retry ISR Mask -** BC mode
BIT 9 **A Interrupt Mask -** BC mode
BIT 8 **B Interrupt Mask -** BC mode

BIT 7 **Response Time -** BC, MON mode
BIT 6 **Status Word 2 -** BC,MON mode
BIT 5 **Status Word 1 -** BC,MON mode
BIT 4 **New Data Pointer -** MRT mode

BIT 3 **Status Word 2 Mask -** BC mode
BIT 2 **Status Word 1 Mask -** BC mode
BIT 1 **Error Word Selects -** BC mode
BIT 0 **Error Generation -** BC mode

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Mode Code Enables 15-0**
Address: **CB Base Address + 001C (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location in the RT Control Block is used to enable particular Mode Codes at the RT level.

BIT 15 Mode Code 15
BIT 14 Mode Code 14
BIT 13 Mode Code 13
BIT 12 Mode Code 12

BIT 11 Mode Code 11
BIT 10 Mode Code 10
BIT 9 Mode Code 9
BIT 8 Mode Code 8

BIT 7 Mode Code 7
BIT 6 Mode Code 6
BIT 5 Mode Code 5
BIT 4 Mode Code 4

BIT 3 Mode Code 3
BIT 2 Mode Code 2
BIT 1 Mode Code 1
BIT 0 Mode Code 0

MRT/MON MODE
MRT/MON RT CONTROL BLOCK

Name: **Mode Code Enables 31- 16**
Address: **CB Base Address + 001E (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: This location in the RT Control Block is used to enable particular Mode Codes at the RT level.

BIT 15 Mode Code 31
BIT 14 Mode Code 30
BIT 13 Mode Code 29
BIT 12 Mode Code 28

BIT 11 Mode Code 27
BIT 10 Mode Code 26
BIT 9 Mode Code 25
BIT 8 Mode Code 24

BIT 7 Mode Code 23
BIT 6 Mode Code 22
BIT 5 Mode Code 21
BIT 4 Mode Code 20

BIT 3 Mode Code 19
BIT 2 Mode Code 18
BIT 1 Mode Code 17
BIT 0 Mode Code 16

4.3.3.6.3 Subaddress Control Blocks

After each RT Control Block, there should be 64- (DEC) subaddress blocks (32- receive and 32-transmit). The SA blocks have to be in order with SA = 0 (receive) first and SA = 31 (dec) (transmit) last. The SA Blocks are shown in Table 4.3.3.6.3-1.

NOTE

THERE MUST BE 64 (DEC) OF THESE SUBADDRESS BLOCKS OR AT LEAST THE AMOUNT OF MEMORY REQUIRED FOR 64 BLOCKS AVAILABLE FOR EACH RT SIMULATED OR MONITORED, THAT IS, 32-RECEIVE AND 32-TRANSMIT. NOTE ALSO THAT THE INSTRUMENTATION BIT REDUCES THE NUMBER AVAILABLE BY HALF, IF ENABLED. HOWEVER, THE BOARD STILL REQUIRES THE ENTIRE 64 BLOCKS.

Table 4.3.3.6.3-1. Subaddress Control Block

Byte Address	
0	Data Pointer/SA Options
2	Reserved
4	SA Flags

MRT/MON MODE
MRT/MON SUBADDRESS CONTROL BLOCK

Name: **Data Pointer/SA Options**
Address: **Subaddress CB Base Address + 0000 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: The first subaddress location has two possible functions. In MRT Mode, it is the data pointer and in the Monitor Mode it contains the SA options.

MRT-Data Pointer: Each SA has a unique data pointer within a single page of memory (RT selected). In the case where consecutive messages are transmitted to the same subaddress, the previous message will be written over and possibly lost (since there is only one data pointer per SA). The VMIVME-6000 provides a "New Data Pointer" location in each data buffer to point to the next data buffer for that subaddress. If the New Data Pointer Option is not needed, the host can set the new data pointer with its own address so that all SA specific data will be written/read from one data buffer.

NOTE
THE NEW DATA POINTER DMA MAY BE DISABLED IN THE DMA DISABLE REGISTER.

BIT 15 Address bit 15
BIT 14 Address bit 14
BIT 13 Address bit 13
BIT 12 Address bit 12

BIT 11 Address bit 11
BIT 10 Address bit 10
BIT 9 Address bit 9
BIT 8 Address bit 8

BIT 7 Address bit 7
BIT 6 Address bit 6
BIT 5 Address bit 5
BIT 4 Address bit 4

BIT 3 Address bit 3
BIT 2 Address bit 2
BIT 1 Address bit 1
BIT 0 Address bit 0

MON-SA Options Bit Description: Normally, monitor mode records all bus traffic. With the "No Record" bit set (bit 15 of SA Options), the VMIVME-6000 will not add the message specified by this RT/SA block to the ring buffer.

Bits 14 and 13 of the SA options allow specific messages to START or STOP the monitor mode. The VMIVME-6000 will be initialized to record messages as defined by the host programmed control and SA blocks. If a command is received to an RT/SA combination that has the "Stop Record" bit set in the SA options, the board will stop monitoring the bus. It will not record any more 1553 bus traffic until a message is sent to a RT/SA combination that has the "Start Record" bit set in the SA options, or until the board is re-initialized. The VMIVME-6000 may be "Stopped" and "Started" an unlimited number of times.

If bit 10 of the SA options is set, the board will generate a 50 nsec scope SYNC on reception of a message to that particular RT/SA combination. See Appendix C for connector information on the Scope SYNC.

BIT 15 No Record - Do not record message to this subaddress.

BIT 14 Start Recording - Record all messages that occur after and including the message to this TA/SA.

BIT 13 Stop Recording - Do not record messages until another "Start Record" message is recieved.

BIT 12 Reserved, set to logic "zero"

BIT 11 Reset Time Tag Counter

BIT 10 Scope SYNC Enable

BITS 9-0 Reserved, set to logic "zero"

MRT/MON MODE
MRT/MON SUBADDRESS CONTROL BLOCK

Name: **Subaddress (SA) Flags**
Address: **Subaddress CB Base Address + 0004 (Hex)**
Address Space: **VMEbus Standard Address Space**
Type: **Read/Write**

Description: These flags are applicable to the particular subaddress only, and are stored in MRT/MON RAM space during MRT/MON initialization.

BITS 15-7 Reserved, set to logic "zero"

BIT 6 **Enable Simulated RT Ring Buffer -** Messages to a simulated RT subaddress with this bit set to a “1” will be stored in the Ring Buffer instead of the location pointed to by the data pointer. The starting address and length of the Ring Buffer is defined in the MRT Header Block. This option is suggested only for receive subaddresses. Transmit subaddresses should use the data buffers for consistent data availability.

BIT 5 **Monitor Valid Message Only -** The board will store only valid 1553 messages in the ring buffer. The validity is determined by the Error Mask ALU register.

BIT 4 **Mode Code Data Pointer Enable -** Valid for SA 0 and 31 in MRT MODE only. When this bit is set, the board will use the mode code data pointers in MRT RAM as the memory address to receive/store mode code data from/to.

BIT 3 **Interrupt on Valid Message -** Validity is established via the ISR and Error Mask. Bit 2 will be set when using this feature.

BIT 2 **Interrupt On This SA -** Interrupt at end of message to this subaddress.

BIT 1 **Ignore Subaddress -** The VMIVME-6000 will completely ignore messages to this subaddress including posting of information, data, timetags, etc. The command word will be treated as if it were not sent.

BIT 0 **Illegal CW Received -** Set Manchester Error bit in status response.

4.3.3.6.4 Data Buffer Format

Simulate Data Format: Each subaddress block contains a single data pointer. If more than 1 message is received by the subaddress then the previous message will be written over (unless the New Data Pointer option is used). Table 4.3.3.6.4-1 shows the format of the data buffer. Note that, the transmit buffers must allow 12 locations for message overhead, so the first DW to be transmitted should be located at "DATA POINTER + 12 (DEC words)". The "New Data Pointer" allows dynamic updating of the data pointer (changing it "on the fly"). The pointer contains the address of the next data buffer to be used by this terminal address/subaddress. CW is the received command word. The time tag is the value of the counter at the time the command word was declared valid. The ISR and TSR are discussed in Section 4.2.3.

Monitor Data Format: Messages received by the VMIVME-6000 that are addressed to an RT being monitored are stored in a ring buffer format. In this format, succeeding messages are stored (via DMA) consecutively in on-board memory. The monitor format is shown in Table 4.3.3.6.4-1. Included in each entry in the ring buffer is a "pointer to the next message". This will contain the address in memory for the beginning of the next message in the ring buffer. If the current message is the last in the buffer, the "pointer" will point to itself. The format of each ring buffer entry is shown in Table 4.3.3.6.4-1.

Table 4.3.3.6.4-1. MRT/MON Data Buffers

Simulated RT Data Buffer Byte Address		Monitored RT Data Buffer
0	New Data Pointer	Pointer to Next Message
2	Command Word 1	Command Word 1
4	Reserved	Status Word 1
6	Reserved	Response Time 1
8	Reserved	Command Word 2
A	Reserved	Status Word 2
C	Reserved	Response Time 2
E	GAB Time	Gap Time
10	Time Tag MS	Time Tag MS
12	Time Tag LS	Time Tag LS
14	ISR	ISR
16	TSR	TSR
18	Data Word 1	Data Word 1
	Last Data Word	Last Data Word

4.3.3.7 MRT/MON Broadcast Operation

The VMIVME-6000 is capable of broadcasting. The simulated RTs will set the broadcast received bit in the appropriate status word (LSW for 1553B). The broadcast option is enabled in the MRT header block control word (see Section 4.3.3.6).

A set of one RT and 64 subaddress control blocks is required for executing broadcast. The broadcast control blocks can be located anywhere in the chain of RT Control Blocks, as long as the broadcast option is selected and the RT count takes the added Control Blocks into account. The Terminal Address for the block should be set to 1F (Hex).

The board is also capable of processing broadcast mode codes. Broadcast mode codes are enabled when the broadcast function is enabled, but may be disabled in the MRT header block control word, or in the individual RT Control Block Control Words (see Section 4.3.3.6.1).

4.3.3.8 MRT Mode Code Operation

The VMIVME-6000 can process all the defined mode codes. There are two 16-bit words of enables for each RT (for a total of 64 (dec) words) in the MRT/MON RAM. Any combination of mode codes may be enabled for any or all of the RTs. In cases where a subaddress is received that is defined as a mode code, and the mode code is not enabled, the VMIVME-6000 will treat the CW as an illegal CW and transmit a SW with the message error bit set.

4.3.3.8.1 Enabling Mode Codes

There are two words of enables per RT Control Block. Each bit corresponds to a mode code beginning with bit 0 of the first enable word which corresponds to mode code 0 (zero) (normally Dynamic Bus Allocation). Figure 4.3.3.8.1-1 defines the format for enabling mode codes.

4.3.3.8.2 Mode Code Interrupts

There are 128-words of MRT/MON RAM (2 words per RT) for Mode Code Interrupts at the RT level as shown in Figure 4.3.3.8.1-1. The VMIVME-6000 can be programmed to interrupt on any individual or combination of mode codes for any RT or combination thereof. Note that, if a Mode Code is determined to be illegal for any reason, the interrupt will not be processed. See Section 4.4 (A and B Mode Code Interrupt Enables) for more information on Mode Code Interrupts in MRT/MON RAM.

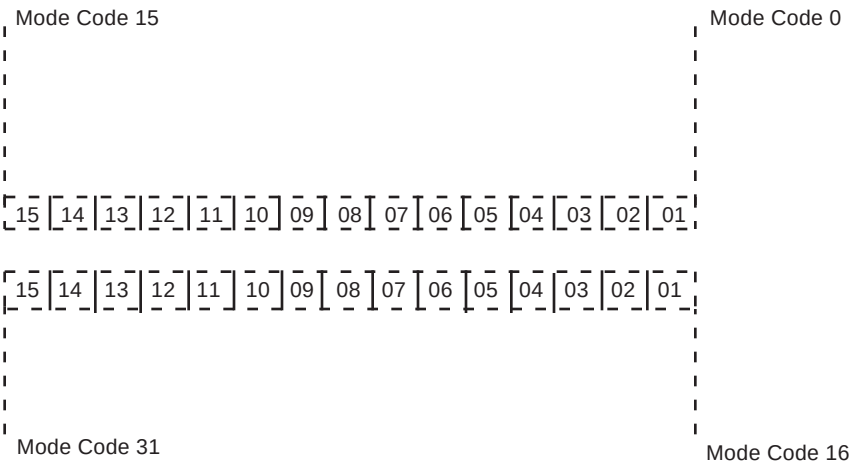


Figure 4.3.3.8.1-1. Mode Code Enables

4.3.3.8.3 Mode Codes

Dynamic Bus Allocation: The VMIVME-6000 will switch automatically to bus controller mode if the RT's corresponding Bus Controller Control Block Address is nonzero. The VMIVME-6000 will set the acceptance bit automatically. If the Control Block address is "zero", the VMIVME-6000 will not switch and will transmit the SW exactly as it is. After transmitting the status response, the VMIVME-6000 will begin executing bus controller mode (using the given control block address).

Synchronize: The "Synchronize" mode code (without data) causes the VMIVME-6000 to reset the time tag counter to "zero" (pulsed reset).

NOTE

THERE IS ONE 32-bit COUNTER FOR THE ENTIRE BOARD (NOT 32 UNIQUE COUNTERS, ONE FOR EACH RT). AS A RESULT, A SYNCHRONIZE MODE CODE TO ANY SIMULATED RT EFFECTIVELY SYNCHRONIZES ALL THE RTS.

Transmit Status Word: The VMIVME-6000 stores the LSW transmitted by each RT and retransmits that LSW for this mode code (according to 1553B).

Initiate Self-Test: The VMIVME-6000 will execute its power-up self-test and update the corresponding BIT word for the current RT. The VMIVME-6000 will be "off-line" for approximately 200 μsec.

Transmitter Shutdown/Override: The VMIVME-6000 executes the "Transmitter Shutdown" mode code for the RT as specified in 1553B.

Inhibit Terminal Flag/Override: The VMIVME-6000 keeps track of whether or not these mode codes have been processed and acts accordingly on each subsequent status response.

Reset Remote Terminal : The VMIVME-6000 will clear the LCW, LSW, BIT word, and associated information that has resulted from 1553 data (such as transmitter shutdown). There are no intermessage gap implications for the Reset Remote Terminal mode code, unless the message is a broadcast mode code.

Transmit Vector Word: The VMIVME-6000 will get the vector word from the first Data Word location of the SA specified data buffer (transmit SA 0 or SA 31).

Synchronize with Data: The VMIVME-6000 will reset the entire 32-bit counter and then load the 16 LSBs of the counter with the associated data word.

Transmit Last Command: The VMIVME-6000 stores the LCW for each RT in MRT/MON RAM. The board will transmit the last command word stored for a particular RT, in response to this mode code.

Transmit Bit Word: There are 32-locations in MRT/MON RAM space dedicated to individual RT built-in-test words. The contents of the BIT words are listed in Table 4.3.3.8.3-1.

Selected Transmitter Shutdown/Override: This mode code is for boards with more than two buses and IS NOT applicable to the VMIVME-6000 (dual redundant). The VMIVME-6000 responds with status but doesn't actually perform a transmitter shutdown (or override). The associated data is available to the host in the data buffer.

Reserved Mode Codes: Normally, reserved mode codes are not enabled. If they are, the VMIVME-6000 will respond to them, but will take no further action.

Table 4.3.3.8.3-1. Bit Word

Bit	Description
15	Spare
14	DMA Error
13	Bus A Shutdown
12	Bus A Shutdown
11	Bus A Self Test Failure
10	Bus B Self Test Failure
9	Memory Self Test Failure
8	ALU Failure
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Internal Bit Failure
1	Reserved
0	Illegal Mode Code Received

4.4 EXTERNAL MRT/MON RAM

The VMIVME-6000 uses a separate 8 kwords of on-board RAM in MRT/MON mode to store information about the 32 possible RTs. This information is loaded by the VMIVME-6000 into the RAM during initialization from the control blocks. Only nonzero information will be used. The RAM should be cleared via a CLEAR XIO upon power-up, or by loading the RAM with "zeros", so that all locations not used will be considered default.

During operation of the VMIVME-6000 in MRT/MON mode, the host may wish to change some parameters of the board's operation that were programmed by the host, and loaded via DMA during initialization. These parameters may be changed "on the fly" by accessing the MRT/MON RAM. The host may read or write the RAM (via XIO) when the VMIVME-6000 is in OFF mode or between 1553 messages. Even though the entire 8 kwords may be read or written, the user will normally need to access only certain locations. The following Table lists the locations that the host may need to access.

Table 4.4-1. MRT/MON External RAM

Word Address (Hex)	Description
0000 to 001F	Lost B Interrupt Ring Buffer
01A0 to 01BF	New Pointer Mask (RT 0 to 31)
01C0 to 01DF	Mode Code Data Pointers
01E0 to 021F	Mode Code AINT Enable (2X32RT)
0220 to 025F	Mode Code BINT Enable (2X32RT)
0300 to 031F	Control Words (RT 0 to 31)
0480 to 049F	Status Word "Set" (RT 0 to 31)
04A0 to 04BF	Status Word "Clear" (RT 0 to 31)
04C0 to 04DF	Monitor Response Timeout (32 RT)
0520 to 053F	Response Mask TSR (32 RT)
0540 to 055F	No Transmit Mask (32 RT)
0600 to 0DFF	Data Pointers (64 SA X 32 RT)

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Lost B Interrupt Ring Buffer**
Address: **0000 to 001F (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: When the VMIVME-6000 initiates a B Interrupt In MRT/MON Mode, the board will first check the status of any previous B interrupts to see if they have been serviced. If the previous B interrupt has not been serviced, the board will store the previous B interrupt pointer and map in a 32-word ring buffer as shown in Table 4.4-1. Each entry in the ring buffer will consist of a 4-bit interrupt map followed by a 16-bit interrupt pointer. Once the ring buffer is filled, the next entry will begin at the first location of the buffer.

First Word in Ring Buffer (Interrupt Pointer)

BIT 15	Not Used	BIT 7	Not Used
BIT 14	Not Used	BIT 6	Not Used
BIT 13	Not Used	BIT 5	Not Used
BIT 12	Not Used	BIT 4	Not Used
BIT 11	Not Used	BIT 3	Address Bit 19
BIT 10	Not Used	BIT 2	Address Bit 18
BIT 9	Not Used	BIT 1	Address Bit 17
BIT 8	Not Used	BIT 0	Address Bit 16

Second Word in ring Buffer (Interrupt Pointer)

BIT 15	Address Bit 15	BIT 7	Address Bit 7
BIT 14	Address Bit 14	BIT 6	Address Bit 6
BIT 13	Address Bit 13	BIT 5	Address Bit 5
BIT 12	Address Bit 12	BIT 4	Address Bit 4
BIT 11	Address Bit 11	BIT 3	Address Bit 3
BIT 10	Address Bit 10	BIT 2	Address Bit 2
BIT 9	Address Bit 9	BIT 1	Address Bit 1
BIT 8	Address Bit 8	BIT 0	Address Bit 0

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **New Pointer Mask (RT 0 to 31)**
Address: **01A0 to 01BF (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: Addresses 1A0H through 1BFH of the MRT/MON RAM corresponds to the "New Data Pointer Masks" for RT addresses 0 through 31. Address 1A0H is the mask for RT address 0, 1A1H is the mask for RT address 1, etc..

The New Data Pointer Masks allow the host to preclude "New Data Pointer" updates based on conditions within the ISR. a "zero" will allow the New Data Pointer to be updated on all messages. A value that has a bit set corresponding to a bit in the ISR will cause the VMIVME-6000 to NOT update the New Data Pointer. This mask should be used if the host wants to ignore invalid data. Default is "zero" (New Data Pointer will always be updated).

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Mode Code Data Pointer**
Address: **01C0 to 01DF (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: Locations 01C0H through 01DFH of the MRT/MON RAM may be programmed by the host to store the data pointer for mode codes recieved by the possible 32 simulated/monitored RTs. Location 1C0H corresponds to Mode Code 0, while location 1DEH corresponds to Mode Code 31. This function must be enabled in the MRT SA flags. If this function is not enabled, the regular SA data pointers for SA 0 or SA 31 will be used.

BIT 15 Address Bit 15
BIT 14 Address Bit 14
BIT 13 Address Bit 13
BIT 12 Address Bit 12

BIT 11 Address Bit 11
BIT 10 Address Bit 10
BIT 9 Address Bit 9
BIT 8 Address Bit 8

BIT 7 Address Bit 7
BIT 6 Address Bit 6
BIT 5 Address Bit 5
BIT 4 Address Bit 4

BIT 3 Address Bit 3
BIT 2 Address Bit 2
BIT 1 Address Bit 1
BIT 0 Address Bit 0

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: Mode Code "A" Interrupt Enable (2 x 32 RT)
Address: 01E0 to 021F (Hex) (Word Addressing)
Address Space: MRT/MON RAM
Type: Read/Write

Description: There are two banks of 64 registers for enabling interrupts for each mode code at the RT level. Each bank corresponds to one of two levels of interrupts (A or B). In both banks of 64 registers, each RT has two 16-bit words for enabling A or B interrupts on mode codes. The least significant bit of the least significant word of the two-word enable corresponds to Mode Code 0, while the most significant bit of the most significant word of the two-word enable corresponds to Mode Code 31.

Most Significant Word

BIT 15	Mode Code 31	BIT 7	Mode Code 23
BIT 14	Mode Code 30	BIT 6	Mode Code 22
BIT 13	Mode Code 29	BIT 5	Mode Code 21
BIT 12	Mode Code 28	BIT 4	Mode Code 20
BIT 11	Mode Code 27	BIT 3	Mode Code 19
BIT 10	Mode Code 26	BIT 2	Mode Code 18
BIT 9	Mode Code 25	BIT 1	Mode Code 17
BIT 8	Mode Code 24	BIT 0	Mode Code 16

Least Significant Word

BIT 15	Mode Code 15	BIT 7	Mode Code 7
BIT 14	Mode Code 14	BIT 6	Mode Code 6
BIT 13	Mode Code 13	BIT 5	Mode Code 5
BIT 12	Mode Code 12	BIT 4	Mode Code 4
BIT 11	Mode Code 11	BIT 3	Mode Code 3
BIT 10	Mode Code 10	BIT 2	Mode Code 2
BIT 9	Mode Code 9	BIT 1	Mode Code 1
BIT 8	Mode Code 8	BIT 0	Mode Code 0

example: 01E0 RT 0 Least Significant Word
01E1 RT 0 Most Significant Word
01E2 RT 1 Least Significant Word
01E3 RT 1 Least Significant Word
:
021E RT 31 Least Significant Word
021F RT 31 Most Significant Word

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: Mode Code "B" Interrupt Enable (2 x 32 RT)
Address: 0220 to 025F (Hex) (Word Addressing)
Address Space: MRT/MON RAM
Type: Read/Write

Description: There are two banks of 64-registers for enabling interrupts for each mode code at the RT level. Each bank corresponds to one of two levels of interrupts (A or B). In both banks of 64-registers, each RT has two 16-bit words for enabling A or B interrupts on mode codes. The least significant bit of the least significant word of the two-word enable corresponds to Mode Code 0, while the most significant bit of the most significant word of the two-word enable corresponds to Mode Code 31.

Most Significant Word

BIT 15 Mode Code 31	BIT 7 Mode Code 23
BIT 14 Mode Code 30	BIT 6 Mode Code 22
BIT 13 Mode Code 29	BIT 5 Mode Code 21
BIT 12 Mode Code 28	BIT 4 Mode Code 20
BIT 11 Mode Code 27	BIT 3 Mode Code 19
BIT 10 Mode Code 26	BIT 2 Mode Code 18
BIT 9 Mode Code 25	BIT 1 Mode Code 17
BIT 8 Mode Code 24	BIT 0 Mode Code 16

Least Significant Word

BIT 15 Mode Code 15	BIT 7 Mode Code 7
BIT 14 Mode Code 14	BIT 6 Mode Code 6
BIT 13 Mode Code 13	BIT 5 Mode Code 5
BIT 12 Mode Code 12	BIT 4 Mode Code 4
BIT 11 Mode Code 11	BIT 3 Mode Code 3
BIT 10 Mode Code 10	BIT 2 Mode Code 2
BIT 9 Mode Code 9	BIT 1 Mode Code 1
BIT 8 Mode Code 8	BIT 0 Mode Code 0

example:
```
0220  RT 0 Least Significant Word
0221  RT 0 Most Significant Word
0222  RT 1 Least Significant Word
0223  RT 1 Least Significant Word
      :
025E  RT 31 Least Significant Word
025F  RT 31 Most Significant Word
```

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Control Words (RT 0 x 31)**
Address: **0300 to 031F (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: Addresses 300 through 31F of the MRT/MON RAM are used to hold the RT Control Words corresponding to RT addresses 0 through 31. These control words are the logical OR of each individual RT Control Word with the Master Control Word of the Header Block, along with some internal microprogram flags. The bit map of these locations corresponds to the RT Control Word. Before changing these locations, the host should first read the location to be changed. The host may then selectively set or clear the appropriate bits, being careful to leave all other bits unchanged. The bits that may be modified are bits 15, 14, 13, 12, and 6.

BITS 15 - 14 Bits 15 and 14 eliminate the respective subaddress (0 and 31) from being declared as a mode code. Once a subaddress is disabled, it becomes a normal valid subaddress like all other subaddress.
BIT 13 A Bus Disable - totally disables A bus
BIT 12 B Bus Disable - totally disables B bus
BIT 11 **Switchover Disable** - Don't do bus switchover at all. This bit may be set to logic "one" to eliminate possibility of bus switchover occurring. Conditions that possibly would warrant disabling bus switchover would be monitor, or simulating a specification that does not provide for bus switchover.
BIT 10 **Broadcast Enable** - An RT control Block with TA=31 and bit 9 set must be provided.
BITS 9 - 8 **Rt Simulate Master/Rt Monitor Master-** The VMIVME-6000 distinguishes simulated RTs from monitored RTs via bits 9 and 8 of the control words. Bit 9 should be set if the RT is to be simulated and bit 8 if the RT is to be monitored. If bit 9 or 8 is not set, then "programming Error" will be set, and the RT will be ignored.
BIT 7 **Reserved, set to logic "zero"**
BIT 6 **Broadcast Mode Code Processing Disable** - The board will NOT execute a Broadcast Mode Code. The Broadcast Received bit will still be set.
BITS 5-2 **Reserved, set to logic "zero"**
BIT 1 **F18-1553A** - Obey protocol of 1553A and F18 (refer to respective specifications for more details).
BIT 0 **F16** - Follow the protocol and configure the status word based on F16.

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Status Word "Set" (RT 0 x 31)**
Address: **0480 to 049F (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: The VMIVME-6000 may be programmed to "set" and or "clear" status word bits. After each SW transmittal, the VMIVME-6000 will set and/or clear bits from the next SW response based on the Status Word "Set" and "Clear" registers for the particular RT. (There are a total of 32-SET registers and 32-CLEAR registers.) If these registers are left "zero", then there will be no real-time changing of the of the status words "on the fly". The host may write to these locations at any time. Note that the VMIVME-6000 will continue setting or clearing bits of the SW as long as the mask is nonzero. The Host Array and ALU register global SW "set" and "clear" masks also control this function for all simulated RTs.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Status bit 10
BIT 9 Status bit 9
BIT 8 Status bit 8

BIT 7 Status bit 7
BIT 6 Status bit 6
BIT 5 Status bit 5
BIT 4 Status bit 4

BIT 3 Status bit 3
BIT 2 Status bit 2
BIT 1 Status bit 1
BIT 0 Status bit 0

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Status Word "Clear" (RT 0 x 31)**
Address: **04A0 to 04BF (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: The VMIVME-6000 may be programmed to "set" and or "clear" status word bits. After each SW transmittal, the VMIVME-6000 will set and/or clear bits from the next SW response based on the Status Word "Set" and "Clear" registers for the particular RT. (There are a total of 32-SET registers and 32-CLEAR registers.) If these registers are left "zero", then there will be no real-time changing of the of the status words "on the fly". The host may write to these locations at any time. Note that the VMIVME-6000 will continue setting or clearing bits of the SW as long as the mask is nonzero. The Host Array and ALU register global SW "set" and "clear" masks also control this function for all simulated RTs.

BIT 15 Reserved, set to logic "zero"
BIT 14 Reserved, set to logic "zero"
BIT 13 Reserved, set to logic "zero"
BIT 12 Reserved, set to logic "zero"

BIT 11 Reserved, set to logic "zero"
BIT 10 Status bit 10
BIT 9 Status bit 9
BIT 8 Status bit 8

BIT 7 Status bit 7
BIT 6 Status bit 6
BIT 5 Status bit 5
BIT 4 Status bit 4

BIT 3 Status bit 3
BIT 2 Status bit 2
BIT 1 Status bit 1
BIT 0 Status bit 0

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Monitor Response Timeout (32 RT)**
Address: **04C0 to 04DF (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: The default response timeout in all modes is 14 μsec. The response timsout of the VMIVME-6000 in monitor mode (in microseconds) is programmable by writing to locations 4C0H-4DFH. These locations correspond to the 32 possible RTs that may be monitored. The acceptable values for these locations are 7 to 7FFFH.

BIT 15 Count bit 15
BIT 14 Count bit 14
BIT 13 Count bit 13
BIT 12 Count bit 12

BIT 11 Count bit 11
BIT 10 Count bit 10
BIT 9 Count bit 9
BIT 8 Count bit 8

BIT 7 Count bit 7
BIT 6 Count bit 6
BIT 5 Count bit 5
BIT 4 Count bit 4

BIT 3 Count bit 3
BIT 2 Count bit 2
BIT 1 Count bit 1
BIT 0 Count bit 0

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Response Mask TSR (32 RT)**
Address: **0520 to 053F (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: The Response Mask in MRT RAM provides a way for the board to respond (in MRT mode) to a message which contains a message error. The Response Mask is compared to the TSR, and if a bit is common between the two, a response to the message will be sent. This is basically usefully when simulating 1553A RTs, but may be used with all protocols. Locations 520 (Hex) to 53F (Hex) correspond to the 32 possible RT addresses.

BIT 15 Invalid Message Type
BIT 14 Mode Code Error
BIT 13 Bus Busy
BIT 12 Transmitter Timeout

BIT 11 TA Compare
BIT 10 Instrumentation Bit Error
BIT 9 -Word Count Error
BIT 8 +Word Count Error

BIT 7 Reserved, set to logic "zero"
BIT 6 Gap Error
BIT 5 -Bit Count Error
BIT 4 +Bit Count Error

BIT 3 Response Error
BIT 2 SYNC Error
BIT 1 Parity
BIT 0 Manchester Error

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **No Transmit Mask (32 RT)**
Address: **0540 to 055F (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: The VMIVME-6000 will not transmit data (in MRT mode) if corresponding bits are set in the status response and No Transmit Mask (i.e., in 1553B, the RT is not supposed to transmit data if the busy bit is set in the status response). Addresses 540H through 55FH correspond to the possible 32-simulated RTs.

BIT 15 Invalid Message Type
BIT 14 Mode Code Error
BIT 13 Bus Busy
BIT 12 Transmitter Timeout

BIT 11 TA Compare
BIT 10 Instrumentation Bit Error
BIT 9 - Word Count Error
BIT 8 +Word Count Error

BIT 7 Reserved, set to logic "zero"
BIT 6 Gap Error
BIT 5 - Bit Count Error
BIT 4 +Bit Count Error

BIT 3 Response Error
BIT 2 SYNC Error
BIT 1 Parity
BIT 0 Manchester Error

MRT/MON MODE
EXTERNAL MRT/MON RAM

Name: **Data Pointers (64 SA x 32 RT)**
Address: **0600 to 0DFF (Hex) (Word Addressing)**
Address Space: **MRT/MON RAM**
Type: **Read/Write**

Description: Locations 600 (Hex) through DFF (Hex) of the MRT/MON RAM are used by the board to store the data pointers (if simulating) or SA options (if monitoring) programmed in the subaddress blocks. Address 600H corresponds to RT address 0, receive, subaddress 0. Each address has 32-receive subaddress locations followed by 32-transmit subaddress locations, starting with address 0 and incrementing to address 31.

BIT 15 Data Ptr bit 15/SA Op- No Record
BIT 14 Data Ptr bit 14/SA Op- Start Record
BIT 13 Data Ptr bit 13/SA Op- Stop Record
BIT 12 Data Ptr bit 12/SA Op- Reserved

BIT 11 Data Ptr bit 11/SA Op- Reset Timetag Counter
BIT 10 Data Ptr bit 10/SA Op- Scope Sync Enable
BIT 9 Data Ptr bit 9/SA Op- unused
BIT 8 Data Ptr bit 8/SA Op- unused

BIT 7 Data Ptr bit 7/SA Op- unused
BIT 6 Data Ptr bit 6/SA Op- unused
BIT 5 Data Ptr bit 5/SA Op- unused
BIT 4 Data Ptr bit 4/SA Op- unused

BIT 3 Data Ptr bit 3/SA Op- unused
BIT 2 Data Ptr bit 2/SA Op- unused
BIT 1 Data Ptr bit 1/SA Op- unused
BIT 0 Data Ptr bit 0/SA Op- unused

4.5 INTERRUPTS

All modes have maskable 2-level interrupt capability. The "High Priority" A Interrupt, and the Standard B Interrupt will cause the IRQ line to the VMEbus to be asserted low . When an A level interrupt occurs, the board will halt its current operation and return to OFF mode. The board considers the A interrupt serviced when the A INT Vector is read during the VMEbus interrupt acknowledge, and the A interrupt pointer is either read by the host, or cleared through the clear A interrupt pointer bit in the XIO Hardware Control register. The events that will cause an A interrupt to occur are programmable in the A Interrupt Mask. The A Interrupt mask is contained in each Control Block for Bus Controller/Simulator mode, and in the Master Header Block as well as the individual RT Control Blocks for MRT/MON mode.

The B level interrupt is used for standard message processing. A "B" interrupt will not stop board operation, but instead will allow board operation to continue. The VMIVME-6000 considers the B interrupt serviced when the B INT Vector is read during the VMEbus interrupt acknowledge cycle, and the B interrupt pointer is either read by the host, or cleared through the clear B interrupt pointer bit in the XIO Hardware Control register. The events that will cause a B interrupt to occur are programmable in the B Interrupt Mask. The B Interrupt Mask is contained in each Control Block for Bus Controller/Simulator mode, and in the Master Header Block as well as the individual RT Control Blocks in MRT/MON mode.

The VMIVME-6000 provides interrupt pointers and maps for both A and B level interrupts. These pointers/maps contain the address of the last BC/SIM Control Block or RT/MON data buffer that caused an interrupt. The pointers are located in the Host ASIC Hardware registers and are accessed by the host via XIO commands.

NOTE

THESE POINTERS/MAPS ARE ONLY A 20-bit ADDRESS. IF THE CONTROL OR DATA BLOCKS ARE ABOVE THE FIRST 1 MEGABYTE PAGE OF MEMORY, THE HOST MUST ADD THE MEMORY PAGE ADDRESS TO THIS 20-bit POINTER/MAP TO GET THE REAL VMEBUS 24-bit ADDRESS.

The following steps should be taken by the host to properly service interrupts on the VMIVME-6000.

a. Read the ASR to determine the level and type of interrupt

b. If the interrupt is a B interrupt on XIO complete, the ASR must be read a second time to clear the XIO complete bit. Also, if the interrupt is a B interrupt on XIO complete, the B interrupt pointer must be cleared by writing to the clear interrupt pointer bit of the XIO Hardware Control register.

If the interrupt is any other type or level, the appropriate interrupt pointer and map should be read to determine the control block or data buffer that caused the interrupt. This pointer will be for the current interrupt. If a B interrupt is asserted before the previous B interrupt is serviced, a bit will be set in the ASR, and the previous B interrupt pointer and map will be stored in the lost B interrupt ring buffer in MRT/MON RAM.

4.5.1 Interrupt Enable/Disable

Bits 14, 13, and 4 of the Control register (see Section 4.2.2.1, Hardware registers) are used to enable/disable the interrupt hardware. These bits enable a hardware interrupt (IRQ) and the output of the interrupt vector to the VMEbus. They have no effect on the interrupt masks or firmware such that the VMIVME-6000 could be configured to interrupt itself (and set ASR bits 14 and 13 of the ASR) without setting the IRQ to the host. This gives the host the option of setting the appropriate masks and polling the ASR and/or pointers rather than go through a full-scale interrupt sequence.

Bus Controller provides an interrupt mask for each message. MRT/MON has a master interrupt mask in the header word and an interrupt mask for each RT in the RT Control Blocks.

4.5.2 Interrupt Status Register/Masks (ISR)

The Interrupt Status Register bits are shown below. This Internal ALU register informs the host of the events listed. A mirror image serves as the A and B Interrupt Masks so the user may interrupt on any ISR events or conditions. Only nonzero ISRs are posted to the host so the host will always have the most recent ISR in which an event happened (programmable in VMIVME-6000 Option register and ISR Mask).

BIT 15 Transmission Error
BIT 14 DMA Error
BIT 13 Monitor Ring Buffer Page (64 kbytes) Full
BIT 12 Interrupt at End of Message

BIT 11 Programming Error
BIT 10 Status Word Mask Compared
BIT 10 Ring Buffer Full
BIT 9 Stop
BIT 8 Context Lock Lost

BIT 7 Illegal Command Word Received
BIT 6 CW Trigger
BIT 5 Mode Code was Received
BIT 4 Automatic Retry Successful

BIT 3 Automatic Retry Failed
BIT 3 Bus Switchover
BIT 2 BIT Failed
BIT 1 BIT Data Compare
BIT 0 Message was on B (secondary) Bus

4.5.2.1 Transmission Error

The Transmission Status register bits are shown below. This Internal ALU register informs the host of the errors associated with bit 15 of the ISR. A mirror image serves as a TSR Mask. The TSR Mask gives the host control over which transmission errors cause bit 15 of the ISR to be set and, in effect, gives the host control over which transmission errors will initiate an interrupt. If a bit is set to a logic "one" by the host in the TSR Mask, and an event occurs that causes the corresponding bit to be set in the TSR, then the board will set bit 15 of the ISR.

BIT 15	**Invalid Message Type**	**BIT 7**	**Reserved, set to logic "zero"**
BIT 14	**Mode Code Error**	**BIT 6**	**Gap Error**
BIT 13	**Bus Busy**	**BIT 5**	**- Bit Count Error**
BIT 12	**Transmitter Timeout**	**BIT 4**	**+Bit Count Error**
BIT 11	**TA Compare**	**BIT 3**	**Response Error**
BIT 10	**Instrumentation Bit Error**	**BIT 2**	**SYNC Error**
BIT 9	**- Word Count Error**	**BIT 1**	**Parity**
BIT 8	**+Word Count Error**	**BIT 0**	**Manchester Error**

4.5.2.2 DMA Error

Bit 14 of the ISR indicates that something is wrong with the memory channel. The VMIVME-6000 must have data available to it from the memory when it is needed in the current 1553 message. If a DMA Timeout occurs while the board is accessing control block information, the VMIVME-6000 will flag the error in the ISR and return to OFF mode. If the DMA error occurs while the board is accessing data for a 1553 data transfer, the data word will be transmitted as a "zero", and it will be the responsibility of the host to detect that a DMA error occurred, by interrupting on the condition (set bit 14 in the A or B interrupt mask). The subsystem error bit of the SW may be programmed to be set on a DMA error via a bit in the option register.

4.5.2.3 B Interrupt Not Serviced

The VMIVME-6000 considers a B Interrupt serviced when the B INT vector is read during a VMEbus interrupt acknowledge cycle, and the B Interrupt Pointer is either read by the host, or is cleared by a bit in the XIO Control Register (see Section 4.2.2.1, Hardware Registers.) If the board attempts a B interrupt before the previous B interrupt was serviced, it will set bit 3 of the ASR, and will store the B INT pointer and map of all following interrupts in the Lost B Interrupt Ring Buffer in MRT/MON RAM. Additionally, the Lost B Interrupt Counter Register will be incremented each time a B Interrupt is asserted before the initial B interrupt was serviced and the Lost B Interrupt Pointer Register will contain the address in MRT/MON ROM where the next Lost B Interrupt Pointer will be stored. The VMIVME-6000 will not update the B INT pointer and map with the most recent control block (BC/SIM) or data buffer (MRT/MON) address until the current B INT is serviced. The following steps should be used as minimum to service a Lost B Interrupt:

1. Within the Interrupt Service Routine (ISR) first read ASR bits 13 (B Interrupt Requested) and 3 (B Interrupt Not Serviced.)

2. If bit 13 is set and bit 3 is not, then only one interrupt is pending and processing for this interrupt can take place as follows at step 3. If both bits 13 and 3 of the ASR are set, then there are at least two interrupts pending and processing for all interrupts should take place at step 6.

3. Read the B Interrupt Map and Address Pointer registers to complete servicing of the interrupt.

4. Clear ASR bits 13 and 3 by writing zeros to both bits of the ASR at offset 98 HEX.

5. Exit the ISR.

6. Read the B Interrupt Map and Address Pointer registers to complete servicing of the initial interrupt.

7. Read the Lost B Interrupt Counter register to determine how many interrupts have asserted since the last B interrupt was serviced.

8. Read the Lost B Interrupt Pointer register to determine the address in External MRT/MON RAM where the next Lost B Interrupt Pointer will be stored.

9. Determine where the first address location of the lost B interrupts is by multiplying the value read at the Lost B Interrupt Counter Register by two 16-bit words (for each interrupt entry in the Lost B Interrupt Ring Buffer) and subtracting this value from the value read at the Lost B Interrupt Pointer register.

10. Read all map and address locations in External MRT/MON RAM.

11. Clear ASR bits 13 and 3 by writing zeros to both bits of the ASR at offset 98 HEX.

12. Clear the Lost B Interrupt Counter by writing it to a zero value.

13. Read the ASR one last time to be sure no interrupts are pending.

14. Exit the ISR.

NOTE:

BE SURE TO FOLLOW ALL RULES FOR READING AND WRITING THE VARIOUS REGISTERS.

4.5.2.4 End of Message Interrupt

This interrupt indicates one of the SA Flags was set requesting an End of Message Interrupt in MRT/MON mode. In BC/SIM mode, this bit indicates the board has completed processing the current control block. In both BC/SIM and MRT/MON modes, bit 12 of the appropriate interrupt mask (A or B) should be set for an end of message interrupt to occur.

4.5.2.5 Programming_Error

The VMIVME-6000 will flag several conditions as programming errors. The programing errors that are detected are listed below. A bit will be set in the ISR indicating a Programming Error occurred, and a bit will be set in the Programming Error register indicating what the error is. This register must be cleared by the host.

Table 4.5.2.5-1. Programming Error Register

Bit	Description
15	Invalid Mode - The user attempted to enter an invalid mode.
14	Invalid Gap - Intermessage gap less than the allowable 30 μsec (Bus Controller).
13	Invalid Response Timeout - Has to be "0" (default) or 7 or greater.
12	Data Word Count - Data Word Count of control block and word count of the command word do not agree, or the word counts of both command words of an RT-RT message do not agree.
11	Invalid XIO - Invalid XIO Command was attempted.
10	Inconsistent Control Word - An inconsistent control word such as RT to BC (bit 15) and RT to RT (bit 14) "set" in the same message (Bus Controller).
9	SA Flags/Options Inconsistent - Inconsistent bits set in the SA flags or SA options such as both start and stop record.
8	BC Pointer/Conditional Branch Count = 0 - The BC pointer table or a conditional branch was enable but the count was "0".
7	Major Time Frame - Major time frame is enabled but the counters are LESS than the time to execute the list.
6	Dynamic Bus Allocation Error - A CBADDR for the new mode wasn't given.
5	Invalid CBADDR - CBADDR was "0" during START XIO. The board will still attempt to start.
4	RT Count = 0 - If a START initialization is executed there should have been at least 1 RT (MRT/MON).
3	Invalid Pointer - Initial Ring Buffer pointers are invalid.
2	RT Control Word - Bit 9 (simulate) or 8 (monitor) has to be set in the RT control word.
1	Both Simulate and Broadcast Enabled in same message.
0	DMA latency - Caused Programmed Gap Time to be exceeded.

4.5.2.6 Status Word Mask Compare

In Bus Controller mode, the received SW had a "one" (logic high) that corresponded to a "one" in the SW mask programmed by the host.

4.5.2.7 Ring Buffer Page Full

The Ring Buffer has reached the end of a 64 k page of memory. The next message entry in the ring buffer will be stored at the beginning of a new page.

4.5.2.8 Ring Buffer Full

The Ring Buffer has reached the ending pointer. The next message entry in the ring buffer will be stored at the beginning of the ring buffer.

4.5.2.9 "STOP" Detected

Indicates the board stopped processing Bus Controller control blocks because the "STOP" bit was set in control word. The board has returned to OFF mode.

4.5.2.10 Context Lock Lost

While acting as monitor, once the VMIVME-6000 receives a valid message, a context lock is established. If an invalid message occurs on the bus, the monitor will lose context until the next valid message is received.

4.5.2.11 Illegal Command Word Received

An illegal CW is a command word that meets the word validation criteria, but requests the RT to perform a function that is not enabled. The VMIVME-6000 declares a CW illegal if it addresses a mode code that is not enabled, or addresses a subaddress with SA flag bit "zero" set. The VMIVME-6000 sets the message error bit automatically.

4.5.2.12 Command Word Trigger

If the command trigger word located in the Internal ALU register compared to the just received valid command word, bit 6 of the ISR will be set.

4.5.2.13 Mode Code Received

In MRT mode, when the VMIVME-6000 receives and executes a mode code, bit 5 of the ISR will be set.

4.5.2.14 Auto_Retry_Successful

An automatic retry was successfully executed. The number of retries, bus (it or opposite), and the conditions that initiate auto retry are programmable (via control block, Control Word 2, Auto SW Mask, and Auto TSR Mask).

4.5.2.15 Auto_Retry_Failed

An automatic retry was executed, but the message transfer was not successful in the number of retries, or on the bus (same or opposite), or under the conditions that initiated auto retry.

4.5.2.16 Bus_Switchover_Performed

The VMIVME-6000 will execute a bus switchover if the following conditions exist:

a. The VMIVME-6000 is currently processing a previously received command word

b. A second valid command word is received on the opposite bus

c. The CW is addressed to an RT that the VMIVME-6000 is simulating or monitoring and does not have bus switchover disabled (bit 11 of the RT Control Word set).

d. The 1553 bus to which the switch will be made is not disabled (via a "Transmitter Shutdown" mode code or host programming via the RT Control Word).

Bit 3 will be set in the ISR and posted to the new message that initiated the bus switchover. Refer to bit 0 of the ISR in order to determine which bus was terminated. Note that the "Gap Measurement" is not valid for a message initiated via a bus switchover, and the VMIVME-6000 will not generate errors in a transmit status response following a switchover.

4.5.2.17 Bit_Failed

There are three self-tests in which this bit may be set. It will be set upon power-up if ANY errors are detected during the power-up self-test. It will be set if Diagmode detects any errors - data compare and/or transmission errors. It will be set if a mode code is received initiating the RT self-test and errors are detected.

4.5.2.18 Bit Data Compare (Loop Fail)

Transmitted data did not agree with received data. Set anytime the board's self-test (including Loop Around) detects a data compare error.

4.5.2.19 Message on B (Secondary) Bus

If this bit is "zero" (logic low), the message occurred on the A bus (primary) and if it's "one" (logic high), the message occurred on the B bus.

4.5.3 Interrupt Vectors

The VMIVME-6000 supports interrupt Release-on-Acknowledge (ROAK), and has 16-bit interrupt vectors to support both A and B level interrupts. During initialization of the board, the host should program the interrupt vectors for the A and B levels of interrupt. The A INT and B INT vector registers are Host ASIC Hardware registers and are loaded by the host using XIO. If during operation of the board, both an A and B level interrupts are pending, the A interrupt vector will take priority, and will be outputted on the first interrupt acknowledge cycle.

4.6 ERROR GENERATION

4.6.1 Error Generation Selects

All modes of the VMIVME-6000 have the capability to generate 1553 bus errors. The errors may be generated on a control block basis in BC mode, and at the RT Header level or individual RT Control Block in MRT/MON mode. Error generation is also possible in Diagmode. The possible error generation choices are listed below in Table 4.6.1-1.

Table 4.6.1-1. Error Generation Selects

Bit	Description
15	Manchester - The particular bit time is programmable.
14	Parity
13	SYNC
12	Bit Count Error - Word length programmable in Frame Register.
11	TA Error - (MRT) Will force an erroneous +1 TA into status word.
10	+Word Count
9	- Word Count
8	Respond on Wrong Bus
7	Gap Between Data Words
6	Reserved
5	Reserved
4	Reserved
3	SW1 - In both MRT and SIM modes.
2	SW2 - In both MRT and SIM modes.
1	Error in CW1 (BC)/Positive SYNC Words (DIAG)
0	Error in CW2 (BC)/Negative SYNC Words (DIAG)

4.6.1.1 Manchester Error

The VMIVME-6000 will generate a Manchester Error based on the Manchester Error Type Register (shown in 4.6.1.1-1). Default is a Hi-Biphase error at bit time 8. The bit time in which the error will be generated is selected through the Bit Time Error Register located in the Special Function XIO registers, and described in Section 4.2.2.2. For a normal 20-bit time word, the range of values is 0 to 19.

Table 4.6.1.1-1. Manchester Type Register

Bit	Description
15	HI BI-0 Error - Biphase will be high for entire bit time.
14	LOW BI-0 Error - Biphase will be low for entire bit time.
13	SYNC Error - Board will generate a 500 nsec SYNC error.
12	Last Half SYNC Error - Error will be in last 500 nsec of bit time.
11	+Transition Error - Causes transition delay after ideal crossing.
10	-Transition Error - Causes transition before ideal crossing.
9-4	Reserved
3-0	Transition Error Delay - If bits 10/11 set, causes 21 nsec delay per increment.

Hi-Biphase: If bit 15 of the Manchester Type register is set, the board will generate a Hi-Biphase error for the bit time specified in the Bit Time Error register, as specified by the RT validation test plan.

Lo-Biphase: If bit 14 is set, the board will generate a Lo-Biphase error for that bit time specified in the Bit Time Error Register, as specified by the RT validation test plan.

SYNC Error: If bit 13 is set, the VMIVME-6000 will generate a SYNC Error. The SYNC is divided into 3-bit times consisting of six 500 nsec time boards. Bit 12 determines if the error is to be in the first 500 nsec half of the particular bit time, or the last 500 nsec half. The bit time selected in the Bit Time Error register should be 0, 1, or 2 for a SYNC Error. Bit 14 or 15 should be set to select between Hi-Biphase or Lo-Biphase errors.

NOTE

WHEN ATTEMPTING TO GENERATE A SYNC ERROR, BE AWARE OF THE TYPE OF SYNC AND THE IMPLICATIONS. GENERATING A LO-BIPHASE ERROR ON THE LAST HALF OF BIT TIME 1 DURING THE CW (POSITIVE SYNC) WILL NOT SHOW UP BECAUSE THE BIPHASE WILL ALREADY BE LOW.

Transition Error: Bit 11 of the manchester type selects causes a plus transition error to occur. Bits 0 to 3 determine the amount of transition. The skew will be in approximately 20 nsec increments (0 = 20 nsec). A value of 6 in bits 0 to 3 will cause a skew of 140 nsec. Bit 10 causes a minus transition error. On a minus transition, the reference point will be 250 nsec before the ideal transition. The value inserted in bits 0 to 3 will subtract from the 250 nsec before the ideal transition. For example, a "one" in bits 0 to 3 will cause the transition 210 nsec before the ideal transition. Note that inserting a value large enough will generate a plus transition.

4.6.1.2 Parity Error

The VMIVME-6000 will invert the parity bit.

4.6.1.3 SYNC Error

The VMIVME-6000 will invert the SYNC.

4.6.1.4 Bit Count Error

The VMIVME-6000 will generate bit count errors. The word length is programmable in the Frame Length Register via an Operation Command, and may vary the word length from 17 bit times to 27 bit times. (See Section 4.2.2.2, Special Function registers, for details on the Frame Length register, 00A4 (Hex).) The default error is 19-bit times (-1 bit). A programmed bit time of 20 will not show up as an error. The Frame Length register is ignored except when the Bit Count Error bit is set in the Error Generation Selects.

4.6.1.5 Word Count Error

In MRT Mode, if the +WC or -WC bit is set, the number of data words transmitted by the VMIVME-6000 will be taken from the Error Data Word Count Register instead of the wordcount field of the command word. (See Section 4.2.2.3, ALU Function registers, for details on the Word Count Error Plus and Minus registers, 0146 (Hex) respectively.)

4.6.1.6 Wrong Bus Response Error

Setting bit 8 will cause status responses (and associated data words) from the selected simulated RT to be returned on the opposite bus that the command word was received. (Not allowed if switchover is enabled for the particular RT.)

4.6.1.7 Data Word Gap Error

Bit 7 selects a gap error between data words. If a data word has this error, it will not be transmitted as a contiguous word, but will have a gap between the last word and the SYNC. The length of the gap is programmable in the Data Word Gap Error register described in Section 4.2.2.3, ALU Function registers section, at address 0152 (Hex).

4.6.1.8 Error in Status Word and Command Word

The remaining two bits are used to determine which command and status words are to contain selected errors. The data words are enabled in the Error Generation Word Register.

4.6.2 Error Generation Words

Both MRT and BC Modes have two 16-bit registers in their control block (for a total of 32-bits) associated with data word error selection. Each bit in the two registers corresponds to one data word. If that bit is set to a logic "one", the DW will contain the errors selected. Register 1 corresponds to the first 16 data words with bit "zero" (LSB) corresponding to data word 1 and bit 15 (MSB) corresponding to data word 16. The second register corresponds to data words 17 to 32 in the same manner. Any combination of data words may be selected. Figure 4.6.2-1 demonstrates the error selection.

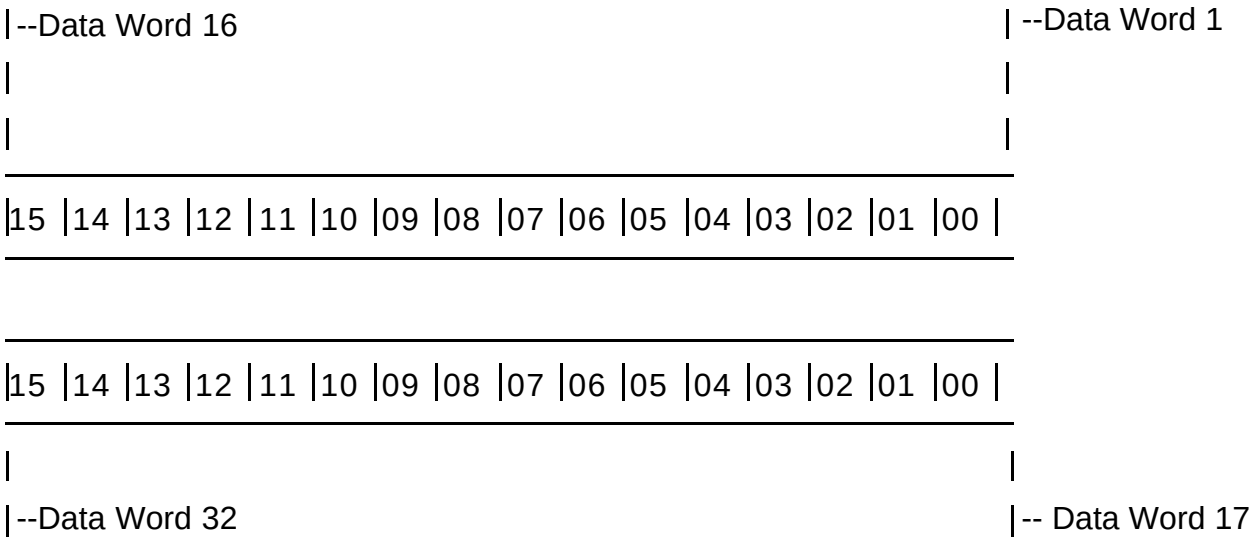


Figure 4.6.2-1. Error Generation Words

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
*****************
*    CAUTION    *
*****************
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

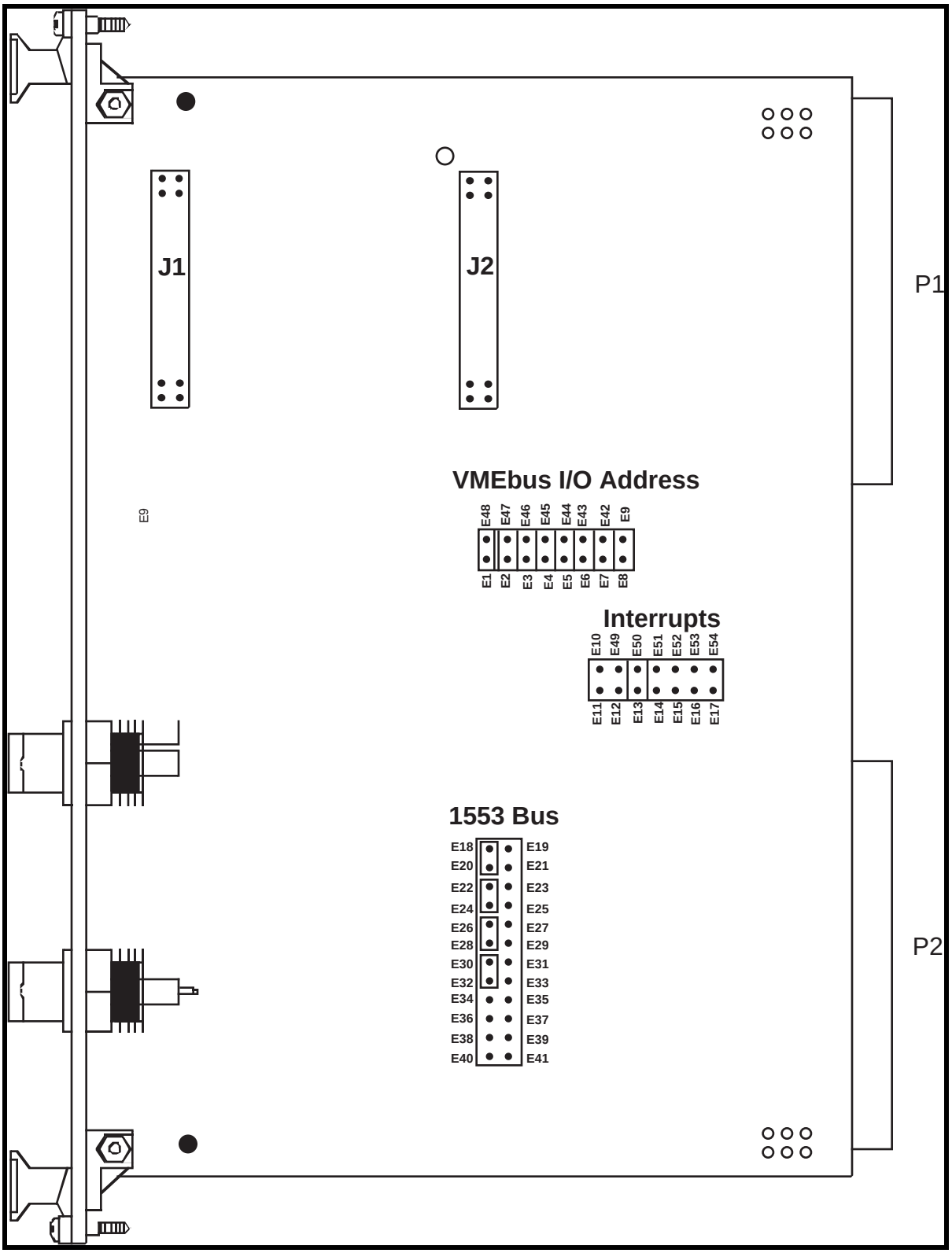
```
*****************
*    CAUTION    *
*****************
```

DO NOT INSTALL OR REMOVE BOARD WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 JUMPER INSTALLATIONS

Figures 5.3-1 shows the layout of jumpers on the MIL-STD-1553 Communications Interface. The following paragraphs describe in detail the position and function of the jumpers.



(Factory Default Shown)

Figure 5.3-1. VMIVME-6000 Jumper Location

5.3.1 VMIVME-6000 Short I/O Base Address Header

Headers E1 through E9 and E42 through E48 of the VMIVME-6000 allow the user to select the base address of the I/O configuration registers on the VMEbus. The board has 16-word length register locations that are accessible by the host. These registers may be mapped in the Short I/O space of the VMEbus, in 64-byte increments. Note that bits 14 and 15 are always a logic "one", such that the lowest allowable address in the short I/O space is C000H.

The figure below shows the configuration of the address header, which will be mapped at the factory to address C000H. The header is configured such that an OPEN connection constitutes a logic "one" and a jumper (CLOSED) connection to E9 or E42-E48 (GND) represents a logic "zero".

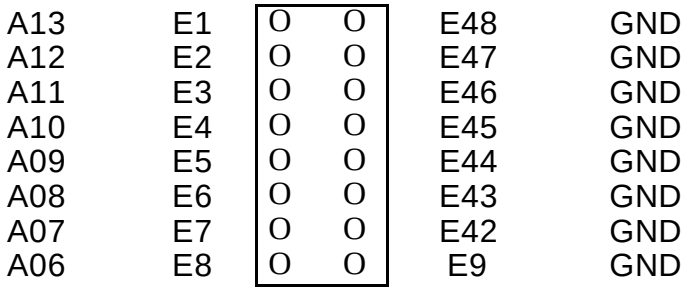
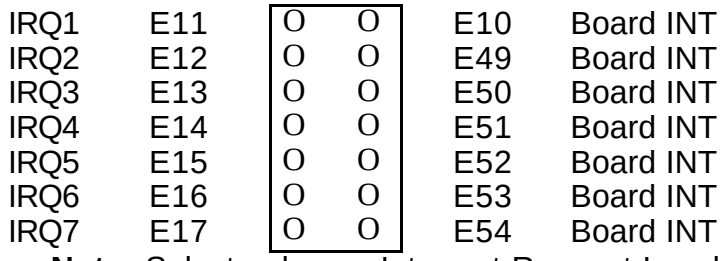


Figure 5.3.1-1. VMIVME-6000 Address Header

5.3.2 Interrupt Request Header

Headers E10 through E17 and E49 through E54 determine the interrupt request level to be used by the VMIVME-6000. Bits 2-4 of the I/O Control Register are used to program the corresponding interrupt acknowledge level that will be compared with address lines A01 - A03 during an interrupt acknowledge cycle.



Note: Select only one Interrupt Request Level

Figure 5.3.2.1. Interrupt Request Header

Table 5.3.2-1. VMIVME-6000 Interrupt Level Header

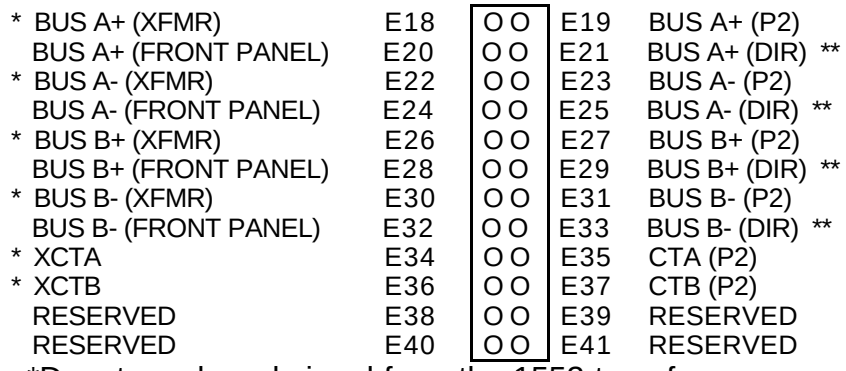
IRQ LEVEL	A01	A02	A03
IRQ1	1	0	0
IRQ2	0	1	0
IRQ3	1	1	0
IRQ4	0	0	1
IRQ5	1	0	1
IRQ6	0	1	1
IRQ7	1	1	1

5.3.3 1553 Bus Header

Headers E18 through E41 allow the user to configure the 1553 bus of the VMIVME-6000 to connect with the user-defined pins ROW C of the VMEbus P2 connector, or with the front panel connector. The figure below describes the options for the connection of the 1553 bus to the P2 connector or front panel connector.

Figure 5.3.3-2 demonstrates how to jumper the board for direct coupled operation and Figure 5.3.3-3 demonstrates transformer coupled operation. An electrical diagram is followed by the proper jumper orientation for each configuration.

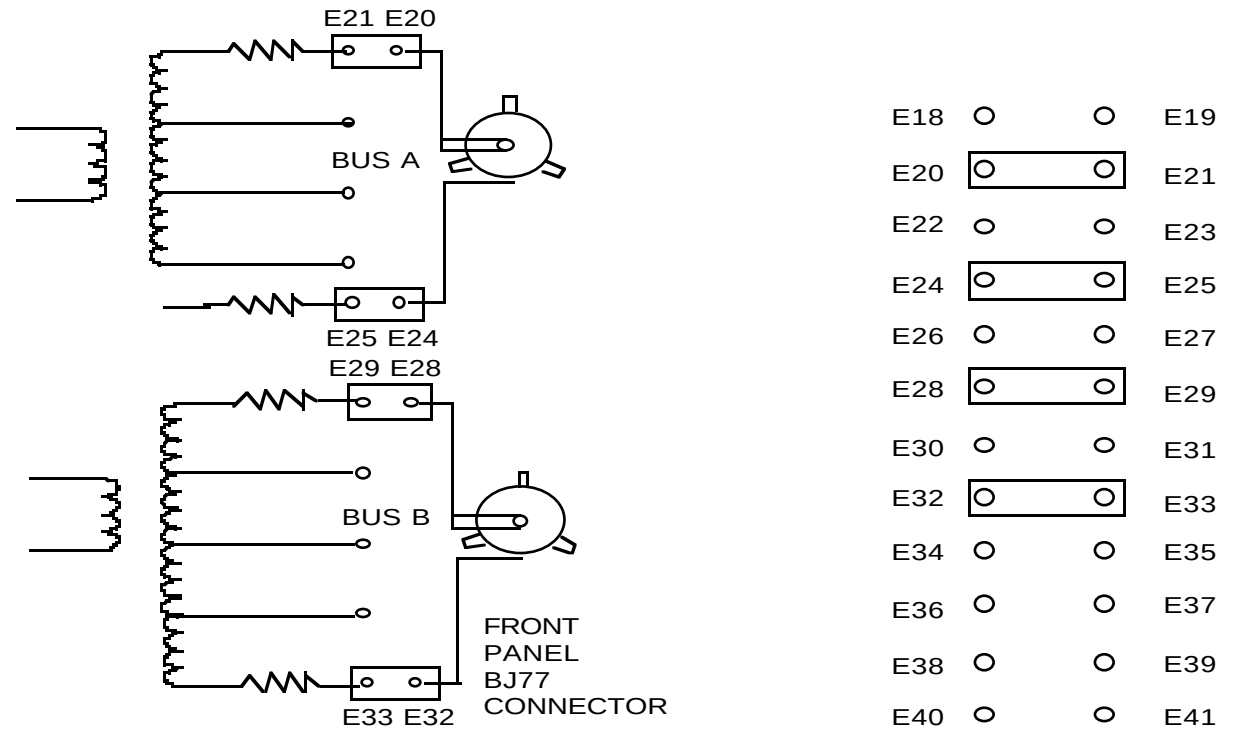
Figure 5.3.3-4 shows the configuration of the last four jumper positions (E34 through E41) of the 1553 Bus configuration header. Header positions E34/E35 and E36/E37 bring out the coupling transformer secondary center taps to the VMEbus P2 connector. The header positions marked RESERVED (E38/E39 and E40/E41) allow the coupling transformer primary center taps to be grounded.



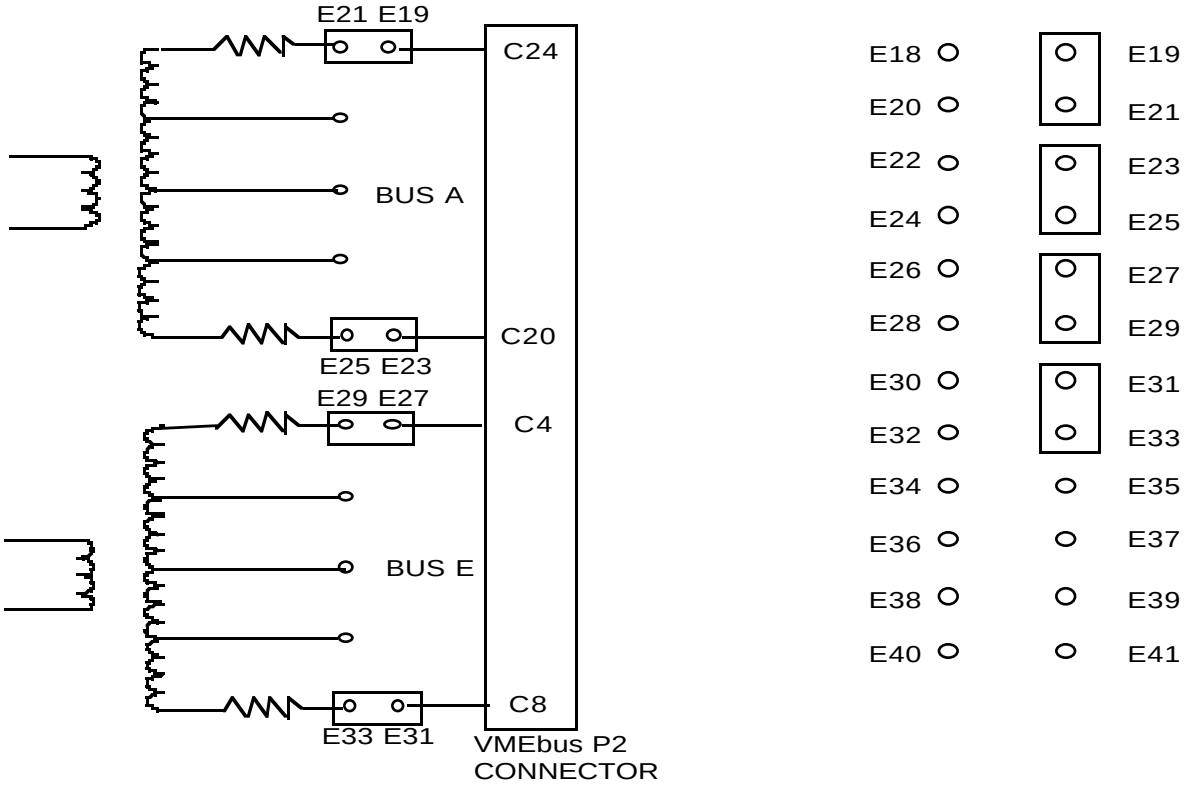
*Denotes a board signal from the 1553 transformer.

**Denotes a board signal from the 1553 isolation resistors.

Figure 5.3.3-1. VMIVME-6000 1553 Bus Header



DIRECT COUPLED THROUGH FRONT PANEL CONNECTOR



DIRECT COUPLED THROUGH VMEbus P2 CONNECTOR

M6000/F5.3.3-2

Figure 5.3.3-2. Direct Coupled Jumper Settings

5.3.4 Transformer Center Tap Jumpers

The Coupling Transformer Center Tap Jumpers are shown in Figure 5.3.4-1. These jumpers are used in allowing different types of transceivers to be used in coupling the board to the MIL-STD-1553 bus. These jumpers should always be open for the VMIVME-6000.

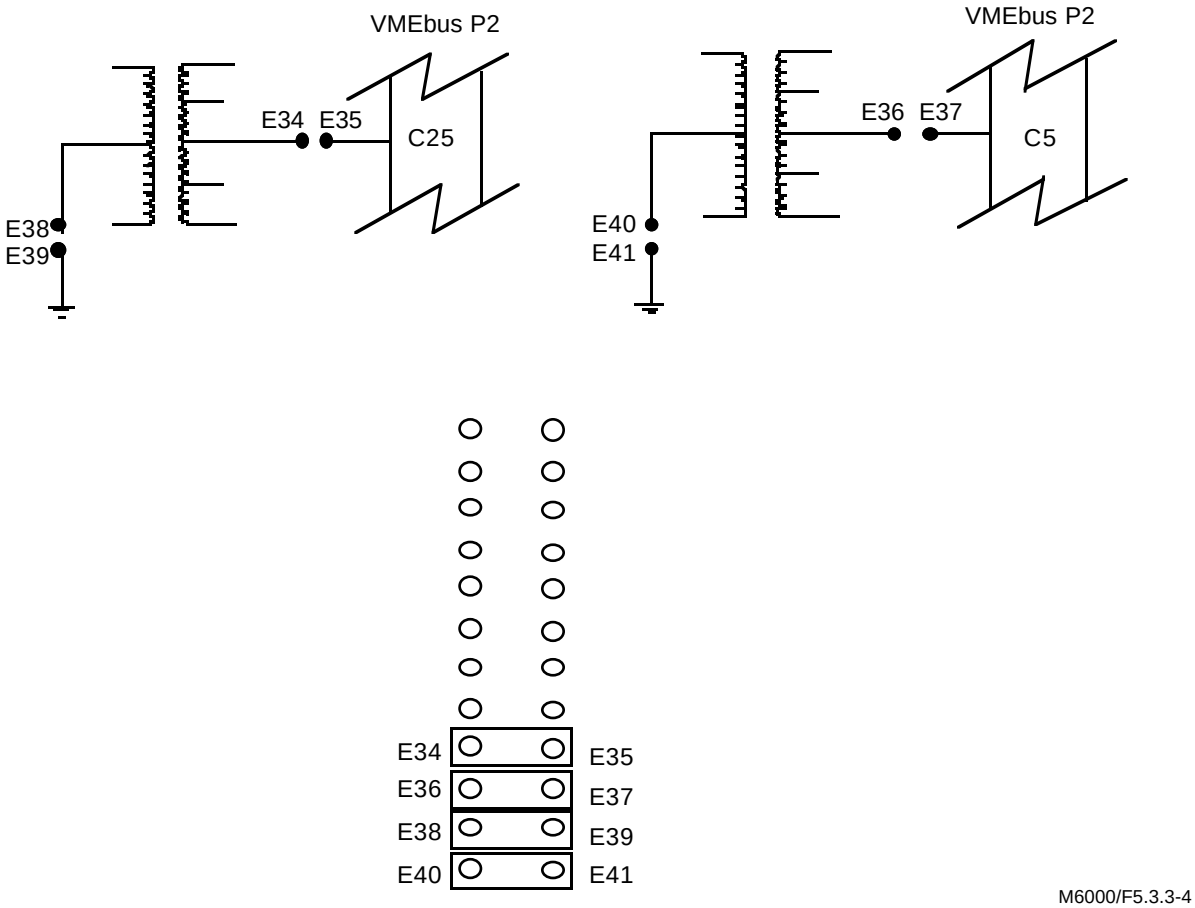


Figure 5.3.4-1. Coupling Transformer Center Tap Jumpers

5.4 MIL-STD-1553 CABLES

Cable requirements are given in the MIL-STD-1553B specification.

5.5 CABLE CONNECTOR

The VMIVME-6000 uses Trompeter Electronics, Inc., BJ-77 type twinax/triax connectors on the front panel for connection to the MIL-STD-1553 bus when this option is chosen. The connectors supply direct or transformer coupled stubs and should be connected to a bus as recommended by MIL-STD-1553B.

The connectors' center pin will be positive during the first half of the Command SYNC and are attached to the "high" side of the isolation transformer.

Table 5.5-1 provides names for the Test Point J1 connector. The connector consists of two rows of pins labeled rows (1 through 25) and (26 - 50).

Table 5.5-1. Pin Assignments for the J1 Test Point Connector

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	26	GND
2	SY0	27	MD01
3	SY1	28	MD02
4	SY2	29	MD03
5	GND	30	MD04
6	SY3	31	MD05
7	SY4	32	MD06
8	GND	33	MD07
9	SY5	34	MD08
10	SY6	35	MD09
11	GND	36	MD10
12	SY7	37	MD11
13	SY8	38	MD12
14	GND	39	MD13
15	SY9	40	MD14
16	SY10	41	MD15
17	GND	42	MD16
18	SY11	43	MD17
19	SY11L	44	MD18
20	GND	45	MD19
21	PD	46	MD20
22	JZ	47	MD21
23	GND	48	MD22
24	MD00	49	MD23
25	GND	50	GND

M6000/T5.5-1

Table 5.5-2 provides names for the Test Point J2 connector. The connector consists of two rows of pins labeled rows (1 through 25) and (26 - 50).

Table 5.5-2. Pin Assignments for the J2 Test Point Connector

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	26	GND
2	WRITE	27	ENA1LB
3	RESET	28	ENA1HB
4	BA03	29	DATAL
5	AS	30	DATAH
6	DS0	31	RAMEN
7	DS1	32	RAMDIR
8	DACK	33	SYSCLK
9	HTESTW	34	RDYD
10	EDTESTW	35	AMEN
11	LDCLK	36	RAMADD
12	MCLK	37	IOQ
13	MASTER	38	IACKIN
14	RAMEXT	39	WELB
15	STRBA	40	WEHB
16	STRBD	41	INTCYC
17	TEST	42	TSTCLK
18	MMATCH	43	ADDSTR
19	IMATCH	44	RW
20	IOEN	45	CS
21	ENA2	46	INTACK
22	DATENHB	47	ADDRESS
23	DATENLB	48	RAMADDR
24	DIR	49	ADEN
25	GND	50	GND

M6000/T5.5-2

Table 5.5-3 provides names for the "1553 Bus B" J3 connector. The BJ77 connector consists of a center conductor, an outer conductor, and a shield. The location of the J3 connector is shown in assembly drawing 132-006000-000.

Table 5.5-3. 1553 Bus "B" J3 Connector

Conductor	Signal Name
Center	BUSBF
Outer	BUSBFL
Shield	Chassis

M6000/T5.5-3

Table 5.5-4 provides names for the "1553 Bus A" J4 connector. The BJ77 connector consists of a center conductor, an outer conductor, and a shield. The location of the J4 connector is shown in assembly drawing 132-006000-000.

Table 5.5-4. 1553 Bus "A" J4 Connector

Conductor	Signal Name
Center	BUSAF
Outer	BUSAFL
Shield	Chassis

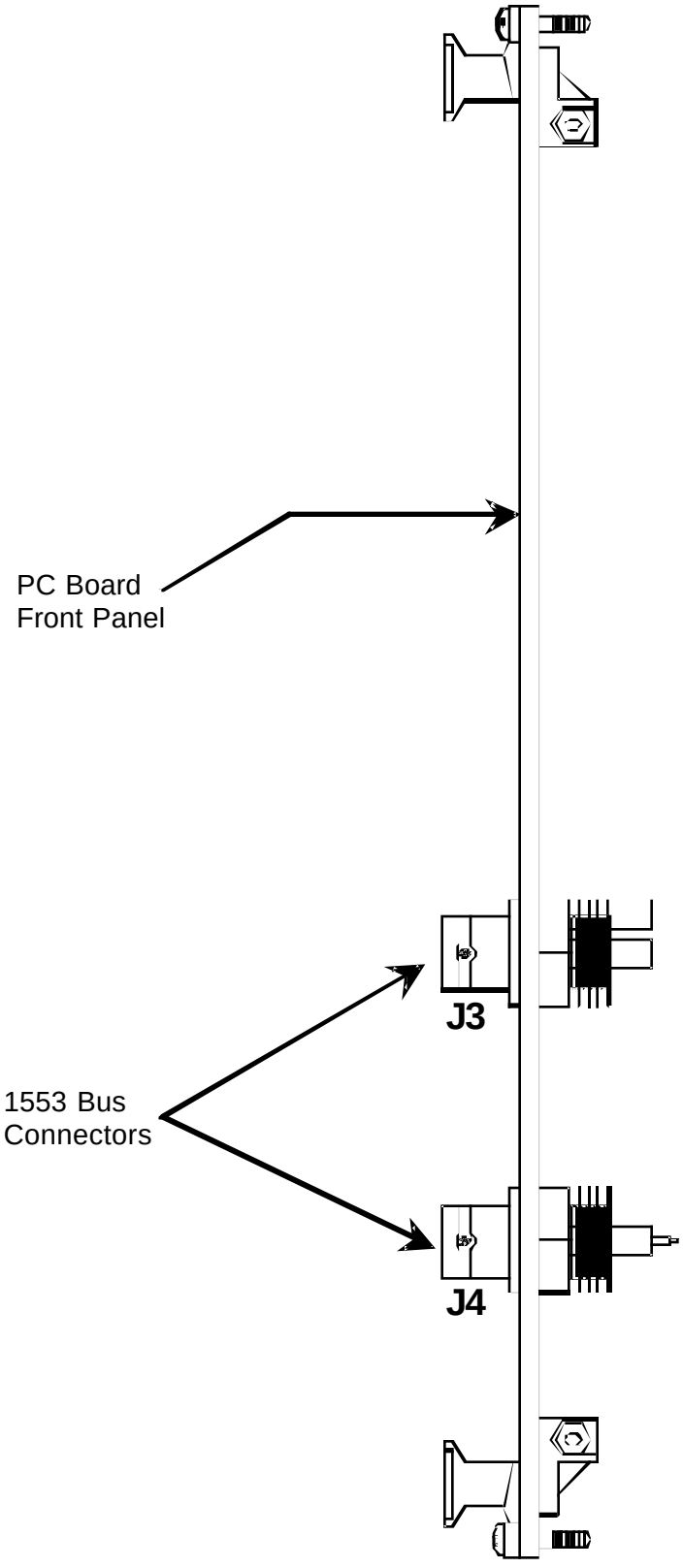
M6000/T5.5-4

Note

The signal names ending in "L" indicate the inverted bus signals.

Note

A connection to the "Scope SYNC" output of the VMIVME-6000 is available at "E-Pad" E58, and a signal "Ground" connection is available at "E-Pad" E57, as shown in assembly drawing 132-006000-000.



M6000/F5.5-1

Figure 5.5-1. 1553 Bus Connector

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

APPENDIX B

PROGRAMMING EXAMPLES

PROGRAMMING EXAMPLES

The following paragraphs give examples of how to configure the VMIVME-6000 for operation. The paragraphs are given in the sequence that they should be performed.

POWER-UP RESET

On Power-up, the VMIVME-6000 should receive a hardware System Reset from the host bus/processor. This reset, and the software reset available in the configuration control register, will reset all internal VMIVME-6000 logic and cause the chips to perform an internal self-test. The self-test will be completed within 10 msec. The results of the test will be available to the host in the ASR, and should be read by the host to examine the condition of the VMIVME-6000 before programming. The VMIVME-6000 may also be "halted" by software by setting bit 15 of the Host ASIC Hardware Control register.

CLEARING VMIVME-6000 INTERNAL REGISTERS

After the VMIVME-6000 passes the internal self-test, or when changing modes of the VMIVME-6000, the Internal Registers should be cleared by the firmware. This is accomplished by performing the CLEAR board XIO. The CLEAR board XIO is initiated by writing an 88 (Hex) to the VMIVME-6000 XIO Address register, then writing any data pattern to the XIO Data Register. This will cause the VMIVME-6000 to clear all of the VMIVME-6000 Internal registers. When the VMIVME-6000 has completed the CLEAR, it will set bit 11 of the ASR. The CLEAR command will take approximately 1 msec to complete.

INITIALIZING THE VMIVME-6000 ON-BOARD MEMORY

Before the host can access the on-board memory of the VMIVME-6000, the starting address of the memory must be programmed in the Configuration Offset register (0006H), and the memory must be enabled by setting bit 15 of the Configuration Control and Status register (0004) to a logic "one". Details on both of these registers is given in Section 4.1.1.

ESTABLISHING OPERATIONAL PARAMETERS

Before entering any mode of operation, the VMIVME-6000 must have certain parameters programmed to define basic operation. The needed options to be used such as DMA timeout, time tag increments, error injection, etc., must also be defined before operation is started. These basic and optional parameters are defined in the Special Function and ALU Internal register assignments (Figures 4.1.2.2-1 and 4.1.2.3-1), and are programmed by the host using XIO. The **only** locations that must be programmed for operation are the Control Block Address and Control Block Map.

These locations will be used by the VMIVME-6000 as the address in the VMIVME-6000 on-board memory of the first BC/SIM or MRT/MON Control Block. The Control Block Address is programmed by the host as follows:

a. Write the XIO address of the CB Address Register (100H) to the XIO Address register.

b. Write the starting address of the Control Block to the XIO Data register.

c. Poll the ASR and wait for bit 11 to be set to "one".

d. Read the ASR again to clear bit 11.

All other writes to internal ALU registers are performed in the same manner, except the address in step a) will be different.

CONTROL BLOCK/DATA BLOCK STRUCTURES

After the basic and optional parameters are selected, the operation control and data blocks must be constructed. The following sections show example control and data block structures for the VMIVME-6000 that would be constructed in the VMIVME-6000 128 k x 16-bit memory.

Bus Controller Control Block Example

Byte Address	HEX Value		Description
20	0010	Control Word 1	; BC-to-RT, A bus, Scope SYNC.
22	8000	Control Word 2	; (Stop bit set).
24	0000	Link	; Link, don't care because of STOP bit.
26	0000	Data Map	; Address of
28	1000	Data Pointer	Data for this message.
2A	0020	Rsp Tmout/DWCNT	; Default Timeout./32 Data words.
2C	0000	Intermessage Gap	; Default 30 μsec.
2E	0000	Reserved	
30	0000	ISR	; Posted by the board.
32	0000	TSR	; Posted by the board.
34	0820	Command Word 1	; TA=1, TR=0, SA=1, WC=32.
36	0000	Status Word 1	; Posted by the board.
38	0000	Command Word 2	; Not used in BC-to-RT.
3A	0000	Status Word 2	; Not used in BC-to-RT.
3C	0000	Response Time	; Posted by the board.
3E	0000	SW Interrupt Mask	; No SW INT Mask.
40	0000	Trans SW INT Mask	; No XMIT SW Mask.
42	8000	A Interrupt Mask	; Interrupt on Transmission error.
44	1000	B Interrupt Mask	; Interrupt at End of Message.
46	0000	Err. Gen. Selects	; No Error Generated.
48	0000	Err. Gen. Words	; Words 16-1.
4A	0000	Err. Gen. Words	; Words 32-17.
4C	0000	Auto Retry TSR	; Not using Auto Retry.
4E	0000	Auto Retry SW	; Not using Auto Retry.
50	0000	Reserved	
52	0000	Reserved	
54	0000	Reserved	
56	0000	Reserved	
58	0000	Branch Mask 1	; No Branching.
5A	0000	Branch Address	; No Branching.

Bus Controller Data Block Example

Data Buffers Byte Address	HEX Value	Description
1000	AAAA DW 1	; Message 1 data buffer.
	• • •	
103E	5555 DW 32	; Message 1 data buffer.

MRT/MON Header Block Example

Byte Address	Hex Value	Description
2000	0000 Control Word	; Programmed in the RT Block.
2002	0001 RT count	; 1 RT Control Block.
2004	0000 Not Used	; This location is unused.
2006	0000 Err. Gen. Sel	; No errors generated.
2008	0000 Err. Gen. Words	; Words 16-1.
200A	0000 Err. Gen. Words	; Words 32-17.
200C	0000 Not Used	; This location is unused.
200E	0000 Ring Buff Begin	; Not used when SIM RT.
2010	0000 Ring Buff End	; Not used when SIM RT.
2012	0000 Ring Map Begin	; Not used when SIM RT.
2014	0000 Ring Map End	; Not used when SIM RT.
2016	0080 AINT Mask	; AINT on ILLEGAL CMD.
2018	8000 BINT Mask	; BINT on TRANS ERROR.
201A	0010 DMA Disable	; Disable New Pointer DMA.
201C	0000 MC En 15-0	; MC. 15-00 not enabled.
201E	0000 MC En 31-16	; MC. 31-16 not enabled.
2020	0000 Reserved	

MRT/MON RT and SA Control Blocks Examples

Byte Address	Hex Value	Description
2022	0200 RT Control Word	; Normal 1553B RT (Simulated).
2024	0006 Terminal Address	; TA = 6.
2026	0000 SW skeleton	; SW Response.
2028	0000 Err. Gen. Sel.	; No errors generated.
202A	0000 Err. Gen. Words	; No errors.
202C	0000 Err. Gen. Words	; No errors.
202E	0000 Reserved	
2030	0000 Data Map	; Data in page 0.
2032	0000 Not Used	
2034	0000 Not Used	
2036	0000 Not Used	
2038	0000 AINT mask	; Interrupts in Header.
203A	0000 BINT mask	; Interrupts in Header.
203C	0000 DMA Disable	; IN MRT Header.
203E	0000 MC En 15-0	; No mode codes.
2040	0000 MC En 31-16	; No mode codes.
2042	0000 Reserved	
Subaddresses for RT 1:		
2044	3000 Data Ptr/SA Opt	; Receive SA=0.
2046	0000 Reserved	
2048	0000 SA Flags	
204A	4000 Data Ptr/SA Opt	; Receive SA=1.
204C	0000 Reserved	
204E	0000 SA Flags	
Subaddress 11111:		; Subaddress 31 with the T/R=1.
21BE	5000 Data Ptr/SAOpt	; Transmit SA=0.
21C0	0000 Reserved	
21C2	0000 SA Flags	
NOTE: An RT Control Block along with its 64 SA blocks must be set up for each RT to be Simulated/Monitored by the VMIVME-6000.		

MRT/MON Data Blocks Example

Word	HEX Value	Description
3000	0000	New Data Pointer (Disabled in MRT Header)
3002	0000	Command Word (CW)
3004	0000	Reserved
3006	0000	Reserved
3008	0000	Reserved
300A	0000	Reserved
300C	0000	Reserved
300E	0000	Gap Time
3010	0000	Time Tag MS
3012	0000	Time Tag LS
3014	0000	ISR
3016	0000	TSR
3018	Data Word 1	
	|	
	Data Word 32	

STARTING/STOPPING THE VMIVME-6000

After the basic and optional registers have been programmed, and the control and data blocks have been constructed, the VMIVME-6000 may be started in the selected mode of operation. Before starting the VMIVME-6000, the host should read the ASR to clear bit 11 if it was set from a previous XIO. Then to **start** the board, the host should write 80H to the XIO Address Register. The desired mode of operation should then be written to the XIO Data Register. (Figure 4.2-1 shows values assigned to the particular modes). The host may then poll the mode bits of the ASR to see when the mode is reflected in this location. When the applicable mode is written by the VMIVME-6000 into the Mode location of the ASR, the VMIVME-6000 will be completely initialized and operational.

To **stop** the VMIVME-6000 while it is operational, the host should issue an Orderly Shutdown XIO, (i.e., write 8AH to XIO Address register, then write any data pattern to the XIO data register). The VMIVME-6000 will reflect OFF mode in the mode bits of the ASR when the shutdown is completed.

APPENDIX C

GLOSSARY OF TERMS

	Definitions	Page
MON	Monitor	3-1
Manchester Encoding		4-10
Time Tag		4-10
Dynamic BC	Dynamic Block Control	4-10
ALU	Arithmetic-Logic Unit	4-8
ISR	Interrupt Status Register	4-10
ASR	Active Status Register	4-9
TSR	Transmission Status Register	4-15
MRT/MON	Multiple Remote Terminal/Monitor	4-65
LSW	Least Significant Word	4-11
MSW	Most Significant Word	4-11
XIO	External Input/Output	4-34
Diagmode	A Self-Test in which the host controls	4-38
DMA	Direct Memory Access	4-39
Parity	Equality in Quantity and Kind	4-41
TA	Terminal Address	4-41
CW	Command Word	4-41
SIM	Simulate	4-51
SW	Status Word	4-53
CB	Control Block	4-59
IGAP	Intermessage Gap	4-80
RT	Remote Terminal	4-96
Biphase		4-148
BIT	Built-In-Test	4-31
LCW	Last Command Word	4-126
LSW	Last Status Word	4-126