

# **VMIVME-2131**

## **64-bit CURRENT SOURCE/SINK DRIVER MEGAMODULE™**

### **INSTRUCTION MANUAL**

DOCUMENT NO. 500-012131-000 B

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**VME MICROSYSTEMS INTERNATIONAL CORPORATION  
12090 SOUTH MEMORIAL PARKWAY  
HUNTSVILLE, ALABAMA 35803-3308  
(205) 880-0444  
1-800-322-3616**

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## RECORD OF REVISIONS

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B	03/08/94	Cover, pages ii, and 5-3	94-0216

## **VMIC SAFETY SUMMARY**

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

### **GROUND THE SYSTEM**

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

### **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE**

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

### **KEEP AWAY FROM LIVE CIRCUITS**

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### **DO NOT SERVICE OR ADJUST ALONE**

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

### **DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM**

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

### **DANGEROUS PROCEDURE WARNINGS**

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

<b>WARNING</b>
----------------

**DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.**



# SAFETY SYMBOLS

## GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



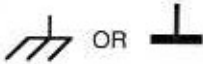
OR



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

**WARNING**

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.



The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

# VMIVME-2131

## 64-bit CURRENT SOURCE/SINK DRIVER MEGAMODULE™

### TABLE OF CONTENTS

	<u>Page</u>
<b>SECTION 1. INTRODUCTION</b>	
1.1 FEATURES .....	1-1
1.2 FUNCTIONAL DESCRIPTION.....	1-1
1.3 REFERENCE MATERIAL LIST .....	1-2
 <b>SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS</b>	
 <b>SECTION 3. THEORY OF OPERATION</b>	
3.1 OPERATIONAL OVERVIEW.....	3-1
3.2 DEVICE ADDRESSING.....	3-1
3.3 VMEbus FOUNDATION LOGIC.....	3-4
3.4 DATA TRANSFERS.....	3-4
3.5 REGISTER CONTROL LOGIC .....	3-4
3.6 CONTROL AND STATUS REGISTER (CSR).....	3-4
3.7 BUILT-IN-TEST .....	3-4
3.8 OCTAL REGISTERS AND OUTPUT DRIVERS.....	3-9
 <b>SECTION 4. PROGRAMMING</b>	
4.1 REGISTER MAP .....	4-1
4.2 REGISTER BIT DEFINITIONS .....	4-2
4.3 DETAILED PROGRAMMING.....	4-5
4.3.1 Output Data Transfers.....	4-5
4.3.2 Built-in-Test.....	4-5

## **TABLE OF CONTENTS (Continued)**

<b>SECTION 5. CONFIGURATION AND INSTALLATION</b>	<b><u>Page</u></b>
5.1 UNPACKING PROCEDURES .....	5-1
5.2 PHYSICAL INSTALLATION.....	5-1
5.3 JUMPER LOCATIONS.....	5-1
5.4 SUPPRESSOR DIODE CONNECTIONS.....	5-3
5.5 ADDRESS MODIFIERS.....	5-3
5.6 ADDRESS SELECTION JUMPERS .....	5-3
5.7 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION .....	5-3
5.8 JUMPER FUNCTIONS.....	5-11

## **SECTION 6. MAINTENANCE AND WARRANTY**

6.1 MAINTENANCE .....	6-1
6.2 MAINTENANCE PRINTS.....	6-1
6.3 WARRANTY .....	6-1
6.4 OUT-OF-WARRANTY REPAIR POLICY .....	6-2
6.4.1 Repair Category.....	6-3
6.4.2 Repair Pricing.....	6-3
6.4.3 Payment.....	6-3
6.4.4 Shipping Charges .....	6-4
6.4.5 Shipping Instructions .....	6-4
6.4.6 Warranty on Repairs.....	6-4
6.4.7 Exclusions.....	6-4

## **LIST OF FIGURES**

<b><u>Figure</u></b>	<b><u>Page</u></b>
3.1-1 VMIVME-2131 Functional Block Diagram.....	3-2
3.2-1 Address Selection Block Diagram.....	3-3
3.3-1 Control Section Block Diagram.....	3-5
3.3-2 Address Section Block Diagram.....	3-6
3.4-1 Data Transfer Block Diagram .....	3-7
3.6-1 CSR Control Logic Block Diagram.....	3-8
3.8-1 I/O Registers Block Diagram.....	3-10
3.8-2 I/O Registers Block Diagram Bank B.....	3-11



## **TABLE OF CONTENTS (Concluded)**

### **LIST OF FIGURES (Concluded)**

<u>Figure</u>	<u>Page</u>
4.3.2-1 Programming Flowchart (Built-in-Test Active).....	4-6
4.3.2-2 Programming Flowchart (Built-in-Test Not Active).....	4-7
5.3-1 Jumper Locations Showing Factory Configuration.....	5-2
5.4-1 Typical Output Driver Stage.....	5-4
5.6-1 Data Register Base Address Select Jumpers .....	5-5
5.6-2 CSR Base Address Select Jumpers .....	5-6
5.7-1 P3/P4 Connector - Pin Configuration.....	5-7
5.7-2 Cable Connector Configuration.....	5-10

### **LIST OF TABLES**

<u>Table</u>	<u>Page</u>
4.1-1 Output Data Register Bit Definitions.....	4-2
4.1-2 CSR Bit Definitions.....	4-4
5.7-1 Connector P4 Pin/Channel Assignments.....	5-8
5.7-2 Connector P3 Pin/Channel Assignments.....	5-9

## **APPENDIX**

- A     Assembly Drawing, Parts List, and Schematic



## SECTION 1

### INTRODUCTION

#### 1.1 FEATURES

The VMIVME-2131 is capable of delivering 64 channels of high current output. These outputs can be current sourcing or current sinking. The VMIVME-2131 is designed with a breakdown voltage of 35 V minimum. A unique feature of the VMIVME-2131 Board is the Built-in-Test (BIT) logic, which allows the user, under software control, to verify the operation of each channel.

A brief overview of the VMIVME-2131's features includes:

- a. 64 bits of high current outputs.
- b. Outputs may be current sourcing/High-Z or current source/sinks.
- c. Output transient protected.
- d. High-breakdown voltage (35 V minimum).
- e. Tri-state outputs.
- f. Built-in-Test logic for fault isolation.
- g. High reliability DIN type output connectors.
- h. 8-, 16-, or 32-bit transfers.
- i. Double Eurocard form factor.
- j.  $\pm 3.5$  A peak output current (100 msec, 10 percent duty cycle).
- k. 500 mA continuous current (fan cooled).
- l. Thermal shutdown protection.
- m. Front panel software controlled Failed LED for Built-in-Test.
- n. Separate user configurable address jumpers for the Control and Status Register (CSR) and the Data Registers allow for contiguous data addressing when more than one I/O board is used in a VMEbus system.

#### 1.2 FUNCTIONAL DESCRIPTION

The VMIVME-2131 is a member of VMIC's MEGAMODULE™ family. It is designed with common programming features such that subsystems may be configured with contiguous I/O addresses to conserve memory. Each of these boards (VMIVME-1110, VMIVME-2130, VMIVME-2131, VMIVME-2120, and VMIVME-2510) is designed with two sets of board address switches or jumpers to provide an efficient memory address map for CSR and I/O addresses. CSR addresses may be set such that all CSRs among a variety of boards in the system may be mapped into contiguous memory locations separate from the I/O data addresses.

The MEGAMODULE™ product line is designed to support 8-, 16-, and 32-bit data transfers and also features a front panel Fail LED that is illuminated at power-up or after a system reset and may be extinguished under program control

upon successful completion of board level diagnostics. Specific hardware has been designed into the VMIVME-2131 to support the Built-in-Test functions. The VMIVME-2131 supports both off-line and on-line fault detection and isolation.

### 1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specifications" is available from the following source:

VITA  
VMEbus International Trade Association  
10229 N. Scottsdale Road  
Scottsdale, AZ 85253  
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

#### **TITLE DOCUMENT NO.**

Digital Input Board Application Guide	825-000000-000
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

**SECTION 2**  
**PHYSICAL DESCRIPTION AND SPECIFICATIONS**

**REFER TO 800-012131-000 SPECIFICATION**



## SECTION 3

### THEORY OF OPERATION

#### 3.1 OPERATIONAL OVERVIEW

The VMIVME-2131 is designed for a variety of applications such as:

- a. Relay drivers.
- b. Lamp drivers.
- c. Solenoid drivers.
- d. Hammer drivers.
- e. Stepping motor drivers.
- f. Triac drivers.
- g. LED drivers.
- h. High current, high voltage drivers.
- i. Fiber-optic LED drivers.

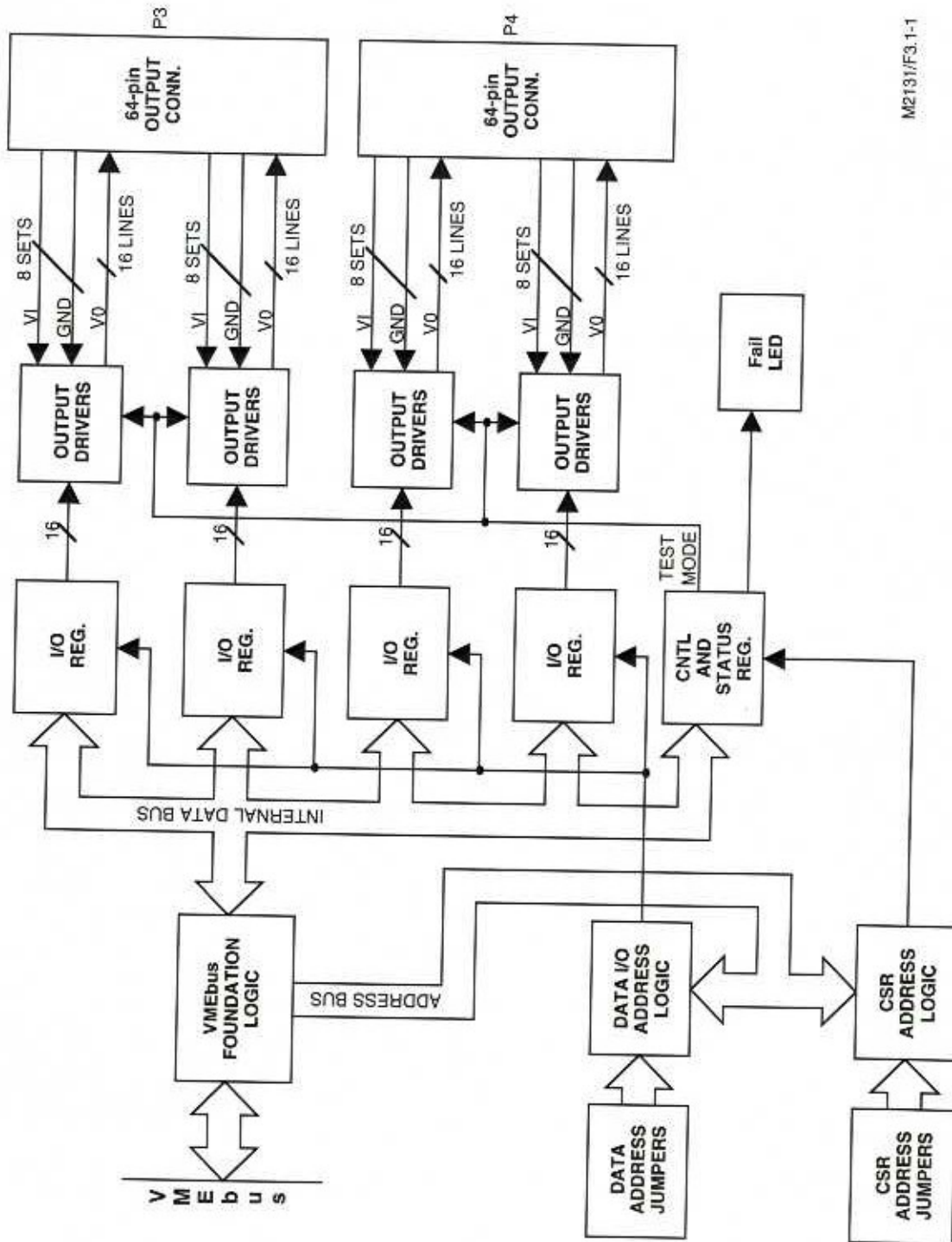
The design of the VMIVME-2131 Board, as shown in the functional block diagram in Figure 3.1-1, consists primarily of 4 sections which are:

- a. Device addressing.
- b. VMEbus foundation logic.
- c. Built-in-Test logic.
- d. Output drivers.

The board is designed using eight bi-directional 8-bit registers, a Control and Status Register (CSR), high performance output drivers, typical VMEbus foundation logic, and two device address jumper banks. The two jumper banks provide the user with the capability and flexibility to map I/O registers and CSRs into separate contiguous memory locations.

#### 3.2 DEVICE ADDRESSING

The VMIVME-2131 is designed to support data transfers in supervisory or nonprivileged short I/O memory space. Jumpers are provided, as shown in Figure 3.2-1 (Address Selection Block Diagram), to allow user selection of either I/O access type. These jumpers are called AM2. There is one jumper for the Data Registers and one jumper for the CSR. The VMIVME-2131 is factory configured (jumpers AM2 not installed) to respond to short supervisory I/O access.



M2131/F3.1-1

Figure 3.1-1. VMIVME-2131 Functional Block Diagram

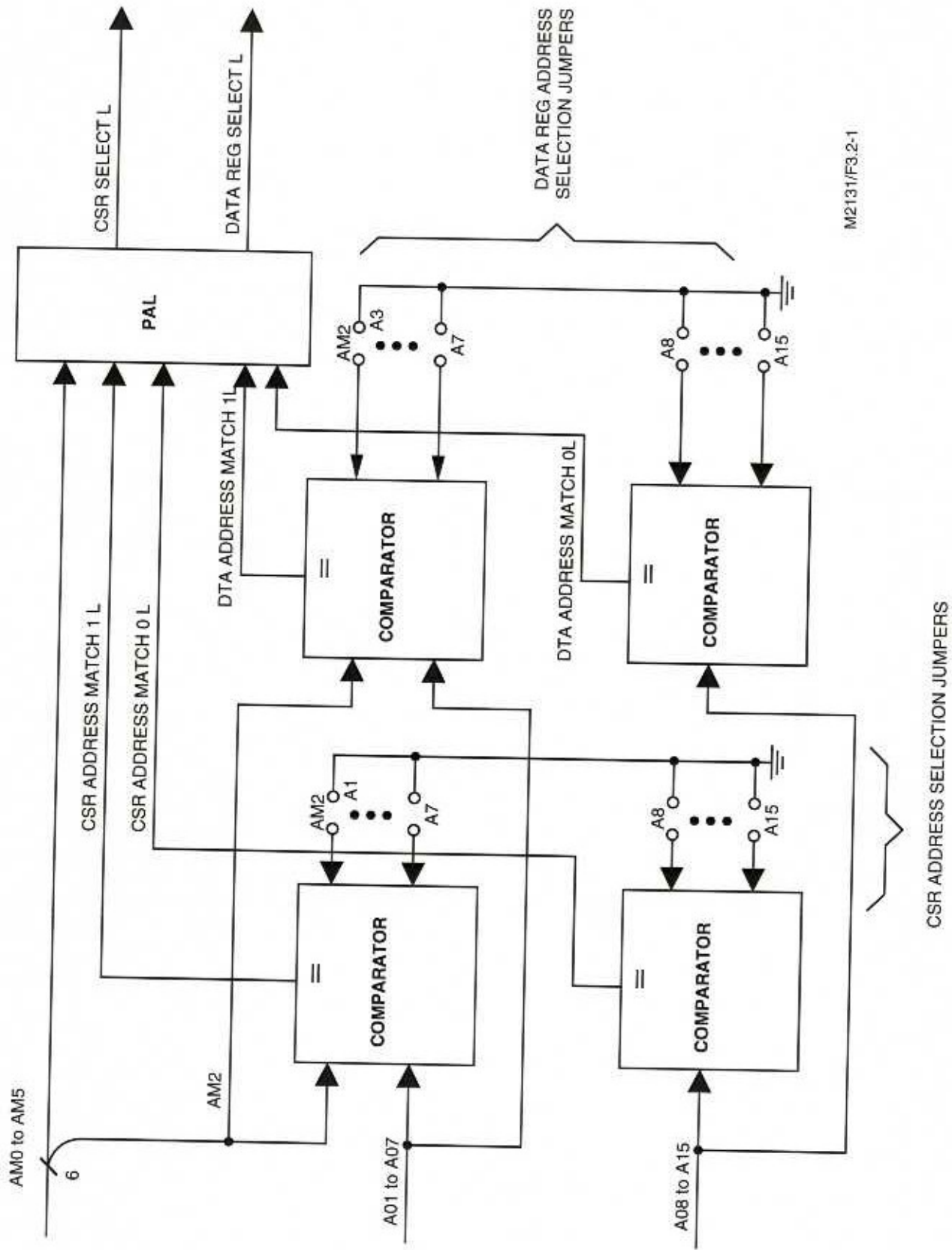


Figure 3.2-1. Address Selection Block Diagram



The VMIVME-2131 is designed with two sets of board select jumpers and decode logic as shown in Figure 3.2-1 to provide an efficient memory address map for the CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into separate contiguous memory locations when configuring subsystems that require more than one board.

### **3.3 VMEbus FOUNDATION LOGIC**

Typical VMEbus drivers, receivers, and control logic are shown in Figures 3.2-1, 3.3-1, and 3.3-2. The detailed logic design is shown on the schematic in Appendix A.

### **3.4 DATA TRANSFERS**

Data transfer transceivers are shown in Figure 3.4-1. The data transceivers are designed to support write and read operations on 8-, 16-, and 32-bit boundaries. Thus, the 64 current source/sink outputs are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes.

### **3.5 REGISTER CONTROL LOGIC**

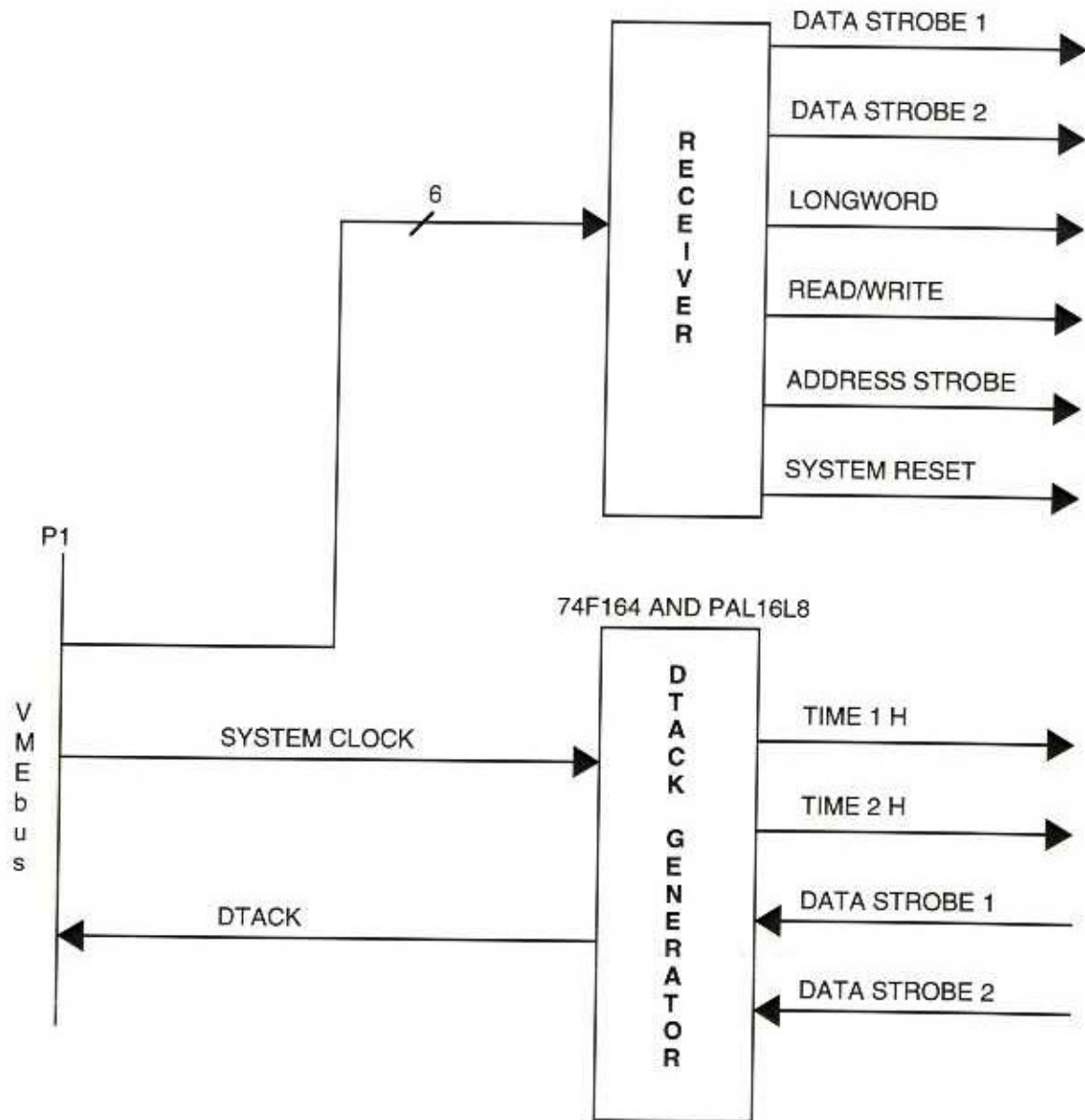
The register control logic for the VMIVME-2131 Board is designed to support write and read operations to and from the eight 8-bit bi-directional dual-port latches and write transfers to a CSR that controls the test mode and front panel LED. The control logic provides the capability to read or write 8, 16, or 32 bits of data. This control logic is implemented in PALs as shown on the schematic in Appendix A.

### **3.6 CONTROL AND STATUS REGISTER (CSR)**

The CSR is a write-only register that controls the Test Mode (TM) bit and the front panel Fail LED as shown in Figure 3.6-1. The TM bit disables the output drivers to perform Built-in-Test functions. Both bits of the CSR are initialized active upon system reset or power-up such that the driver outputs are disabled and the front panel LED is illuminated. A jumper H1 is configured such that when writing a logic "one" to bits 6 and 7 of the CSR, the LED is illuminated and the output drivers are off-line.

### **3.7 BUILT-IN-TEST**

The Built-in-Test feature of the VMIVME-2131 is enabled by asserting (setting to a logical "one") the test mode bit in the CSR. As an aid to programming the VMIVME-2131, a jumper (H1) is available to the user. This jumper can be used to invert the input data to the CSR of the VMIVME-2131. It is used to permit existing



M2131/F3.3-1

Figure 3.3-1. Control Section Block Diagram

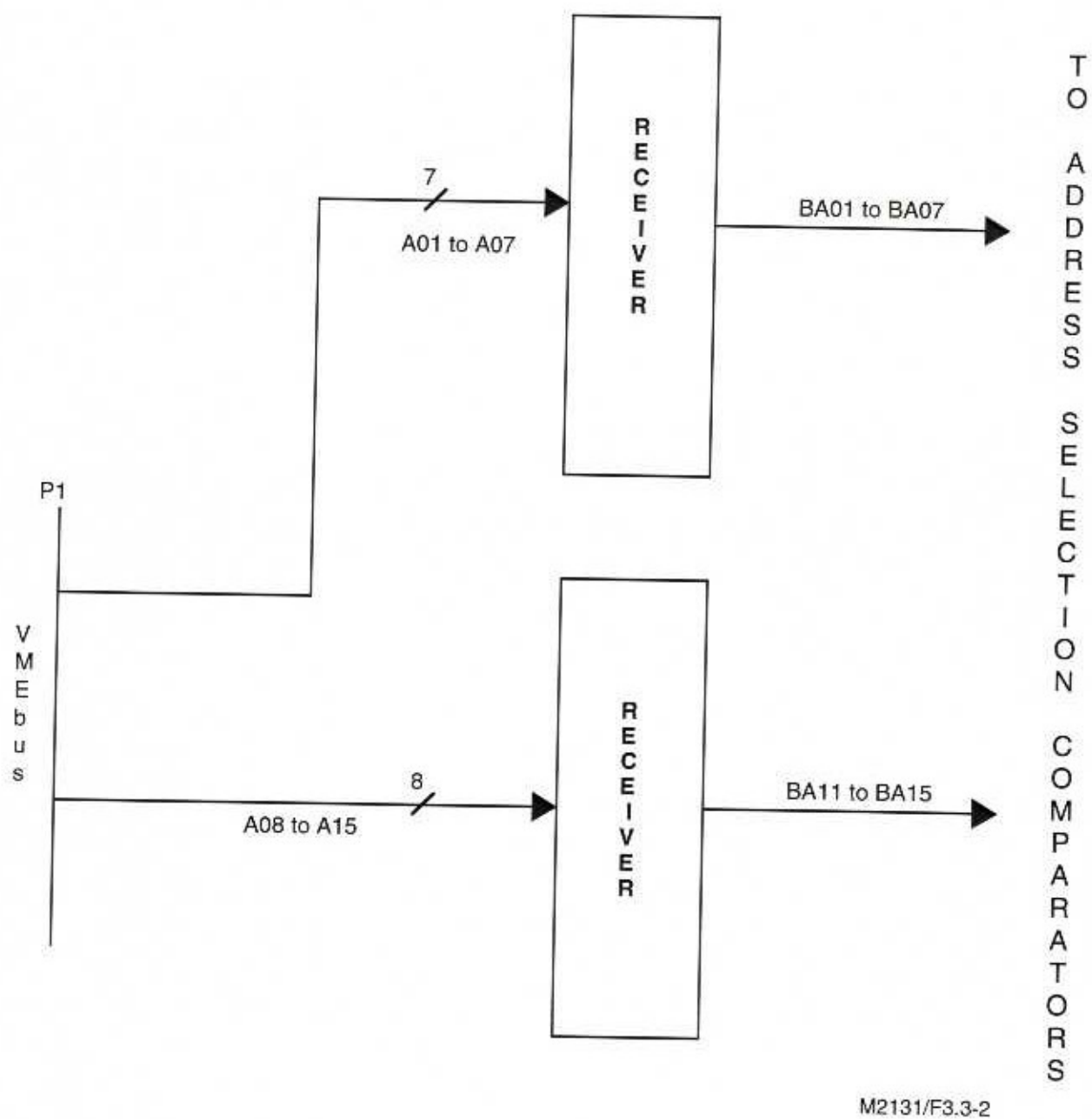


Figure 3.3-2. Address Section Block Diagram



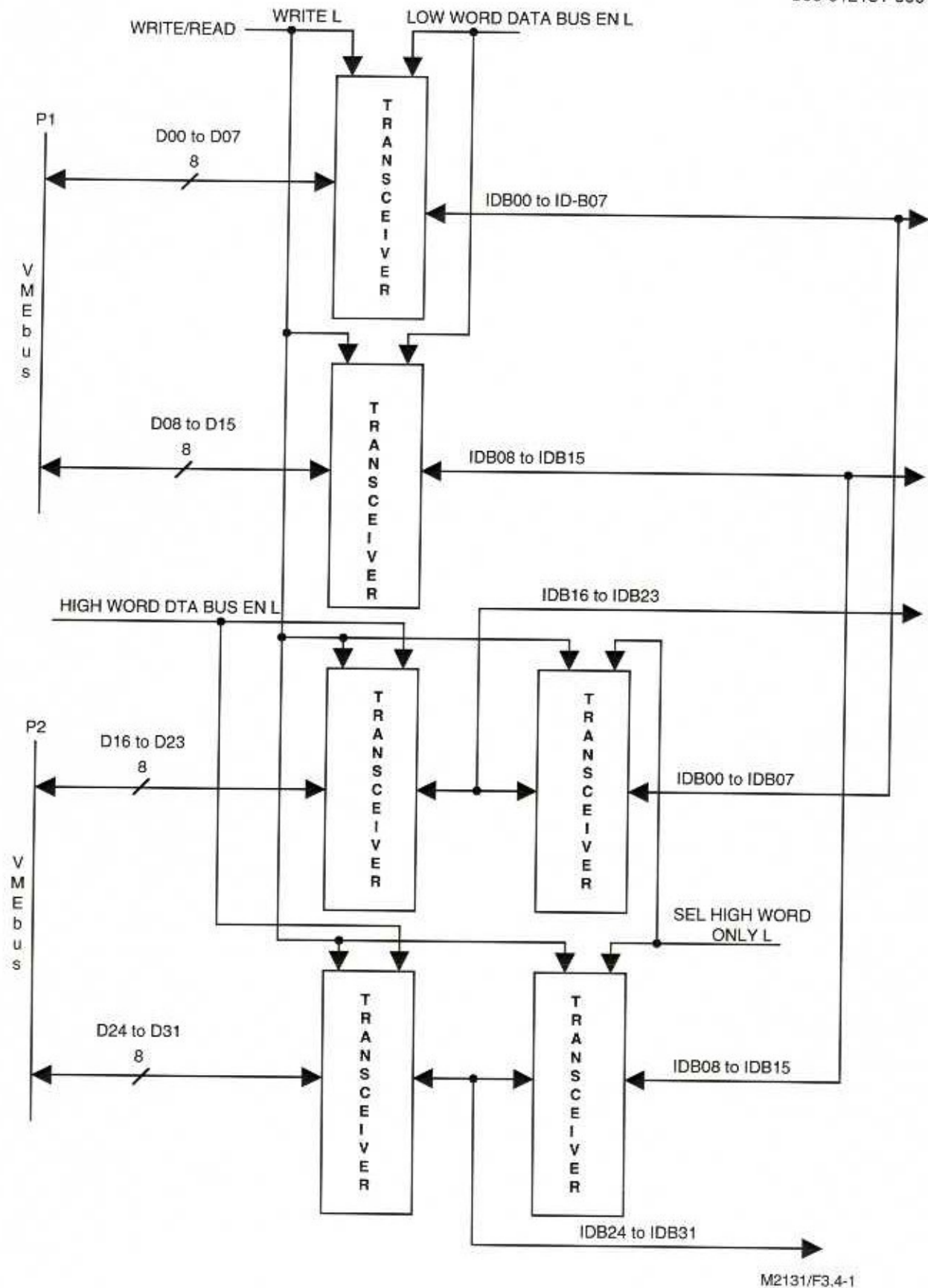
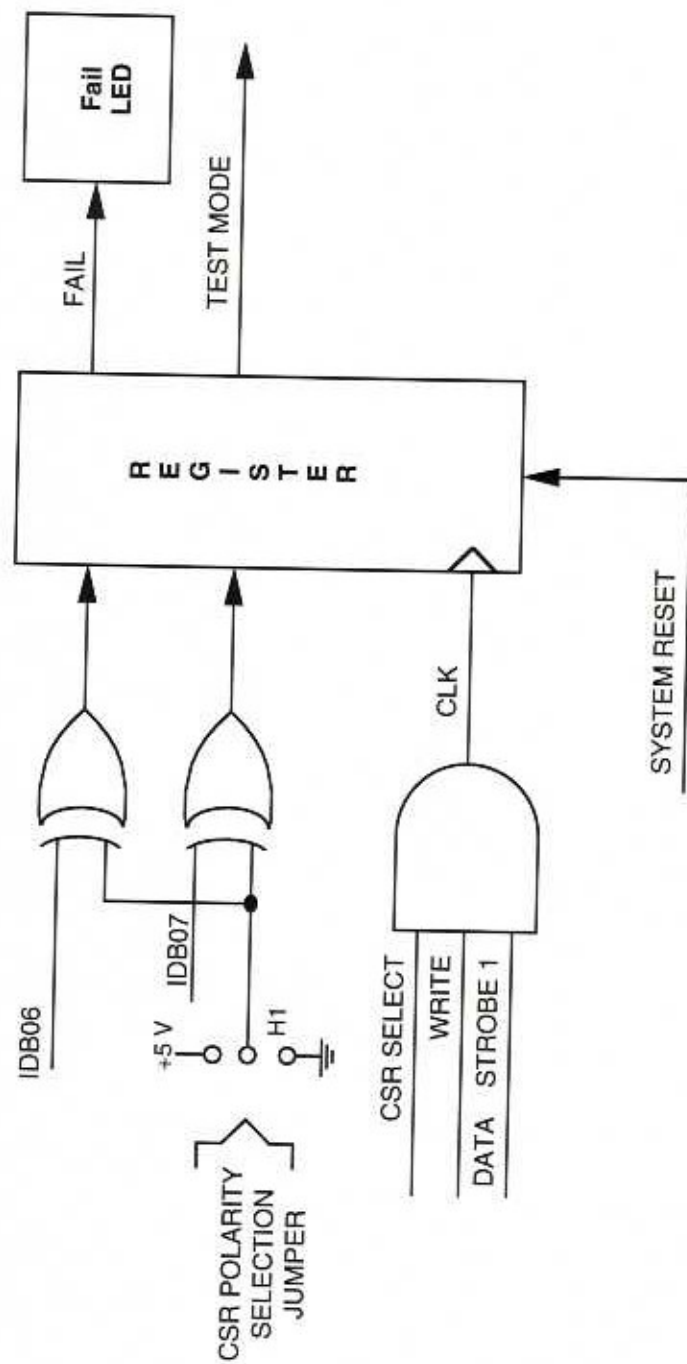


Figure 3.4-1. Data Transfer Block Diagram



M2131/F3.6-1

Figure 3.6-1. CSR Control Logic Block Diagram

software to control the VMIVME-2131. If the program used writes "zeros" to the CSR this jumper can be setup to invert this data (since the VMIVME-2131 uses "ones" in the CSR). This way the H1 jumper can let the user run existing software without modifications.

While in Test Mode, data may be written to any Output Data Register and read back on a following read operation. This way the data written can be compared to the data read and any action necessary can be initiated. While in Test Mode, writing to an output device will have no effect on the field equipment, because the output drivers are disabled during Test Mode operations.

The data loopback circuitry can be used even if TEST MODE is not active. Thus, the Built-in-Test feature of this product provides the user with the capability of performing real-time loopback testing with the output drivers connected to the field equipment.

A front panel Fail LED is provided for quick fault isolation to the board level. The Fail LED is illuminated at power-up or system reset and is extinguished under software control by the user upon successful execution of a user-defined diagnostic program. The board is initialized in the Test Mode at power-up or upon system reset.

### 3.8 OCTAL REGISTERS AND OUTPUT DRIVERS

A block diagram of the eight 8-bit I/O registers is shown in Figures 3.8-1 and 3.8-2. The Output Data Registers were selected as the primary building block of this design, because they have a unique feature that allows "read-back" of their input data, which is used by the Built-in-Test functions. In Test Mode, the Data Register outputs are tri-stated and the data read-back path is internal to the device. Whereas, during normal operation the data read-back path includes the output pins on the Output Data Register. Thus, during Test Mode all of the board's circuitry is tested, except for the output drivers.

Due to the large output currents possible, each driver pair has a separate pin for their source voltage and ground. This voltage is independent of the TTL control voltage driving the output devices. Its maximum value is determined by the output devices (UDN-2935ZH), which is 35 V. A detailed description of the output drivers is given in the product specification, Document Number 800-012131-000.

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

**THE USER SHOULD USE THE CABLE GROUND LINES FOR THE EXTERNAL POWER SUPPLY RETURNS. THIS IS REQUIRED TO PREVENT EXCESSIVE CURRENT FROM FLOWING INTO THE VMEbus BACKPLANE. ALSO, THE USER SHOULD REMOVE POWER BEFORE THE CABLES ARE CONNECTED OR DISCONNECTED (FROM THE BOARD). THIS WILL PREVENT EXCESSIVE CURRENTS FROM DAMAGING THE P3/P4 CONNECTOR PINS.**



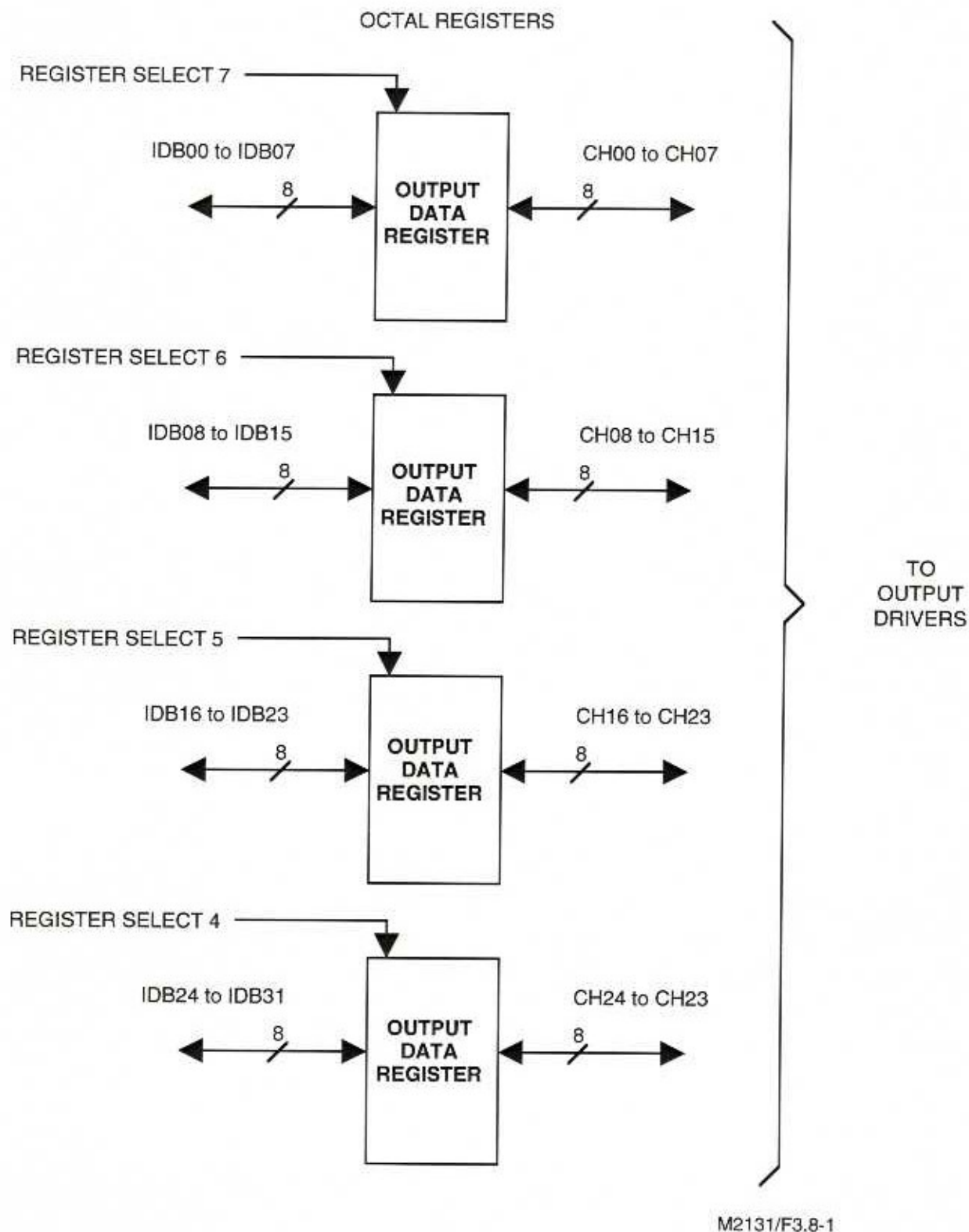


Figure 3.8-1. I/O Registers Block Diagram

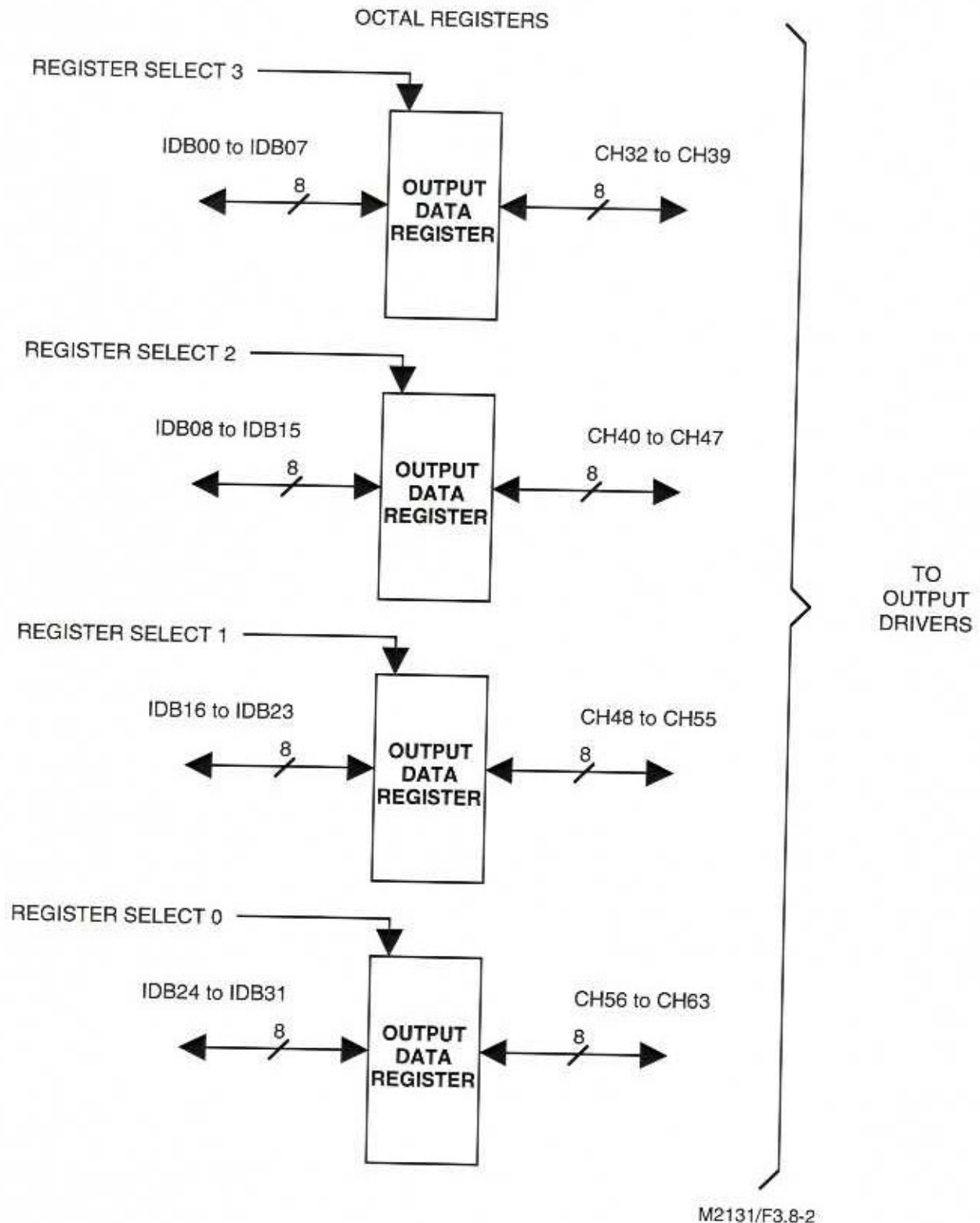


Figure 3.8-2. I/O Registers Block Diagram Bank B

## SECTION 4

### PROGRAMMING

#### 4.1 REGISTER MAP

The VMIVME-2131 contains eight 8-bit Output Data Registers and an 8-bit Control and Status Register (CSR). These Output Data Registers allow access to 64 current source/sink output channels and are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes. The Output Data Registers also support bi-directional transfers, which is used for data validation or diagnostic testing. The CSR is addressable as a 16-bit word or as two 8-bit bytes. It is a write-only register.

#### DATA REGISTERS

<u>RELATIVE ADDRESS</u>	<u>MNEMONIC</u>	<u>NAME/FUNCTION</u>
\$XXX0	DR0	DATA REGISTER 0
\$XXX1	DR1	DATA REGISTER 1
\$XXX2	DR2	DATA REGISTER 2
\$XXX3	DR3	DATA REGISTER 3
\$XXX4	DR4	DATA REGISTER 4
\$XXX5	DR5	DATA REGISTER 5
\$XXX6	DR6	DATA REGISTER 6
\$XXX7	DR7	DATA REGISTER 7

XXX of the address is determined by data register address select jumpers as shown in Section 5.

DR0 to DR7 are read/write registers.

#### CSRs

<u>RELATIVE ADDRESS</u>	<u>MNEMONIC</u>	<u>NAME/FUNCTION</u>
\$YYY0	CSRU	CSR UPPER BYTE
\$YYY1	CSRL	CSR LOWER BYTE

YYY of the address is determined by CSR address select jumpers as shown in Section 5.

The CSR is a write-only register.

## 4.2 REGISTER BIT DEFINITIONS

The following tables (Tables 4.1-1 and 4.1-2) will list and define the bits established by the output channels and the registers that contain the bits as used by the VMIVME-2131 Board.

Table 4.1-1. Output Data Register Bit Definitions

### \$XXX0 DR0

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
OUTPUT DATA REGISTERS							
OD63	OD62	OD61	OD60	OD59	OD58	OD57	OD56

### \$XXX1 DR1

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
OUTPUT DATA REGISTERS							
OD55	OD54	OD53	OD52	OD51	OD50	OD49	OD48

### \$XXX2 DR2

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
OUTPUT DATA REGISTERS							
OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40

### \$XXX3 DR3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUTPUT DATA REGISTERS							
OD39	OD38	OD37	OD36	OD35	OD34	OD33	OD32

M2131/4.1-1/1



Table 4.1-1. Output Data Register Bit Definitions (Concluded)

\$XXX4 DR4

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
OUTPUT DATA REGISTERS							
OD31	OD30	OD29	OD28	OD27	OD26	OD25	OD24

\$XXX5 DR5

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
OUTPUT DATA REGISTERS							
OD23	OD22	OD21	OD20	OD19	OD18	OD17	OD16

\$XXX6 DR6

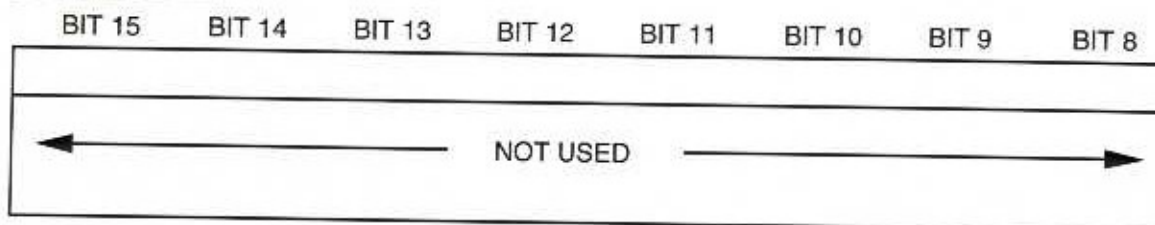
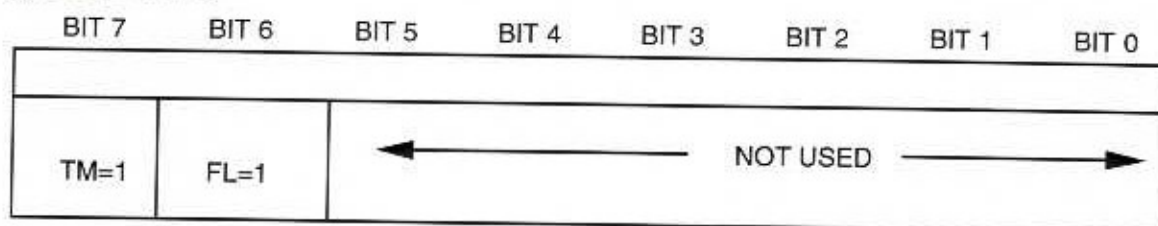
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
OUTPUT DATA REGISTERS							
OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8

\$XXX7 DR7

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUTPUT DATA REGISTERS							
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

M2131/4.1-1/2

Table 4.1-2. CSR Bit Definitions

\$YYY0 CSRU\$YYY1 CSRL

M2131/T4.1-1/2

## **4.3 DETAILED PROGRAMMING**

### **4.3.1 Output Data Transfers**

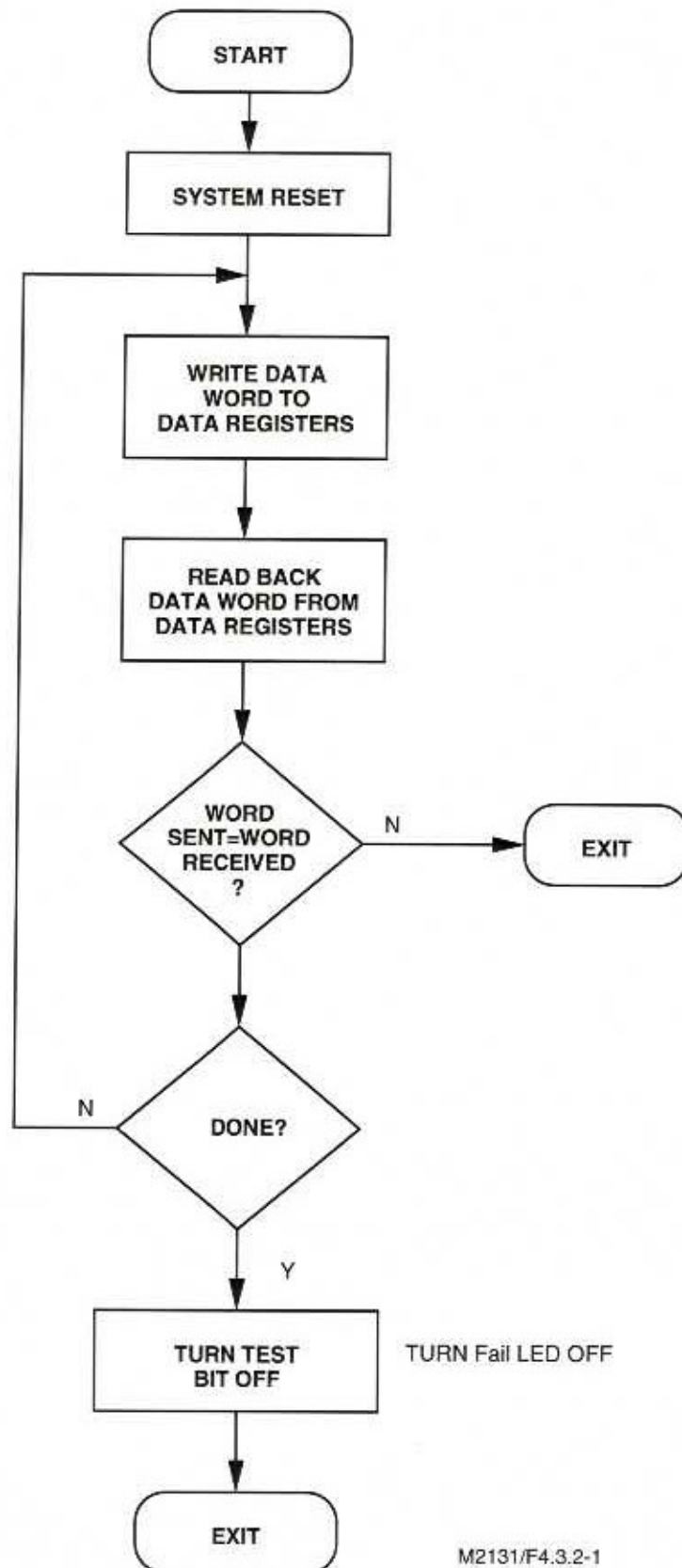
As seen in the register map in Section 4.1, DR0 to DR7 corresponds to output channels 63 to 0. By writing to these Data Registers, any output channel can be controlled.

### **4.3.2 Built-in-Test**

The Built-in-Test features of the VMIVME-2131 provide the user with the capability of real-time loop-back data verification and off-line diagnostic execution. The off-line Built-in-Test feature is initiated by setting the TM bit in the CSR to a logic "one". Test data may be written to the selected Data Register and read back on a read transfer.

At power-up or after a system reset, the Test Mode and Failed LED bits of the CSR are initialized active (a logic "one"). In Test Mode, the operator may perform diagnostic testing of the board's logic and internal registers. At the end of the diagnostic testing, and assuming the board passes, the operator needs to negate (a logic "zero") the CSR bits used to control Test Mode and the Fail LED. A simplified programming flowchart for Built-in-Test is shown in Figures 4.3.2-1 and 4.3.2-2.

The H1 jumper is set at the factory so that Test Mode is active and the LED is illuminated when a logic "one" is written to the CSR. By altering the H1 jumper (moving from +5 V to ground or from ground to +5 V), the user program can activate Test Mode and illuminate the Fail LED by writing a logic "zero" to the CSR. The configuration of H1 is option dependent and is discussed in greater detail in Section 5.8.

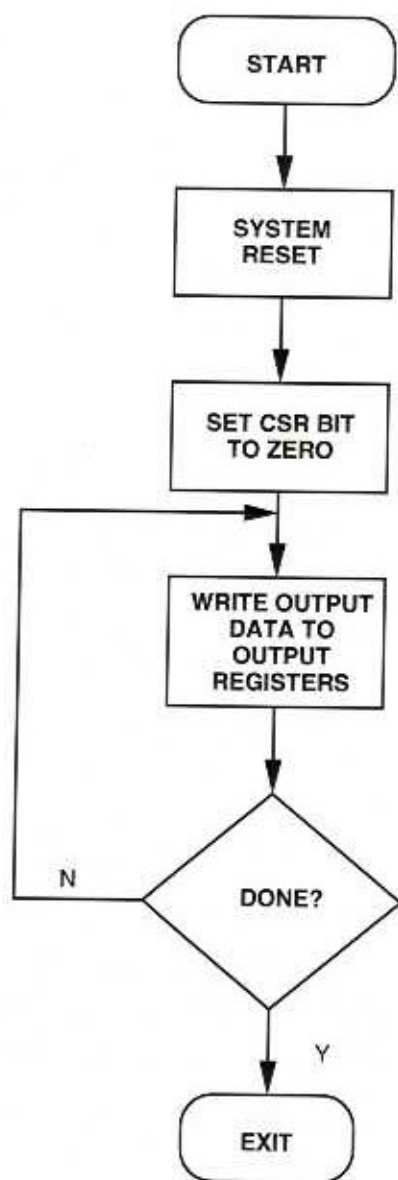


M2131/F4.3.2-1

NOTE: At system reset, the Fail LED is ON and the output drivers are disconnected.

Figure 4.3.2-1. Programming Flowchart (Built-in-Test Active)





M2131/F4.3.2-2

NOTE: At system reset, the output drivers are disconnected and the Fail LED is illuminated.

Figure 4.3.2-2. Programming Flowchart (Built-in-Test Not Active)

## SECTION 5

### CONFIGURATION AND INSTALLATION

#### 5.1 UNPACKING PROCEDURES

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES AS SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ECT., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning disposition of the damaged item(s).

#### 5.2 PHYSICAL INSTALLATION

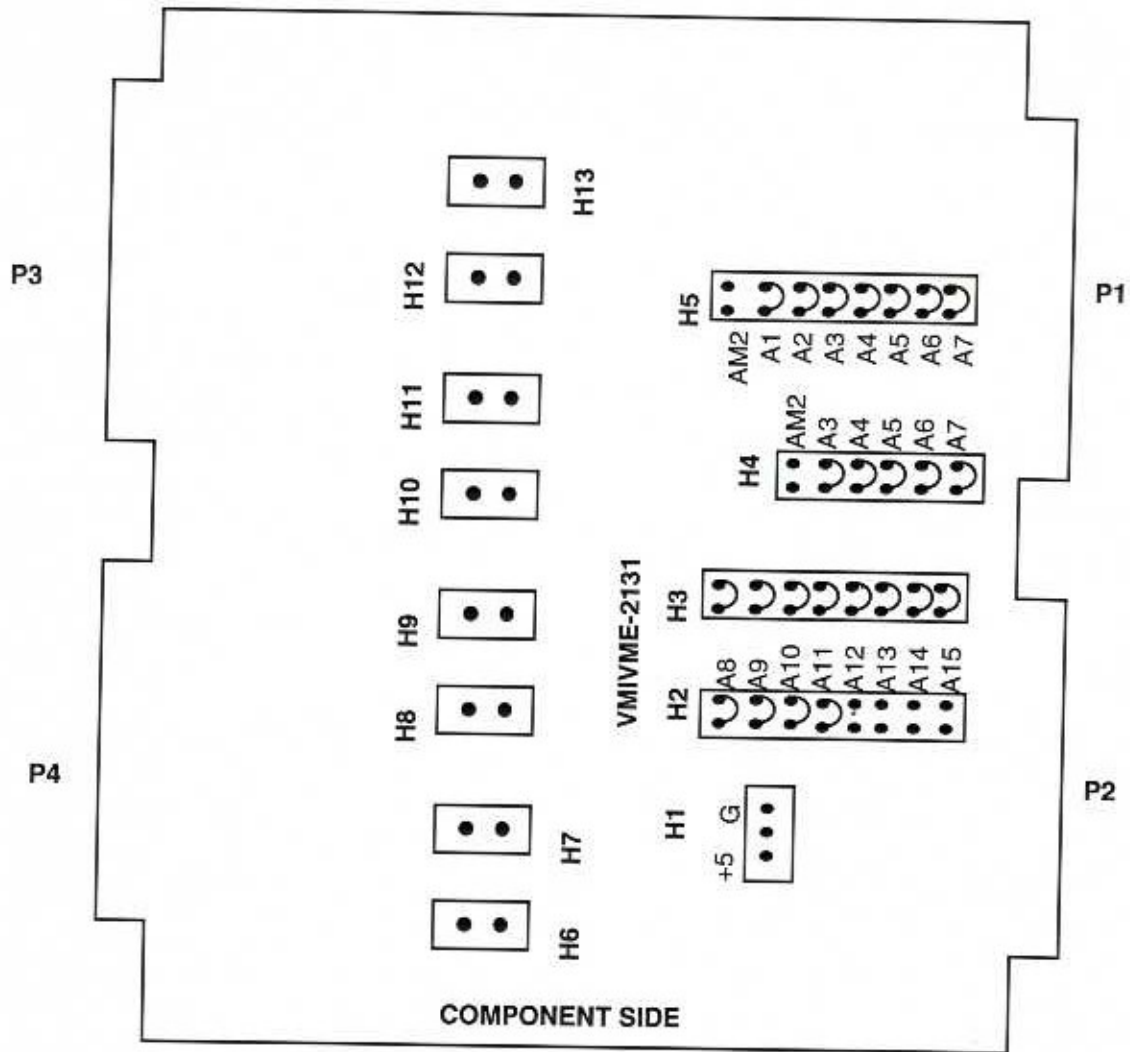
\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

**DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.**

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

#### 5.3 JUMPER LOCATIONS

The physical positions of the jumpers described in this section are shown in Figure 5.3-1.



M2131/F5.3-1

Figure 5.3-1. Jumper Locations Showing Factory Configuration

#### **5.4 SUPPRESSOR DIODE CONNECTIONS**

The output drivers of the VMIVME-2131 have built-in suppressor diodes for driving inductive loads. Thus, the user does not need to add diodes to his circuitry. A typical output driver stage is shown in Figure 5.4-1.

#### **5.5 ADDRESS MODIFIERS**

The VMIVME-2131 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed to short nonprivileged I/O access by installing jumpers in position AM2 of the headers H4 and H5. H4 is for the Output Registers, and H5 is for the CSR.

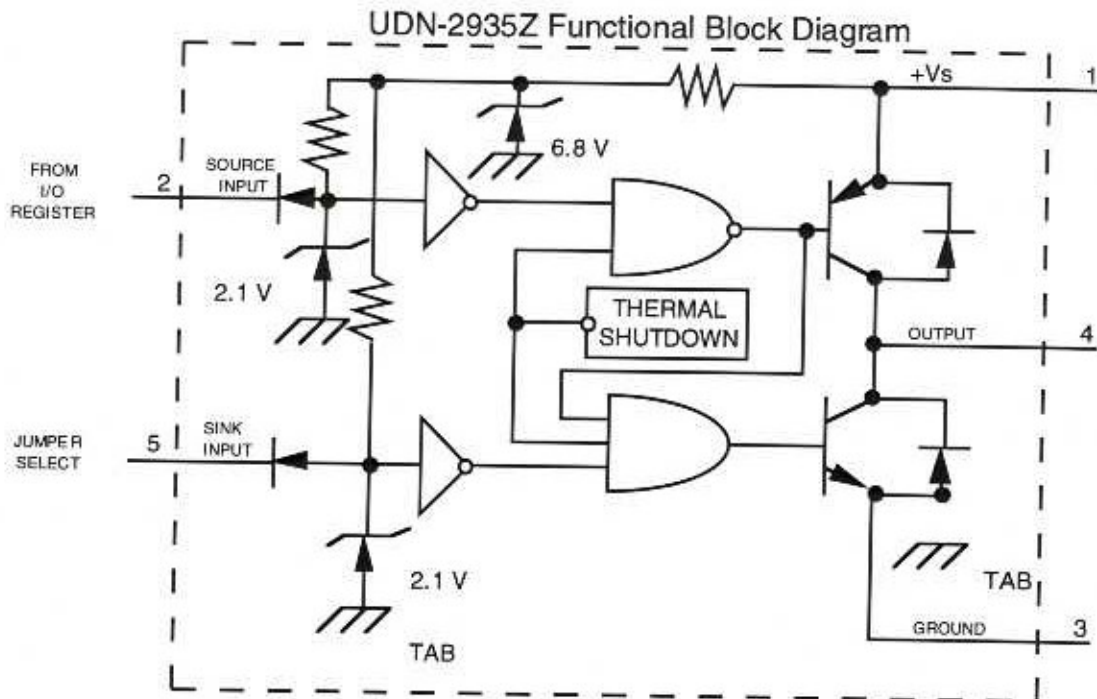
#### **5.6 ADDRESS SELECTION JUMPERS**

The VMIVME-2131 is designed with two banks of address select jumpers that specify the beginning board address for the Data Registers and the address of the CSR. The address selection jumpers are shown in Figures 5.6-1 and 5.6-2. These jumpers are used like an address switch, installing a jumper places the corresponding address bit to a logic "zero". If the jumper is removed, then the corresponding address bit will be a logic "one". The VMIVME-2131 is factory configured to respond to 0000 HEX for Data Registers and to F000 HEX for the CSR.

#### **5.7 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION**

The output connectors (P3 and P4) on the VMIVME-2131 are 64-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC Document No. 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

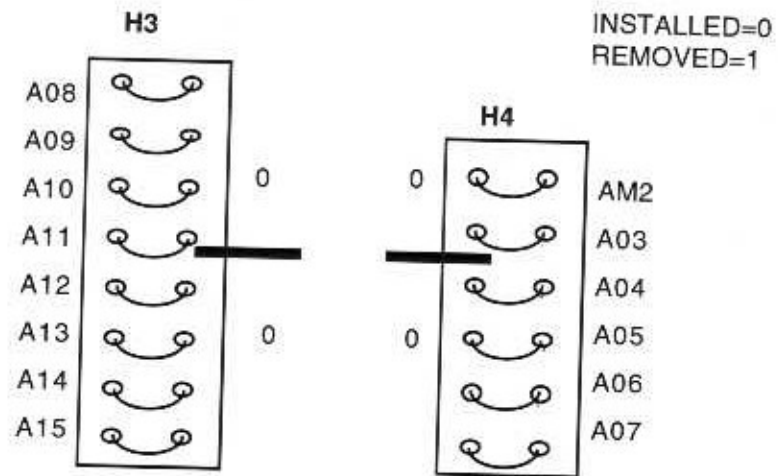


**LOGIC TRUTH TABLE**

DATA REGISTER INPUT, $V_2$	JUMPER SELECT INPUT, $V_5$	OUTPUT $V_4$
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	LOW
HIGH	HIGH	HIGH Z

M2131/F5.4-1

Figure 5.4-1. Typical Output Driver Stage

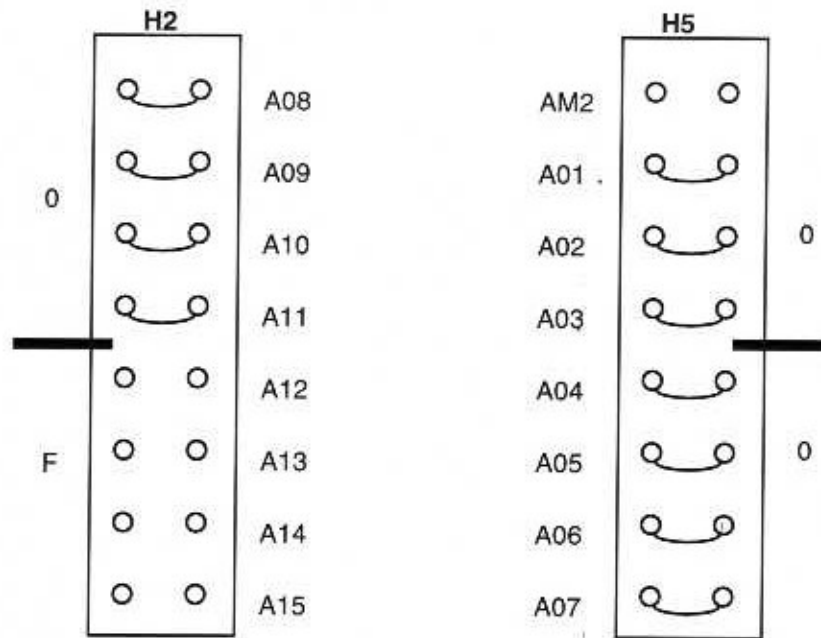


THE EXAMPLE SHOWN IS FOR BASE ADDRESS OF 0000 HEXADECIMAL

M2131/F5.6-1

Figure 5.6-1. Data Register Base Address Select Jumpers

INSTALLED=0  
REMOVED=1



THE EXAMPLE SHOWN IS FOR BASE ADDRESS OF F000 HEXADECIMAL

M2131/F5.6-2

Figure 5.6-2. CSR Base Address Select Jumpers

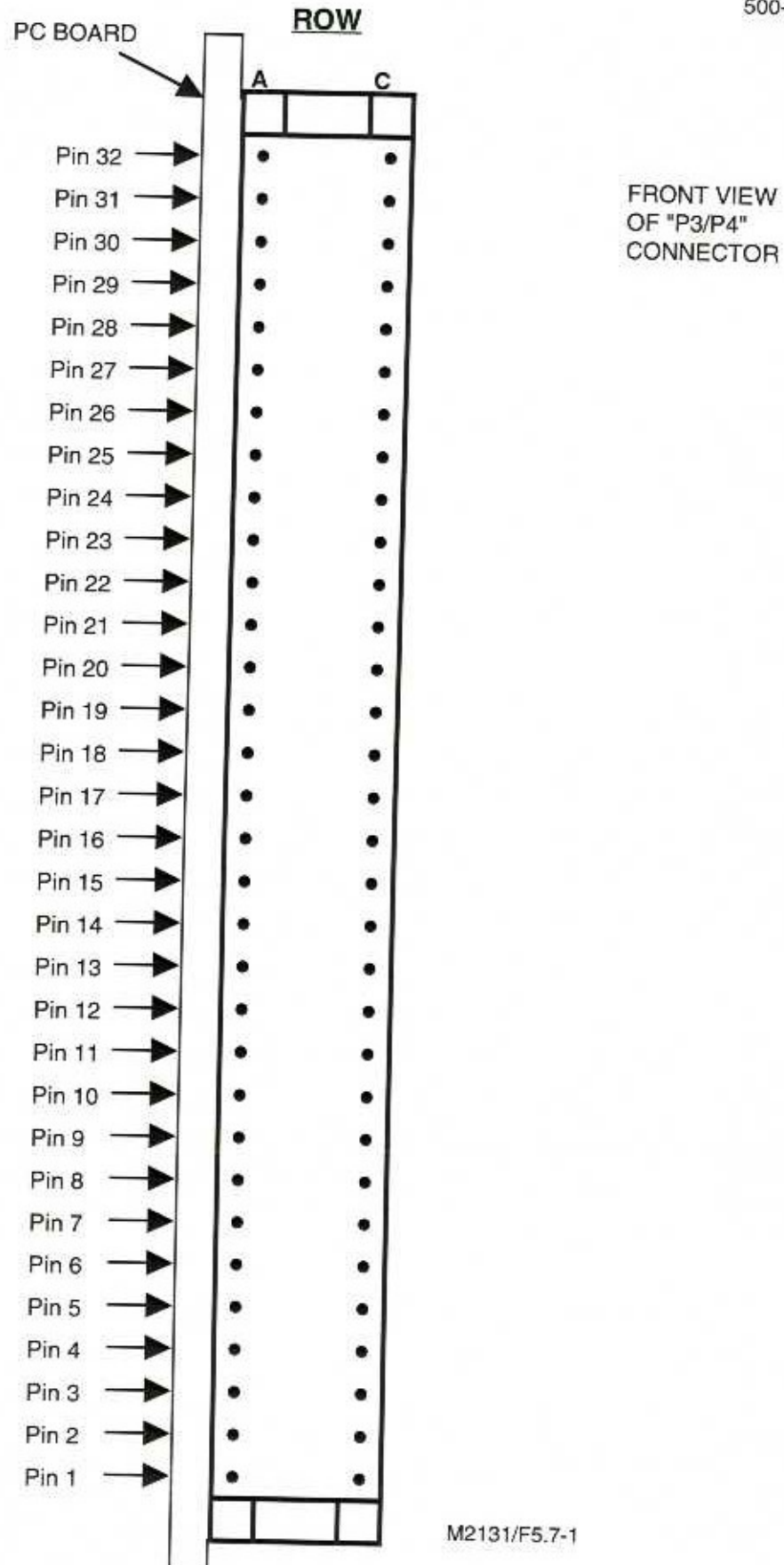


Figure 5.7-1. P3/P4 Connector - Pin Configuration



Table 5.7-1. Connector P4 Pin/Channel Assignments

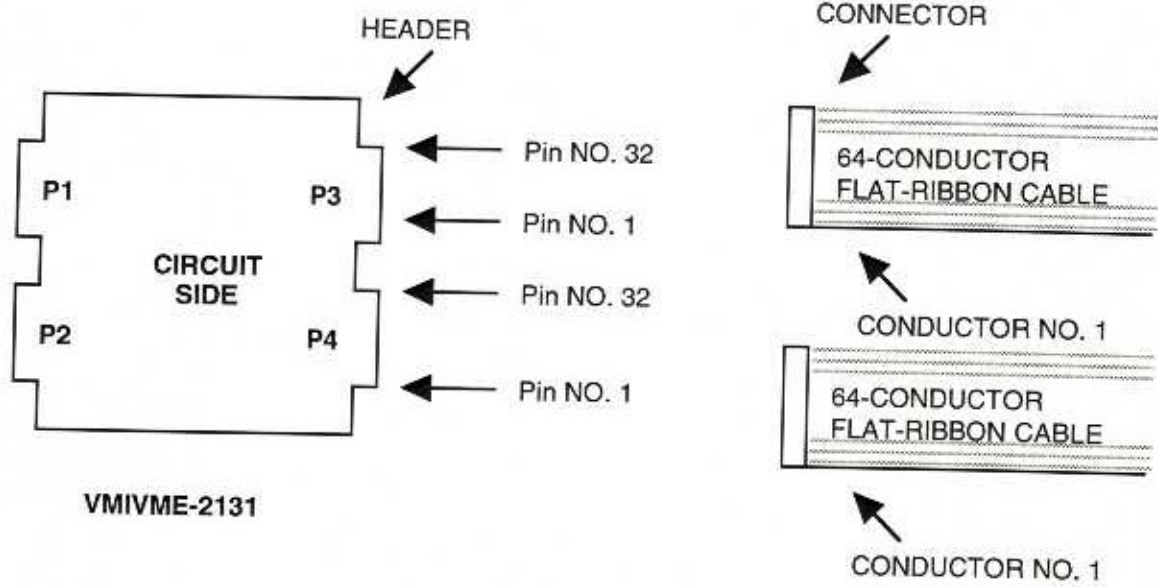
Pin NUMBER	ROW A (SIGNAL USAGE)	ROW C (SIGNAL USAGE)
1	CH00/01 VI	CH00 VO
2	GND	CH01 VO
3	CH02/03 VI	CH02 VO
4	GND	CH03 VO
5	CH04/05 VI	CH04 VO
6	GND	CH05 VO
7	CH06/07 VI	CH06 VO
8	GND	CH07 VO
9	CH08/09 VI	CH08 VO
10	GND	CH09 VO
11	CH10/11 VI	CH10 VO
12	GND	CH11 VO
13	CH12/13 VI	CH12 VO
14	GND	CH13 VO
15	CH14/15 VI	CH14 VO
16	GND	CH15 VO
17	CH16/17 VI	CH16 VO
18	GND	CH17 VO
19	CH18/19 VI	CH18 VO
20	GND	CH19 VO
21	CH20/21 VI	CH20 VO
22	GND	CH21 VO
23	CH22/23 VI	CH22 VO
24	GND	CH23 VO
25	CH24/25 VI	CH24 VO
26	GND	CH25 VO
27	CH26/27 VI	CH26 VO
28	GND	CH27 VO
29	CH28/29 VI	CH28 VO
30	GND	CH29 VO
31	CH30/31 VI	CH30 VO
32	GND	CH31 VO

M2131/T5.7-1

Table 5.7-2. Connector P3 Pin/Channel Assignments

Pin NUMBER	ROW A (SIGNAL USAGE)	ROW C (SIGNAL USAGE)
1	CH32/33 VI	CH32 VO
2	GND	CH33 VO
3	CH34/35 VI	CH34 VO
4	GND	CH35 VO
5	CH36/37 VI	CH36 VO
6	GND	CH37 VO
7	CH38/39 VI	CH38 VO
8	GND	CH39 VO
9	CH40/41 VI	CH40 VO
10	GND	CH41 VO
11	CH42/43 VI	CH42 VO
12	GND	CH43 VO
13	CH44/45 VI	CH44 VO
14	GND	CH45 VO
15	CH46/47 VI	CH46 VO
16	GND	CH47 VO
17	CH48/49 VI	CH48 VO
18	GND	CH49 VO
19	CH50/51 VI	CH50 VO
20	GND	CH51 VO
21	CH52/53 VI	CH52 VO
22	GND	CH53 VO
23	CH54/55 VI	CH54 VO
24	GND	CH55 VO
25	CH56/57 VI	CH56 VO
26	GND	CH57 VO
27	CH58/59 VI	CH58 VO
28	GND	CH59 VO
29	CH60/61 VI	CH60 VO
30	GND	CH61 VO
31	CH62/63 VI	CH62 VO
32	GND	CH63 VO

M2131/T5.7-2



M2131/F5.7-2

Figure 5.7-2. Cable Connector Configuration

Output connector pin configurations for P3 and P4 are shown in Figure 5.7-1. Connector pin assignments for the 64 output channels are shown in Tables 5.7-1 and 5.7-2. The signals on row A of the connectors are used by two output drivers (as stated in the signal name). These power lines should be returned directly to the power source of the external circuitry. This is to help prevent excessive current from flowing in the backplane. A compatible flat-ribbon cable connector is Panduit No. 120-964-435E. A compatible strain relief is Panduit No. 100-000-032. Cable connector configuration is shown in Figure 5.7-2.

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

**THE USER SHOULD USE THE CABLE GROUND LINES FOR THE EXTERNAL POWER SUPPLY RETURNS. THIS IS REQUIRED TO PREVENT EXCESSIVE CURRENT FROM FLOWING INTO THE VMEbus BACKPLANE. ALSO, THE USER SHOULD REMOVE POWER BEFORE THE CABLES ARE CONNECTED OR DISCONNECTED (FROM THE BOARD). THIS WILL PREVENT EXCESSIVE CURRENTS FROM DAMAGING THE P3/P4 CONNECTOR PINS.**

## 5.8 JUMPER FUNCTIONS

Jumper H1 is provided to invert the data written to the Control and Status Register (CSR). It is configured at the factory such that the test software writes positive data to the CSR. The data polarity used by this board is controlled by the selection of data transceivers which interface with the VMEbus. For positive true data, the jumper H1 is placed in the +5 position, and for negative true data the jumper H1 is placed in the G position, unless the option of the board is a -1XX then for positive true data the jumper H1 is placed in the G position, and for negative true data the jumper H1 is placed in the +5 position.

Jumpers H6 through H13 are used to select the mode of operation for output drivers. If the jumper is not installed, the output devices operate in the current source mode. With the jumper installed, the associated output drivers will source as well as sink current (depending on output logic level). Please refer to the logic truth table in Figure 5.4-1 for the logical operation of these devices. This table is based on an impedance to ground.



## **SECTION 6**

### **MAINTENANCE AND WARRANTY**

#### **6.1 MAINTENANCE**

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

- a. Software
- b. System configuration
- c. Electrical connections
- d. Jumper or configuration options
- e. Boards fully inserted into their proper connector location
- f. Connector pins are clean and free from contamination
- g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
- h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

#### **6.2 MAINTENANCE PRINTS**

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

#### **6.3 WARRANTY**

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The

defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

**THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.**

#### **6.4 OUT-OF-WARRANTY REPAIR POLICY**

The following sections describe VMIC's policy on repairs and warranties on repaired products.



#### **6.4.1 Repair Category**

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

- a. Product Exchange
- b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

#### **6.4.2 Repair Pricing**

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

#### **6.4.3 Payment**

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation  
12090 South Memorial Parkway  
Huntsville, Alabama 35803-3308  
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

#### **6.4.4     Shipping Charges**

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

#### **6.4.5     Shipping Instructions**

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

#### **6.4.6     Warranty on Repairs**

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

#### **6.4.7     Exclusions**

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.



## **APPENDIX A**

**ASSEMBLY DRAWING, PARTS LIST,  
AND SCHEMATIC**