VMIVME-2170A
32-bit Optically Coupled Digital Output Board

Product Manual

A GE Fanuc Company

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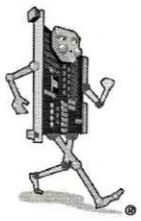

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(IOWorks man figure)

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Overview

Introduction

Features

The VMIVME-2170A is a VMEbus compatible 32-bit optically coupled digital output board. Its features include:

- 32 bits of optically isolated digital outputs
- 8- or 16-bit data transfers
- Inverting or noninverting data options
- Optional pull-up resistors
- 2.5 or 300 mA options
- Nonprivileged or supervisory short I/O transfers

Functional Description

The VMIVME-2170A Optically Coupled Digital Output Board consists of VMEbus compatibility logic, data output control logic, four 8-bit output registers, and 32 bits of optically isolated outputs. The VMEbus compatibility logic contains address decoding logic, and data transfer control logic which provides for 8- or 16-bit data transfers in the short I/O address space. The data output control logic, in conjunction with four 8-bit registers, selects byte or word transfers to the 32 optically isolated output channels. The thirty-two optically coupled output channels convert the TTL output data into optically coupled digital outputs, whose output state either matches or is inverted from the data written to the board.

Reference Material List

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA

VMEbus International Trade Association

7825 East Gelding Drive, No. 104

Scottsdale, Arizona 85260

(602) 951-8866

FAX: (602) 951-0720

www.vita.com

Physical Description and Specifications: Refer to Product Specification, 800-102170-000 available from:

VMIC

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www.vmic.com

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O Products (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

Safety Symbols Used in This Manual

STOP: This symbol informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: This sign denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: This sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER 1

Theory of Operation

Contents

Introduction

The VMIVME-2170A consists of five primary functional building blocks as illustrated in Figure 1-1 on page 18. The five sections of the VMIVME-2170A are:

1. Address Logic
2. Control Logic
3. Data Logic
4. Output Data Registers
5. Output Buffers

Each section of the design is illustrated in further detail as shown in Figure 1-2 on page 19 through Figure 1-5 on page 23.

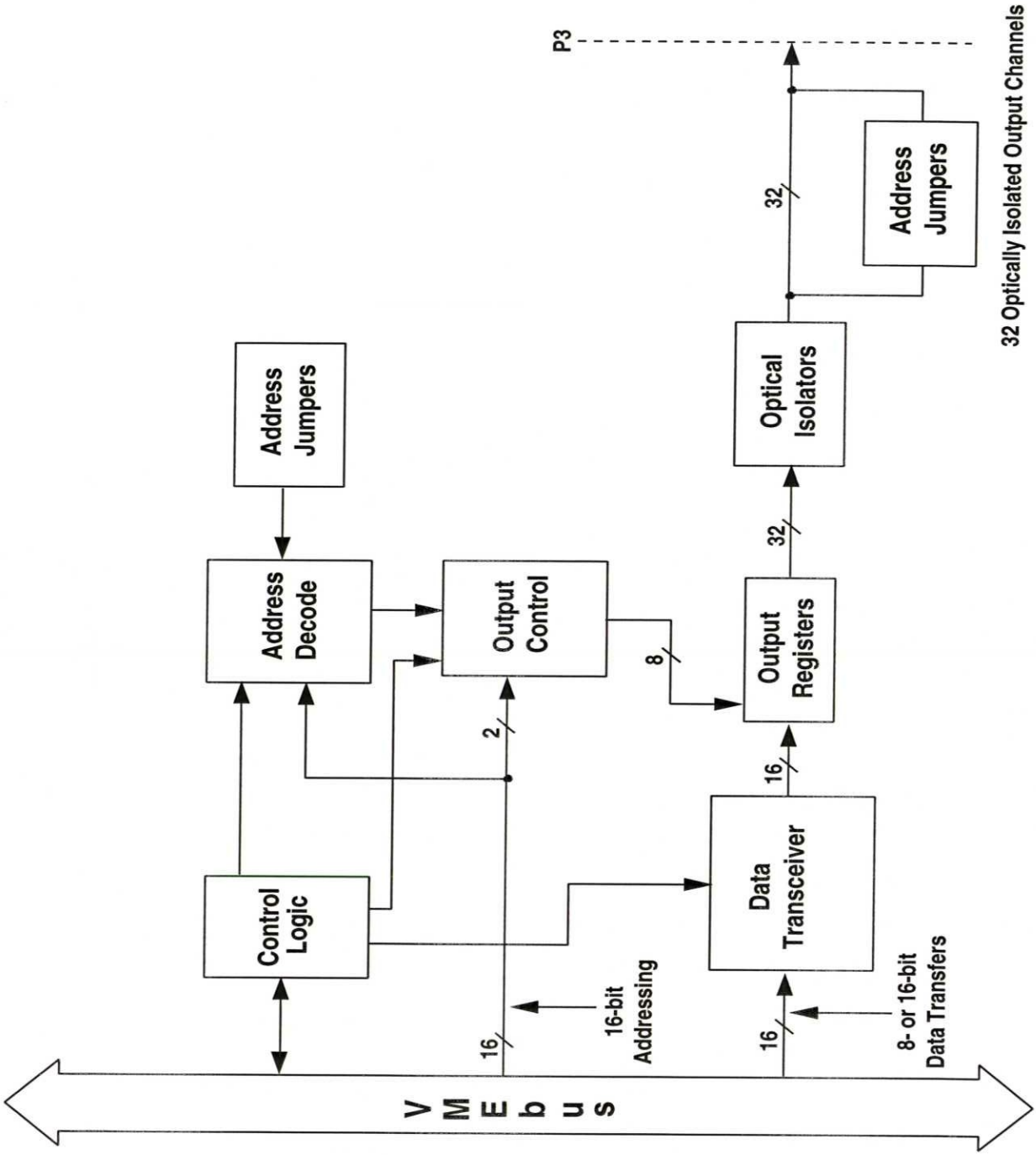


Figure 1-1 VMIVME-2170A Functional Block Diagram

Board Addressing

The VMIVME-2170A is designed to support data transfers in supervisory or nonprivileged short I/O memory space. A jumper (JA1) is provided as shown in Figure 1-2 (Address Section Block Diagram) to allow user-selection of either I/O access type. The VMIVME-2170A is factory configured (jumper JA1 is not installed) to respond to short supervisory I/O access.

The VMIVME-2170A is designed with 14 address select jumpers and decode logic as shown in Figure 1-2. This circuitry is used to establish the base address of the board. A jumper installed requires a logic "zero" for that address bit; otherwise, a logic "one" is needed. This topology provides an efficient memory address map for I/O addresses. This feature allows the user to map the I/O addresses into contiguous memory locations when configuring subsystems that require more than one board.

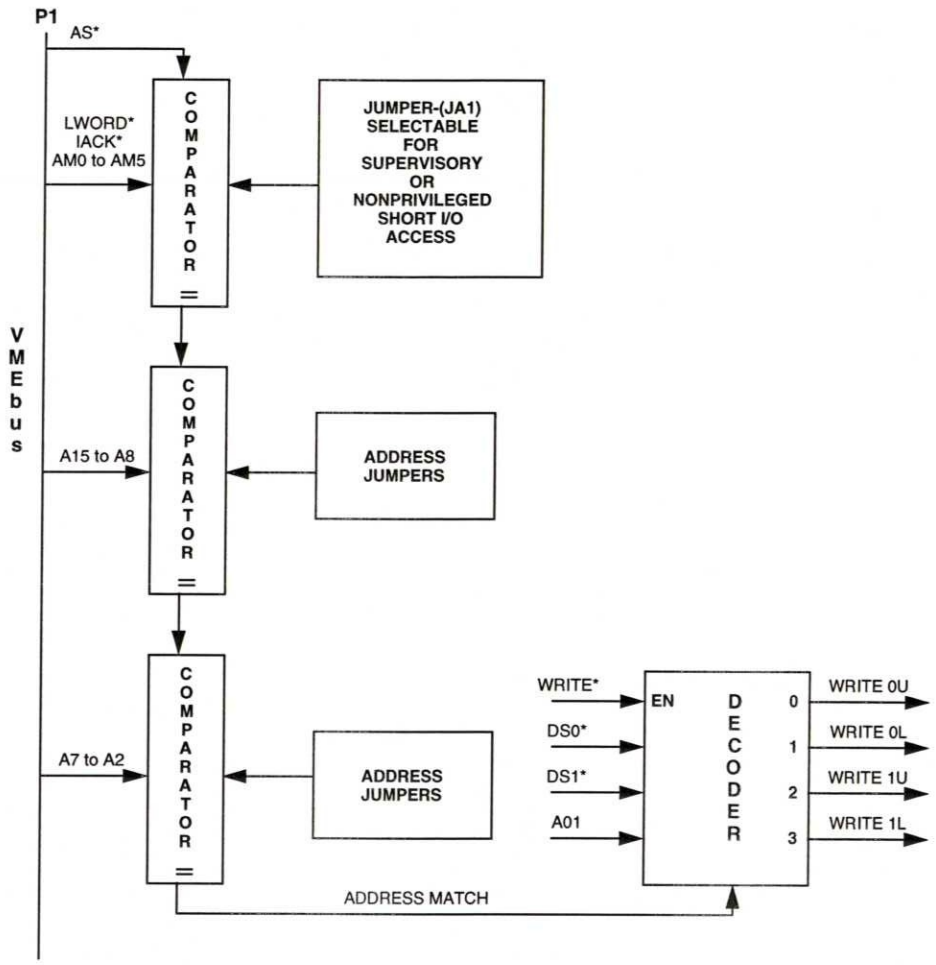


Figure 1-2 Address Section Block Diagram

Logic Description

Typical VMEbus transceivers, receivers, and control logic are shown in Figure 1-3 on page 21. The VMEbus signal lines used by the VMIVME-2170A are shown in Figure 1-4 on page 22. This logic steers data to the proper output registers based on the signals controlling this logic.

To perform data transfers with the VMIVME-2170A, data is written to the output data registers labeled R0 and R1. The appropriate outputs are selected by address bit A01. It is used to select one of two banks of 16 bits for data outputs. The two data strobes DS0 and DS1 allow the 16-bit banks to be accessed as words or bytes.

The address match signal shown inFigure 1-3 on page 21 is logically gated with DS0 and DS1 to produce active signals for data transfer. These gated signals clock data into the output registers, which store the output data from the VMEbus and hold it for the output drivers.

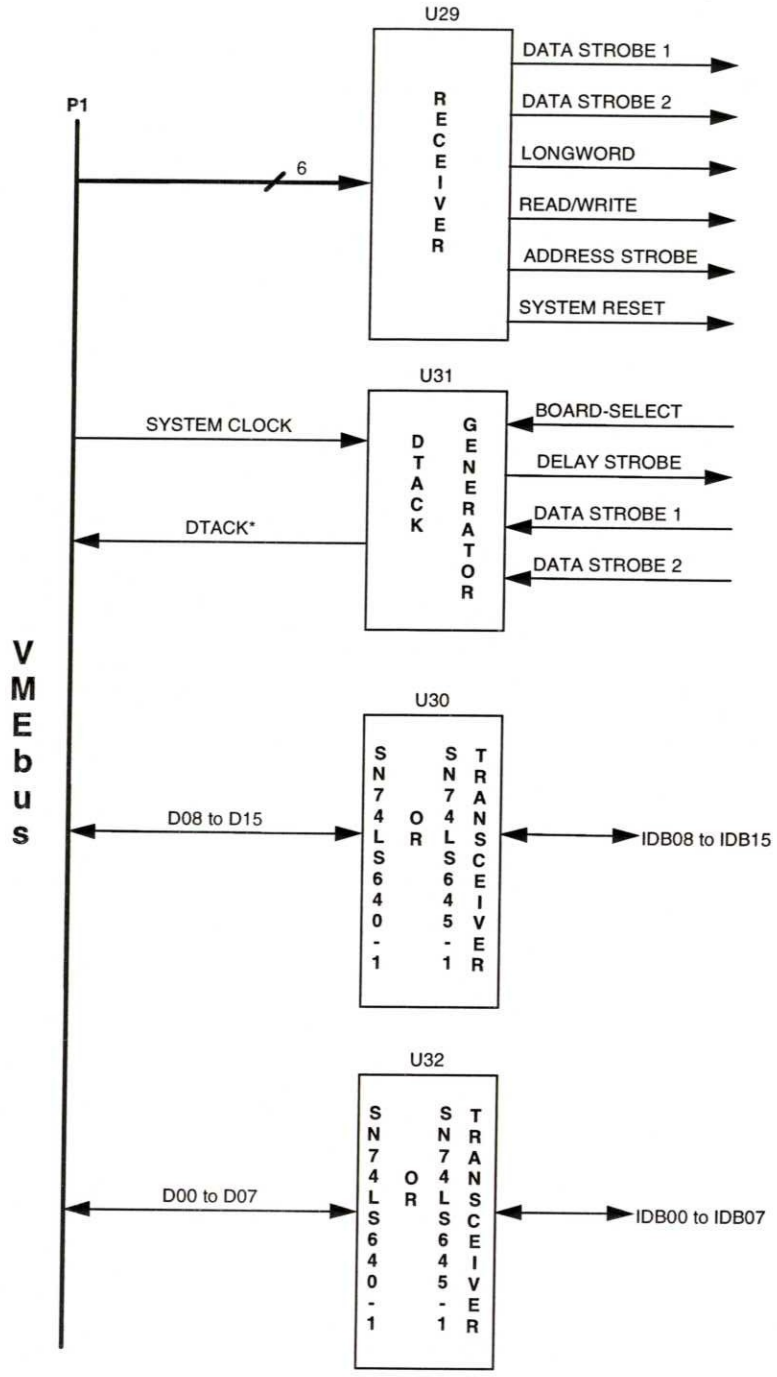


Figure 1-3 Control Section Block Diagram

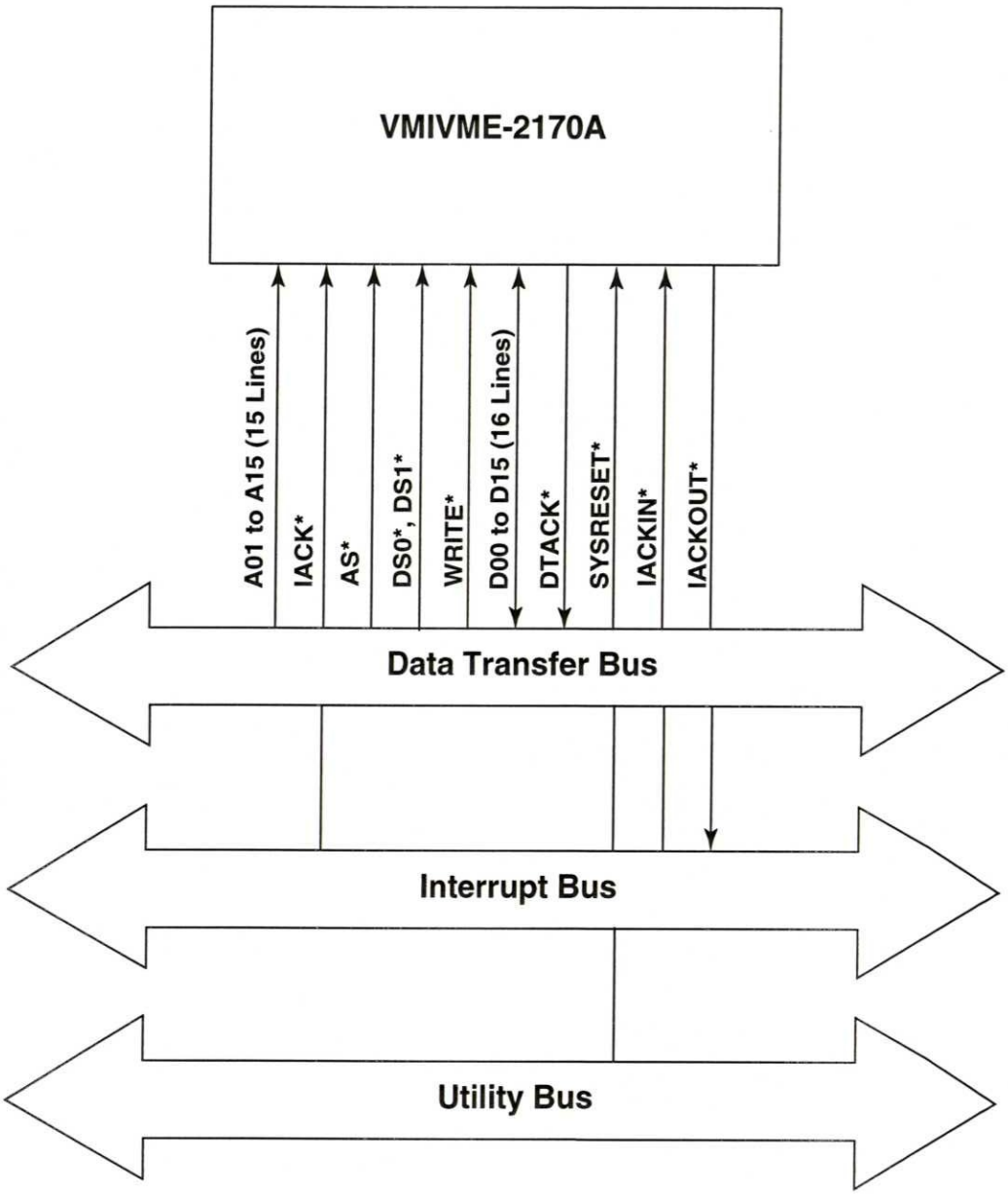


Figure 1-4 VMEbus Signal Lines Used by the VMIVME-2170A

Output Register Logic

The VMIVME-2170A is designed with four 8-bit Output Registers, which are controlled by four flip-flops as shown in Figure 1-5. These flip-flops are initialized at power-up or after a system reset such that all output registers are in the tri-state mode. This effectively disables the output ports until the first write strobe is sent to each register. The register outputs are routed to optical couplers whose outputs are connected to the front panel output connector.

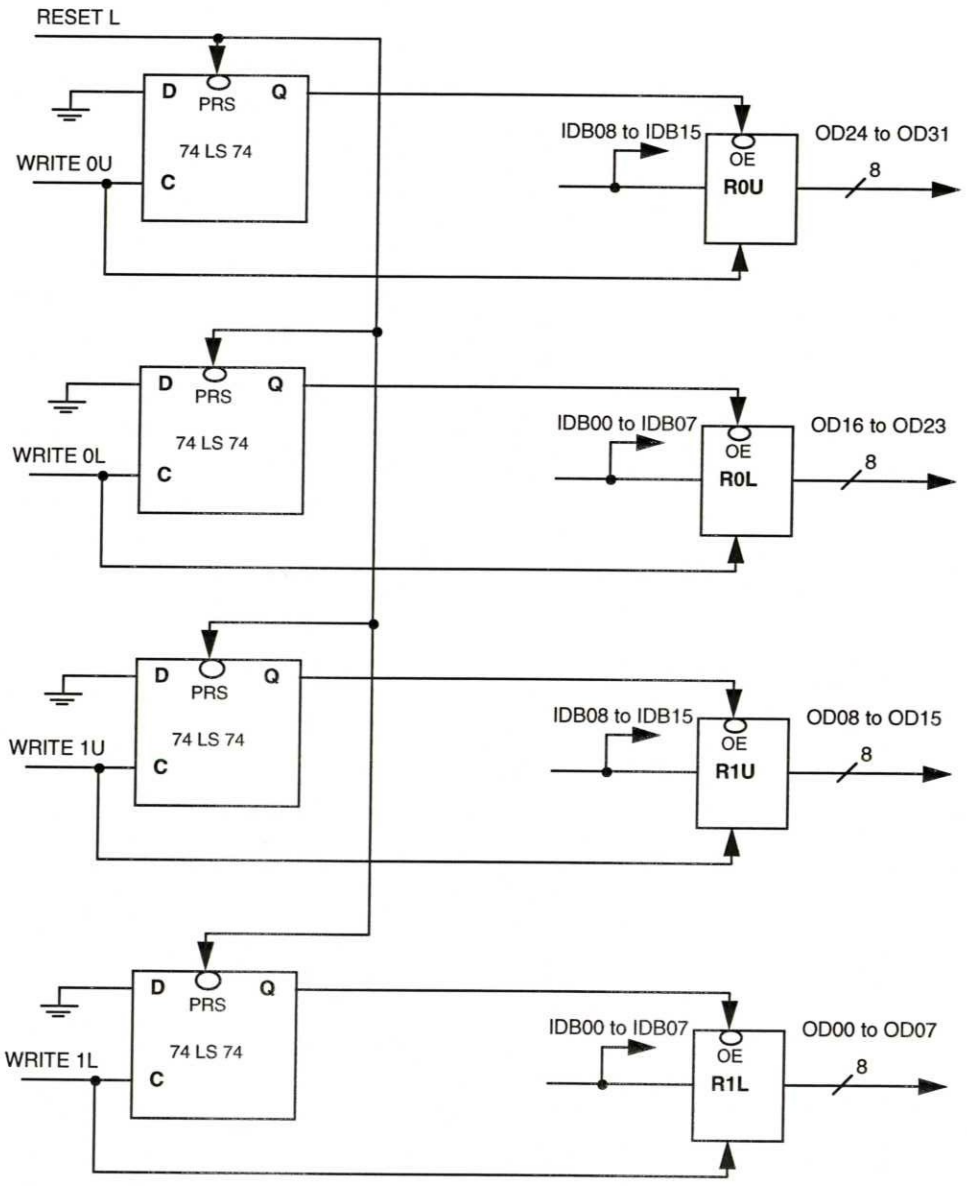


Figure 1-5 Output Register Logic

Optical Isolator and Output Driver

A typical output stage is shown in Figure 1-6 on page 25. A jumper is shown but it really just replaces the 330 Ω resistor. When the low current option is ordered, the 330 Ω resistor is replaced with the jumper. The two transistors and the 680 Ω resistor are not installed. Thus, the opto-isolator's collector and emitter go to the output connector.

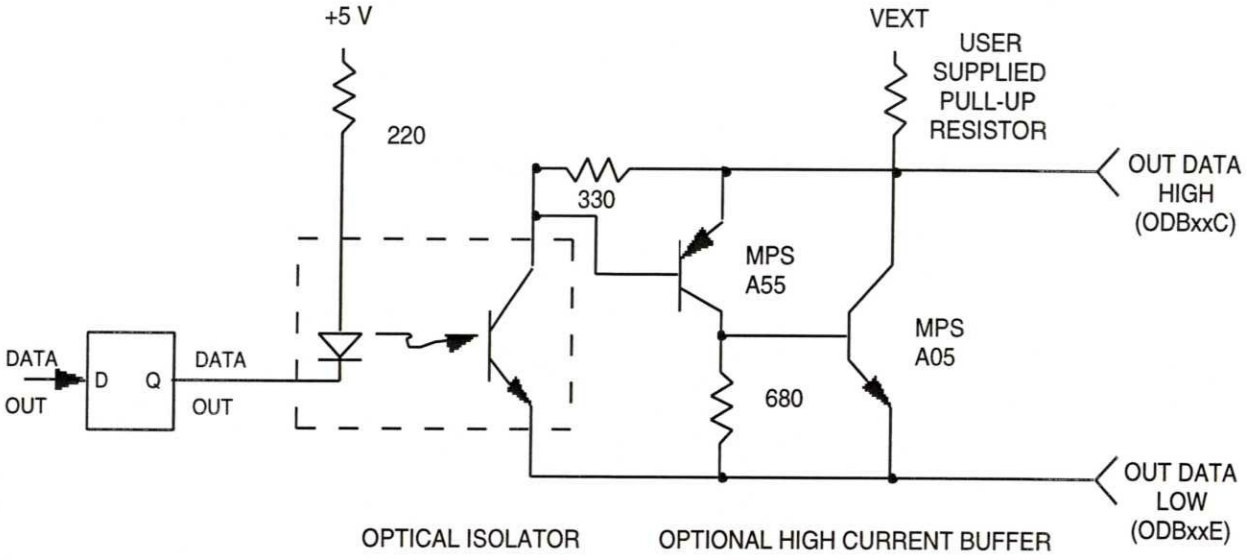
For users who require higher output current, an optional transistor buffer may be installed during manufacturing. An optional pull-up resistor is also shown in Figure 1-6 on page 25. The signal VEXT is provided by the user and is available on pin A28 of connector P2. The maximum value for VEXT is determined by the option ordered. The low current VEXT should not exceed 30 V, and the high current VEXT should not exceed 50 V. The current drawn by this line should not exceed 1 A to prevent damage to the VMEbus and/or the connector pin. However, using the pull-up resistor degrades the isolation between channels because it is part of a DIP resistor package.

Low Current Option

The low current option provides up to six thousand volts (6,000 V) of isolation (for one second) between all outputs, and between the VMEbus and all outputs. The saturation voltage for this option is 0.7 V at 2.5 mA of output current. The installation of DIP resistors will degrade the isolation between channels.

High Current Option

The high current option provides up to six thousand volts (6,000 V) of isolation (for one second) between the VMEbus and all outputs. The saturation voltage for this option is 1.25 V maximum at 300 mA of output current. Please refer to the product specification for more details about this option. The installation of DIP resistors will degrade the isolation between channels.



* Install only a wire in the 330 position for the Low Current Option.
Install the Resistors and Transistors for the High Current Option.

Figure 1-6 Optical Isolator Output Stage Block Diagram

CHAPTER 2

Configuration and Installation

Contents

Introduction

This chapter describes the installation and configuration of the board. Cable configuration, jumper/switch configuration and board layout are illustrated in this chapter.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

CAUTION: Do not install or remove the boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Jumper Locations

Refer to Figure 2-1 below for the locations of the jumpers described in this section.

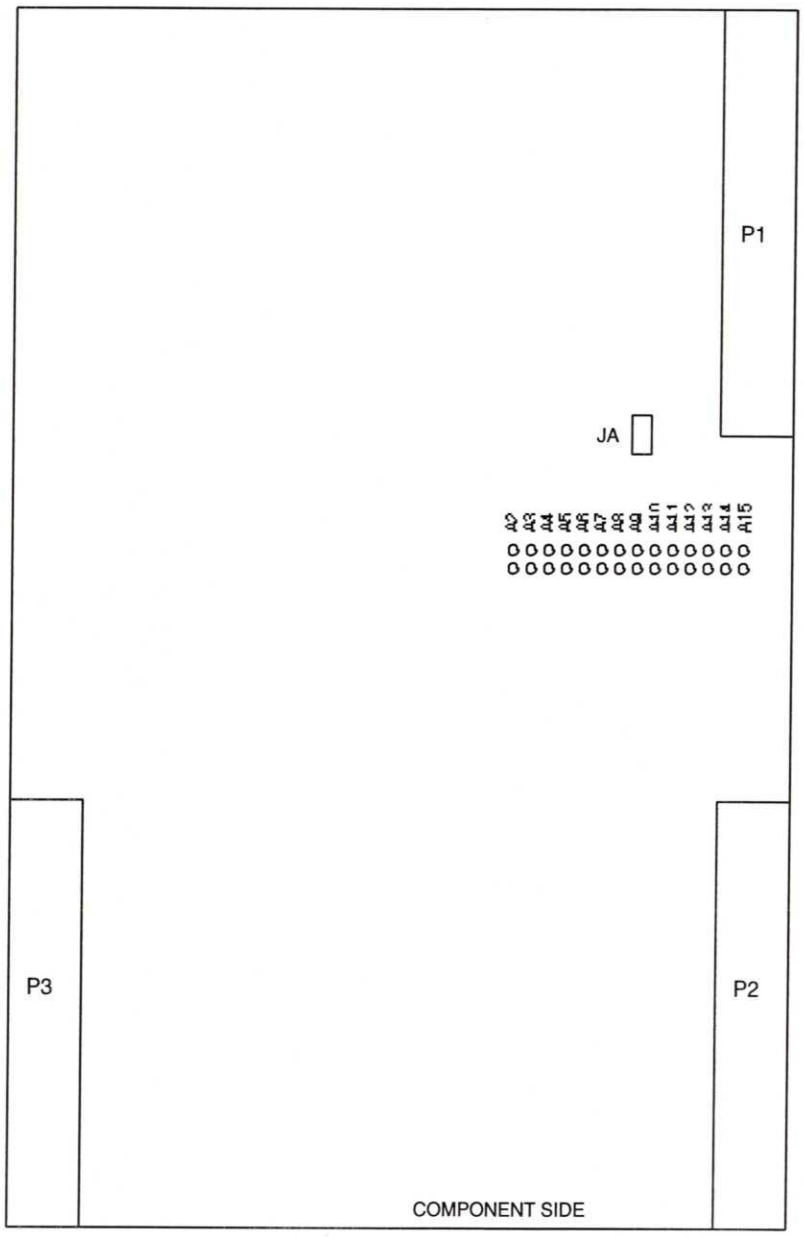


Figure 2-1 Location of Jumpers and Address Switches

External Pull-Up Voltage

External voltage is connected through the P2 connector on pin A28. The current drawn from this pin should not exceed 1 A, to prevent damaging the VMEbus backplane or the pin.

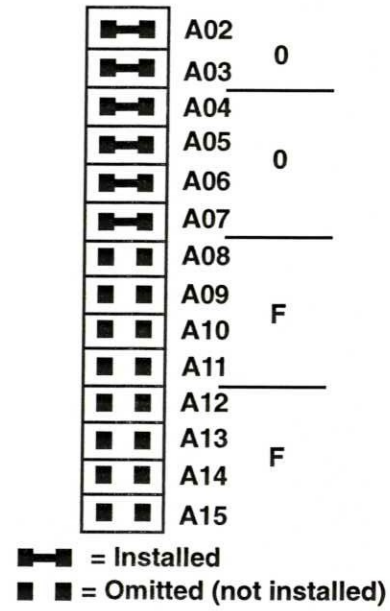
The External voltage return should not be connected to the VMEbus ground. Instead, it should be connected to the applicable C row of the P3 connector. Refer to Figure 2-4 on page 36.

Address Modifiers

The VMIVME-2170A is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper JA1. With a jumper installed at JA1, the board will respond to short nonprivileged I/O access.

Address Selection Jumpers

Figure 2-2 below shows the addressing jumpers on board the VMIVME-2170A and their use in the addressing scheme. The board is factory configured to respond to a base address of $0000. This means that all of the address jumpers are installed. Figure 2-2 is an example of another base address.



Example: For the VMIVME-2170A to respond to a base address of ($FF00) the jumpers should be installed as shown in Figure 2-2.

Figure 2-2 Address Select Jumpers

User-Installed Pull-Up Resistors

DIP sockets are provided so that the user may install resistor DIPs RP1 through RP4, as necessary. The ohmic value of the resistor is left to the expertise of the user; however, lower resistor values may limit the effective output voltage due to a .1 W limit on resistor power dissipation. Using these resistors will degrade the isolation between channels.

WARNING: The power rating of the DIP pull-up resistor is 0.1 W. Exceeding this rating will damage the DIP.

I/O Cable and Front Panel Connector Configuration

The output connector (P3) on the VMIVME-2170A is a 64-pin DIN standard and was selected by VMIC because of its high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC Publication No. 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning the output connections are shown in Figure 2-3 below. This figure has Conductor No. 1 shown at the bottom of the connector as it plugs into the header due to Pin No. 1 of P3 being mounted as shown. Figure 2-4 on page 36 shows the P3 connector pin assignment for the 32 output channels of the VMIVME-2170A. Connector pin configurations are also shown in Figure 2-4 on page 36. The output channel names ending in "C" go to the appropriate output channel's collector lead, while the names ending with "E" are for the appropriate channel's emitter lead. Details concerning the connection of an external voltage are shown in Table 2-1 on page 37.

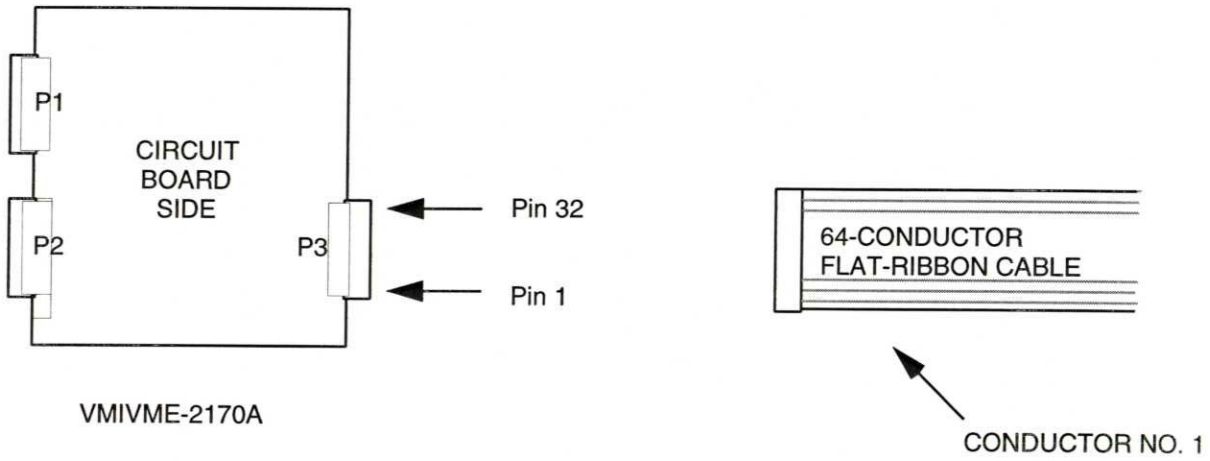


Figure 2-3 Cable Connector Configuration

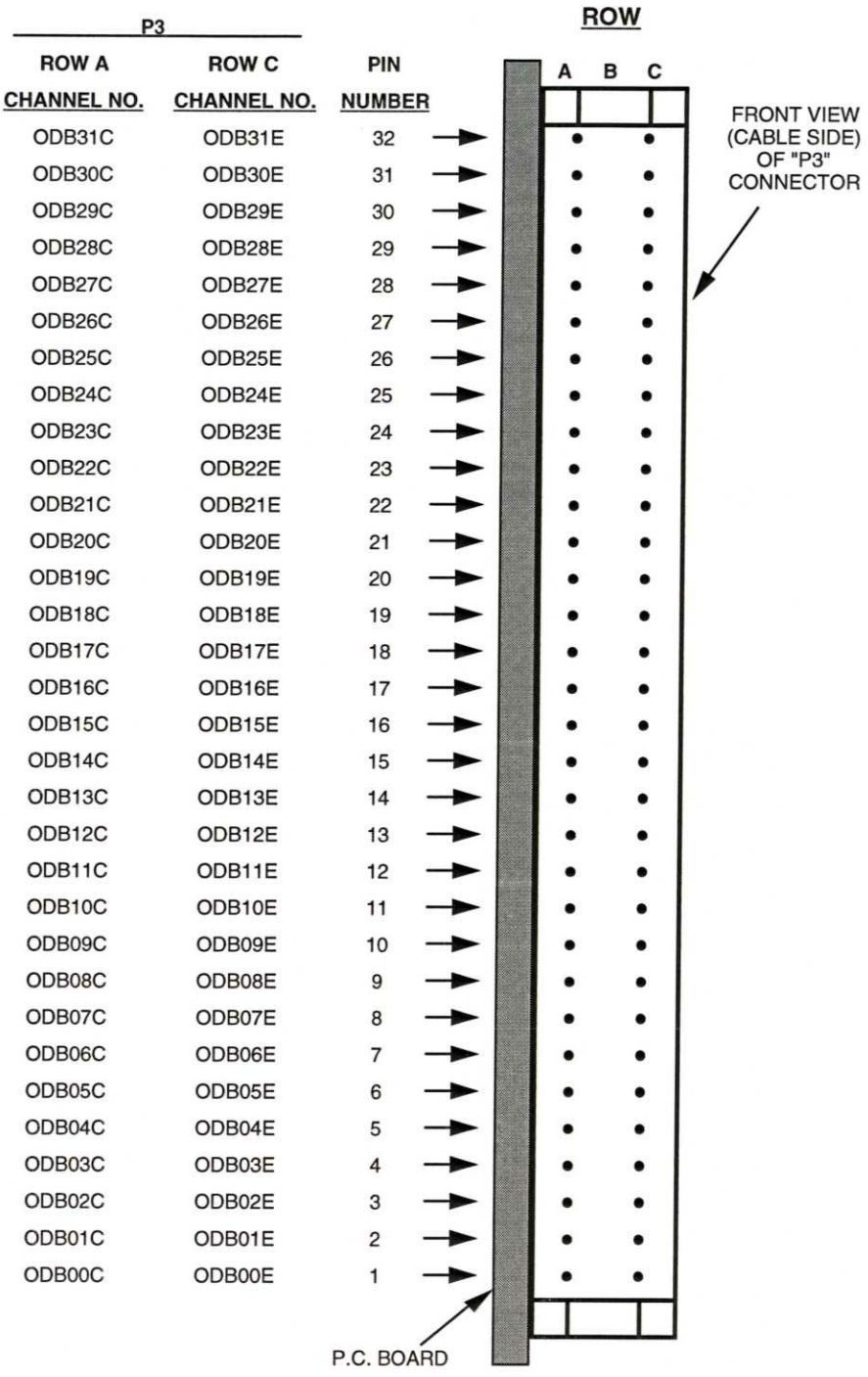


Figure 2-4 P3 Connector Pin Layout

Table 2-1 P2 Connector Pinout

PIN NO.	ROW A (1)	ROW B (2)	ROW C
1		+5 V	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 V	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25			
26			
27			
28	EXT V		
29			
30			
31		GND	
32		+5 V	

Notes: 1. External Reference Voltage is supplied by the user.
2. Inputs to the Board - not required.

CHAPTER 3

Programming

Contents

Introduction

Operational Overview

The four 8-bit Output Data Registers are accessed as two 16-bit words, or as four 8-bit bytes. Bit A01 is used to select each register word, when the board has been selected for a data transfer, and the data strobes select the byte or bytes for data transfer. Fourteen address bits, A15 through A02, are used for decoding the board's base address. When a valid data transfer is decoded, a board-select signal is generated, which activates the board for a data transfer. The reader should refer to Chapter 2 for details concerning board addressing. The VMIVME-2170A supports only 8- or 16-bit data transfers. If a longword access is attempted, the VMIVME-2170A will not respond, and a bus time-out error will occur.

Register Map

Address bits A15 through A2 are selected by address select jumpers; therefore, the XXX in the relative address represents the part of the address that is jumper-selectable. Chapter 2 describes how to set up this base address. A register map is shown in Table 3-1. Detailed register bit definitions are shown in Table 3-2.

Table 3-1 VMIVME-2170A Register Map

Relative Address	Mnemonic	Name/Function
$XXX0	DR0	Data Register 0
$XXX1	DR1	Data Register 1
$XXX2	DR2	Data Register 2
$XXX3	DR3	Data Register 3

Table 3-2 Register Bit Definitions

$XXX0 DATA REGISTER 0

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
OUTPUT DATA							
OD31	**OD30**	**OD29**	**OD28**	**OD27**	**OD26**	**OD25**	**OD24**

$XXX1 DATA REGISTER 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUTPUT DATA							
OD23	**OD22**	**OD21**	**OD20**	**OD19**	**OD18**	**OD17**	**OD16**

$XXX2 DATA REGISTER 2

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
OUTPUT DATA							
OD15	**OD14**	**OD13**	**OD12**	**OD11**	**OD10**	**OD9**	**OD8**

$XXX3 DATA REGISTER 3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUTPUT DATA							
OD7	**OD6**	**OD5**	**OD4**	**OD3**	**OD2**	**OD1**	**OD0**

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

Contact VMIC Customer Care at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.