VMICPCI-1335
CompactPCI bus-Compatible
16-Channel
Optically Coupled Digital Input Board

Product Manual

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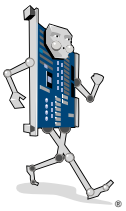

(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

VMIC

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Overview

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Introduction

The VMICPCI-1335 CompactPCI bus 16-Channel Optically Coupled Digital Input Board is designed to provide isolation between the field and the CPCI bus host, and provides 16 optically coupled inputs. The inputs provide a sustained 1.5 kV of system isolation to the CPCI bus. The inputs have a software-selectable debounce timer to prevent false readings of mechanical switches or relays.

The VMICPCI-1335 board has several features as specified below:

1. 16 optically coupled voltage or contact sensing inputs
2. External voltage on byte boundaries to supply power for contact sensing mode
3. Input ranges of 5 to 125 VDC
4. 8-, 16-, or 32-bit data transfers
5. Fail LED
6. 3U Eurocard with optional 6U front panel
7. Compliance with PCI Specification Revision 2.1 and CompactPCI Specification 2.0 R2.1.

Functional Description

The VMICPCI-1335 board contains input circuitry where the input voltage range and configuration of the inputs are set during manufacturing according to the selected option.

A Control and Status Register (CSR) is used to control the state of the board. It allows the user to select one of eight possible input debounce times and provides control for the Fail LED. The purpose of the Fail LED is for status indication under user software control. The default reset condition of the Fail LED is ON. This does not indicate a failure of the board because the board does not contain any self-test capabilities.

Related Documents

For a detailed explanation of the PCI local bus and its characteristics, refer to the *PCI Local Bus Specification* from:

PCI Local Bus Specification, Revision 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)

For a detailed explanation of the CompactPCI bus and its characteristics, refer to the *CompactPCI Specification, 2.0 R2.1* from:

PCI Industrial Manufacturers Group
(PICMG)
301 Edgewater Place
Suite 220
Wakefield, MA 01880 USA
(617) 224-1100
(503) 797-4207 (International)
Fax: (617) 224-1239
Web: www.PICMG.ORG

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

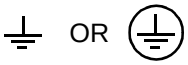
Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

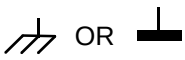
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



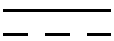
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

The STOP symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER
1

Theory of Operation

Contents

Introduction

The VMICPCI-1335 CompactPCI bus-Compatible 16-Channel Optically Coupled Digital Input Board is designed to provide isolation between the system hardware and the CPCI bus. One of five input threshold levels (5, 12, 24 to 28, 48, or 125 V) is set during manufacturing according to the option ordered.

The VMICPCI-1335 board's address is assigned by the system's Basic Input/Output System (BIOS) during system powerup per the PCI specification. Executing a read cycle to the data register latches field data in the Input Data Registers (IDR). The data is then routed to the proper data lines on the CompactPCI bus for the host to use. Successive reads of the field data will present the same data that was latched from the previous read until the debounce timer expires. Only after expiration of the debounce timer will new data be stored in the IDR on a read cycle. The debounce timer is software-selectable among eight separate time intervals. Refer to Table on page 42 for the specific debounce delay times.

Figure 1-1 is a block diagram of the basic functions of the VMICPCI-1335. These blocks will be discussed in more detail in the following sections.

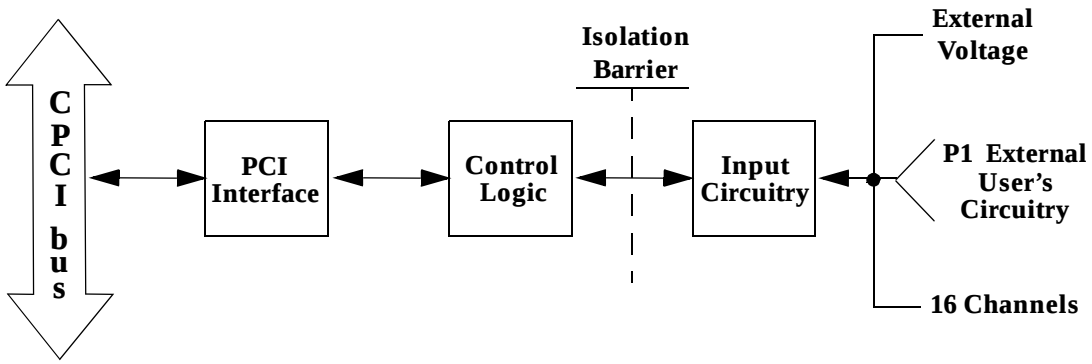


Figure 1-1 VMICPCI-1335 Board's Functional Block Diagram

PCI Compatibility

The VMICPCI-1335 board is a CompactPCI-Compatible Add-On Target Card which provides an 8-, 16-, or 32-bit connection to the CompactPCI bus. The board occupies 64 byte of contiguous I/O and memory space and can be mapped onto any normal PCI I/O and/or memory address. The board does not utilize interrupts or DMA access, and the hardware does not require a **wait state**.

Data Polarity

The VMICPCI-1335 has negative I/O data polarity. This means that when the applied input voltage causes the optocoupler to be active (turned on) it will result in a 0 being seen at the CompactPCI bus.

Input Circuitry

Figure 1-2 shows the basic topology for each input. The open-collector output of the optoisolator goes to an Input Data Register (IDR). When a CompactPCI bus read is performed on the input port, the Input Data Register latches the data present at the output of the optoisolator. The data is held in these registers while the on-board control logic steers the data to the appropriate CPCI bus data lines.

Resistor R_{VS} is an option-dependent, current-limiting resistor. The value of this resistor is selected during manufacturing to provide the typical threshold specified for the one of five available options ordered. The pull-up resistor is provided in the contact sensing mode, and the resistance value is selected during manufacturing depending on the option ordered.

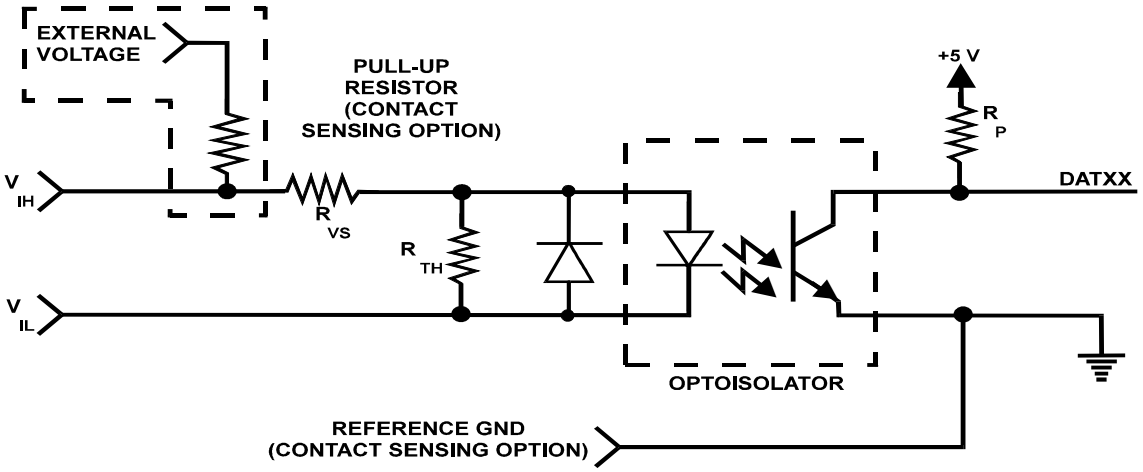


Figure 1-2 Typical Input Configuration

Input Types

The inputs can be configured for one of two types, either as Voltage Sensing or Contact Sensing. Pull-up resistors are provided for Contact Sensing and may be driven by an external voltage supplied by the user (see Figure 2-1 on page 36 and Table 2-1 on page 37). If the Contact Sensing option is selected, the user may need to use the reference ground pin provided on P1, pin1. The signal is intended to provide a monitoring reference ground only, not to be used as a current return.

Note

Since the reference ground input bypasses the optical isolators, the application of high voltage (perhaps due to a fault condition in the field) may cause damage to the PCI bus host.

Configuration Space

This portion of the theory of operation defines the programming model and usage rules for the configuration register space in PCI and CompactPCI compliant devices. The intent of the configuration space definition is to provide an appropriate set of configuration *hooks* which satisfies the needs of current and anticipated system configuration mechanisms.

Configuration Space Organization

This section defines the organization of configuration space registers and imposes a specific record structure or template on the 256-byte space. This space is divided into a predefined header region and a device-dependent region. Devices implement only the necessary and relevant registers in each region. A device's configuration space must be accessible at all times, not just during system boot. The predefined header region has a size of 64 byte and every device must support the register layout of this region. This region consists of fields that uniquely identify the device and allow the device to be generically controlled. See Figure 1-3 on page 23.

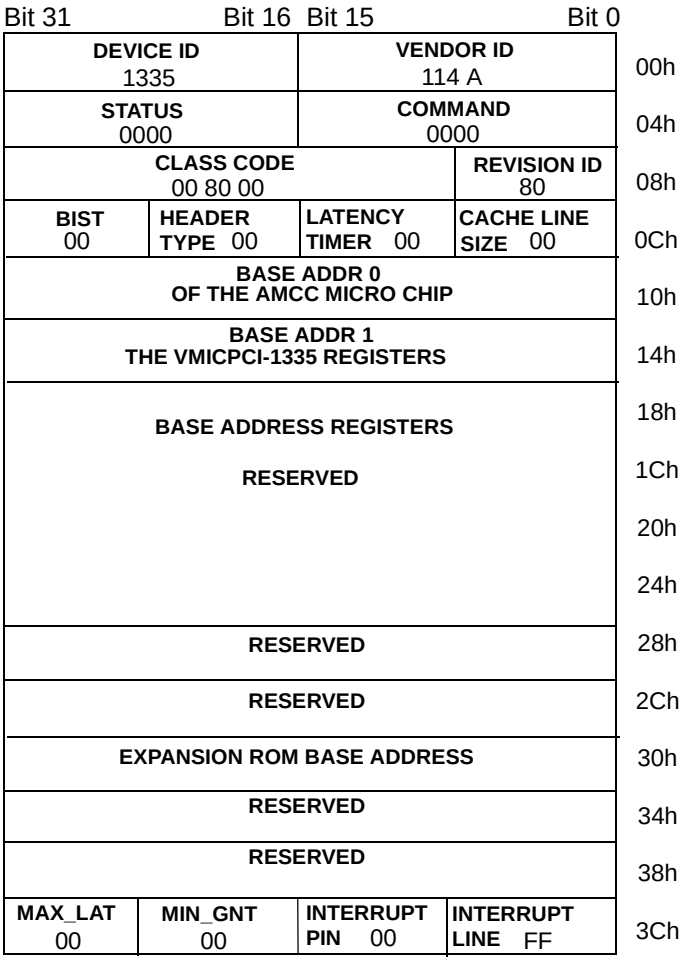


Figure 1-3 Configuration Space Header

All compliant devices must support the Vendor ID, Device ID, Command and Status fields in the header. Implementation of other registers is optional (that is, they can be treated as reserved registers) depending on device functionality. If a device supports the function that the register is concerned with, the device must implement it in the defined location and with the defined functionality.

Configuration Space Functions

The CompactPCI bus has the potential for greatly increasing the ease in which systems may be configured. To realize this potential, all CompactPCI bus devices must provide certain functions that system configuration software can utilize. This section also lists the functions that need to be supported by CPCI bus devices by way of registers defined in the predefined header portion of the configuration space. The exact format of these registers (that is, number of bits implemented) is device-specific. However, some general rules must be followed. All registers must be capable of being read back and the data returned must indicate the value that the device is actually using.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions. Its use should be restricted to initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers.

Device Identification

Five fields in the predefined header deal with device identification. All PCI bus devices are required to implement these fields. Generic configuration software will be able to easily determine what devices are available on the system's CPCI bus(ses). All of these registers are read-only.

Vendor ID	This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 114A is VMIC's vendor ID.
Device ID	This field identifies the particular device. This identifier is allocated by the vendor. The Device ID for the VMICPCI-1335 is 1335.
Revision ID	This register specifies a device-specific revision identifier. The value is chosen by the vendor. **80** is the assigned value.
Header Type	This byte identifies the layout of locations 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. Bit 7 in this register is used to identify a multifunction device. If the bit is 0, then the device has multiple functions. Bits 6 through 0 specify the layout of addresses 10h through 3Fh. One encoding, 00h, is defined and specifies the layout shown in Figure 1-3 on page 23. All other encodings are reserved.
Class Code	The Class Code register is used to identify the generic function of the device. The register is broken into three byte-size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a subclass code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device-independent software can interact with the device.

Device Control

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the CompactPCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's

functionality. For instance, devices that do not implement an I/O space probably will not implement a writable element at bit location 0 of the Command register. Devices typically come up with all zeros in this register. Figure 1-4 shows the layout of the register and Table 1-1 on page 25 explains the definitions of the different bits in the Command register.

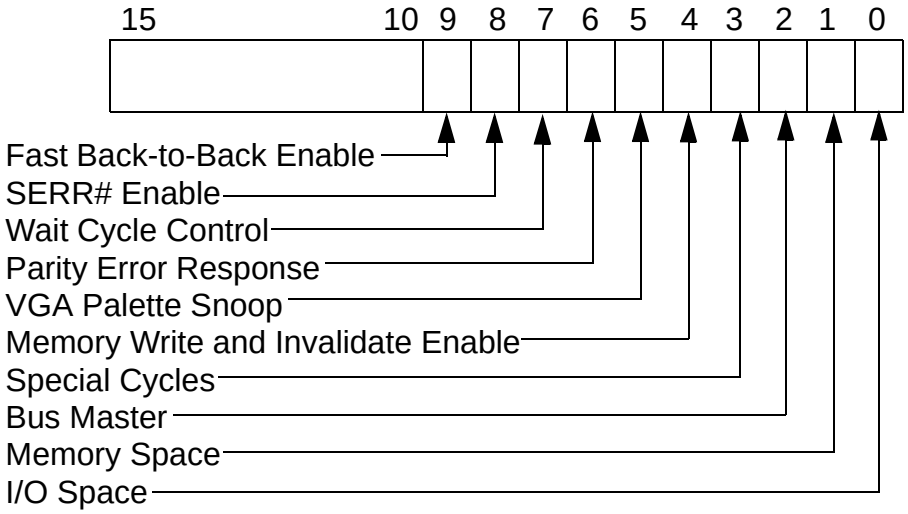


Figure 1-4 Command Register Layout

Table 1-1 Command Register Bits

Bit Location	Bit Definitions
0	Controls a device's response to I/O space accesses. A value of zero disables the device response. A value of 1 allows the device to respond to I/O space accesses. State after RST# is 0.
1	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to memory space accesses. State after RST# is 0.
2	Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. State after RST# is 0.
3	Controls a device's action on Special Cycle Operations. A value of 0 causes the device to ignore all Special Cycle Operations. A value of 1 allows the device to monitor Special Cycle Operations. State after RST# is 0.

Table 1-1 Command Register Bits (Continued)

Bit Location	Bit Definitions
4	This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When this bit is 0, Memory Write must be used instead. State after RST# is 0. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
5	This bit controls how VGA-compatible devices handle accesses to VGA palette registers. When this bit is 1, special palette snooping behavior is enabled (that is, device must not respond). When the bit is 0, the device should treat palette accesses like all other accesses. VGA-compatible devices should implement this bit.
6	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device must ignore any parity errors that it detects and continue normal operation. This bit's state after RST# is 0. Devices that check parity must implement this bit. Devices are still required to generate parity even if parity checking is disabled.
7	This bit is used to control whether or not a device does address / data stepping. Devices that never do stepping must have this bit hardwired to 0. Devices that always do stepping must have this bit hardwired to 1. Devices that can do either should make this bit read / write and have it initialize to 1 after RST#.
8	This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. This bit's state after reset is 0. All devices that have an SERR# pin must implement this bit. This bit (and bit 6) must be ON to report address parity errors.
9	This optional read / write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transactions to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent.
10-15	Reserved

Device Status

The Status register is used to record status information for CompactPCI bus-related events. The definition of each of the bits is given in Table 1-2 on page 28, and the layout of the register is shown in Figure 1-5 on page 27. CompactPCI devices do not need to implement all bits, depending on device functionality. For instance, a device that acts as a target but will never signal target-abort, would not implement bit 11.

Reads to this register behave normally. Writes are slightly different in that the bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

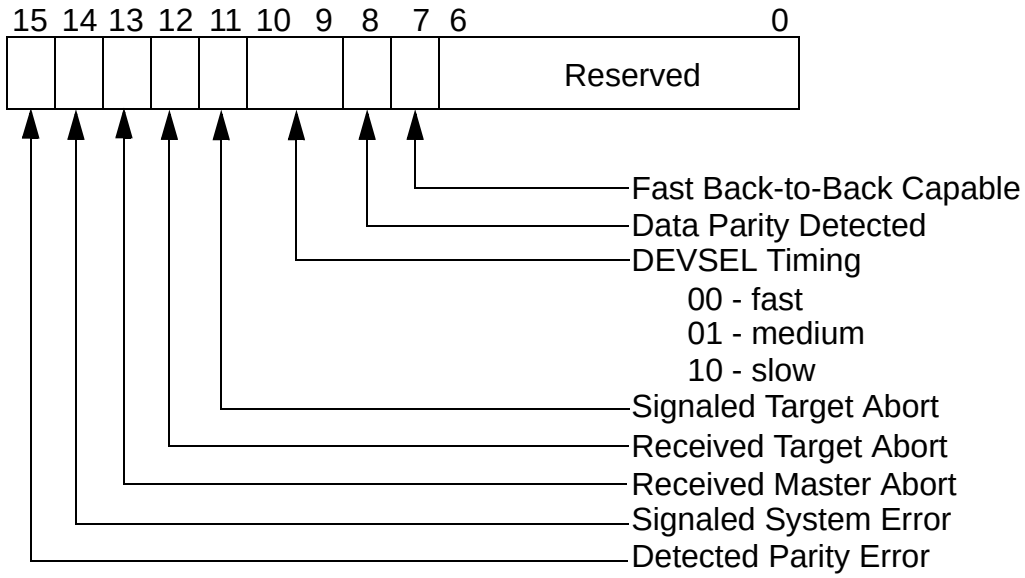


Figure 1-5 Status Register Layout

Table 1-2 Status Register Bits

Bit Location	Descriptions
0 through 6	Reserved
7	This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions, and must be set to 0 otherwise.
8	This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.
9 and 10	These bits encode the timing of DEVSEL#. The bits are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.
11	This bit must be set by a target device whenever it terminates a transaction with Target-Abort. All master devices must implement this bit.
12	This bit must be set by a master device whenever the target terminates a transaction with Target-Abort. All master devices must implement this bit.
13	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
14	This bit must be set whenever the device asserts SERR#. Devices which will never assert SERR# do not need to implement this bit.
15	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled as controlled by bit 6 in the Command register.

Interrupt Line

The VMICPCI-1335 CompactPCI bus board does not utilize interrupts.

Base Addresses

One of the most important functions for enabling superior configurability and ease-of-use is the ability to relocate PCI devices in the address spaces. At system powerup, device-independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM. Each of these areas is covered in the following sections.

Address Maps

Powerup software needs to build a consistent address map before booting the machine to an operating system. This means it must determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, powerup software can map the I/O controllers into reasonable locations and proceed with system boot. In order to do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space.

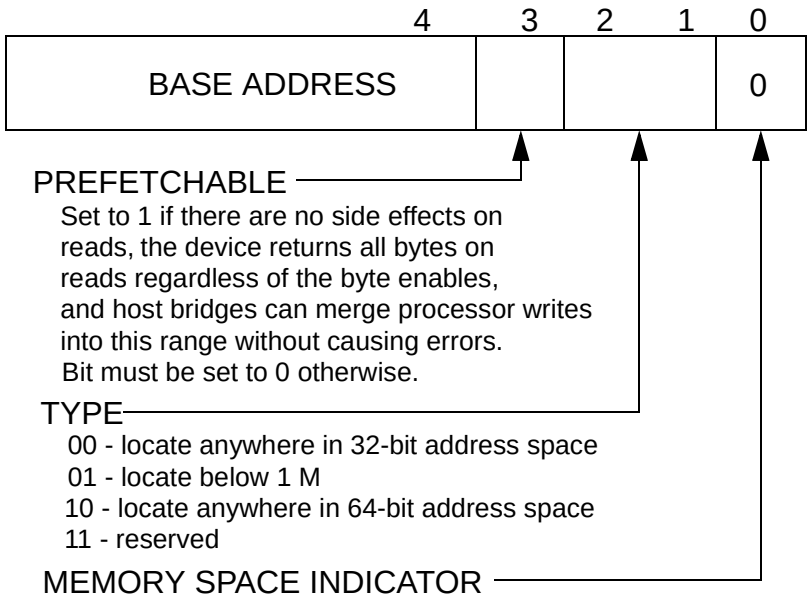


Figure 1-6 Base Address Register for Memory

Bit 0 in all base registers is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a 0 in bit 0. Base registers that map to I/O space must return a 1 in bit 0.

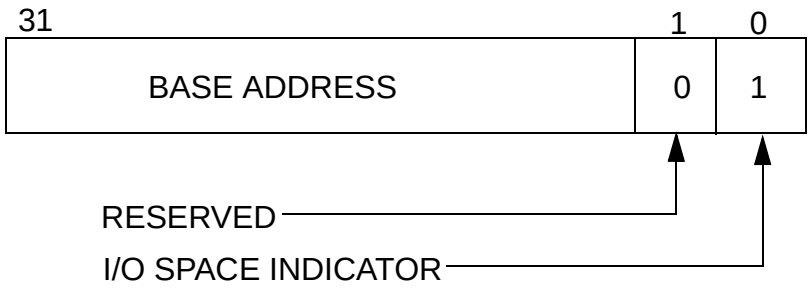


Figure 1-7 Base Address Register for I/O

Base registers that map into I/O space are always 32-bit with bit 0 hardwired to a 1, bit 1 is reserved and must return 0 on reads, and the other bits are used to map the device into I/O space.

Base registers that map into Memory space (Figure 1-6 on page 29 can be 32-bit wide to support mapping into a 64-bit address space) with bit 0 hardwired to a 0. For memory base registers, bits 2 and 1 have an encoded meaning as shown in Table 1-3 below. Bit 3 should be set to 1 if the data is prefetchable, and reset to 0 otherwise. A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bits 0 through 3 are read-only.

Table 1-3 Bits 2/1 Encoding

Bits 2/1	Definition
00	Base register is 32-bit wide, and mapping can be done anywhere in the 32-bit memory space.
01	Base register is 32-bit wide, but must be mapped below 1 Mbyte in memory space.
10	Base register is 64-bit wide, and can be mapped anywhere in the 64-bit address space.
11	Reserved

The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. A device that wants a 1 Mbyte memory address space (using a 32-bit base address register) would build the top 12-bit of the address register hardwiring the other bits to 0.

Powerup software can determine how much address space the device requires by writing a value of all ones to the register and then reading the value back. The device will return zeros in all *don't care* address bits, effectively specifying the address space required.

This design implies that all address spaces used are a power of two in size, and are naturally aligned. Devices are free to consume more address space than required, but decoding down to a 4 Kbyte space for memory and 256 byte for I/O is suggested for devices that need less than those amounts. Devices that do consume more address space than they use are not required to respond to the unused portion of that address space.

Six DWORD locations are allocated for Base Address registers starting at offset 10h in configuration space. The first Base Address register is always located at offset 10h. The second register may be at offset 14h or 18h depending on the size of the first. The offsets of subsequent Base Address registers are determined by the size of previous Base Address registers.

The Base Address of the AMCC Micro is found at offset 10h, with the Base Address of the VMICPCI-1335 registers found at offset 14h.

A typical device will require one memory range for its control functions. Some graphics devices may use two ranges, one for control functions and another for a frame buffer. A device that wants to map control functions into both memory and I/O space at the same time must implement two base registers (one Memory, one I/O). The driver for that device might only use one space in which case the other space will be unused. Devices should always allow control functions to be mapped into memory space.

Any device that has a range that behaves like normal memory, but doesn't participate in PCI's caching protocol, should mark the range as prefetchable. A linear frame buffer in a graphics device is an example of a range that should be marked prefetchable.

Refer to the *PCI Local Bus Specification Revision 2.1* sheet for detailed information about the PCI bus. Refer to the *CompactPCI Bus Specification, 2.0 R2.1* sheet for CompactPCI bus information. The contact information to order these specification sheets is given in the *Related Documents* section on page 13 of this manual.

CHAPTER
2

Configuration and Installation

Contents

Introduction

For a physical description and specifications, refer to the 800-651335-000 specification sheet.

Unpacking Procedures

Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that may have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. This board can be installed in any slot position with a circle above the handle and also on the backplane, the slot with a triangle above the handle is reserved for the system controller.

This symbol identifies the System Controller slot

This symbol identifies the slot inwhich the VMICPCI-1335 can be installed

Do not install or remove the board while power is applied.

Before Applying Power: Checklist

Before installing the board in a CompactPCI bus system, check the following items to ensure that the board is ready for the intended application.

1. Verify that the sections pertaining to theory of operation and programming, (Chapter 1 and Chapter 3), have been reviewed and applied to system requirements. ____
2. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to *Connector Configuration* on page 39 for connector descriptions. _____

After the checklist above has been completed, the board can be installed in a CompactPCI bus system.

Board Configuration

The VMICPCI-1335 board is factory configured for voltage sensing or contact sensing modes. The contact sensing mode provides the user with two external voltage pins at P1, one per eight channels.

Input Topology

Figure 2-1 shows the circuit topology for contact sensing inputs. Figure 2-2 shows the circuit topology for the voltage sensing configuration. Table 2-1 on page 37 shows the two external voltage inputs and the input channels affected by each.

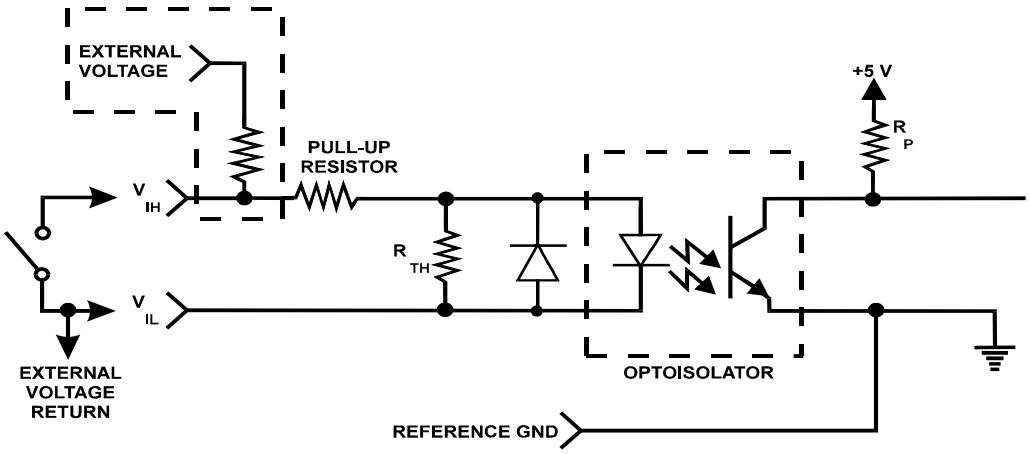


Figure 2-1 Typical Contact Sense Input

Note

Channel-to-channel isolation is on byte-to-byte boundary for Contact Sense Input option.

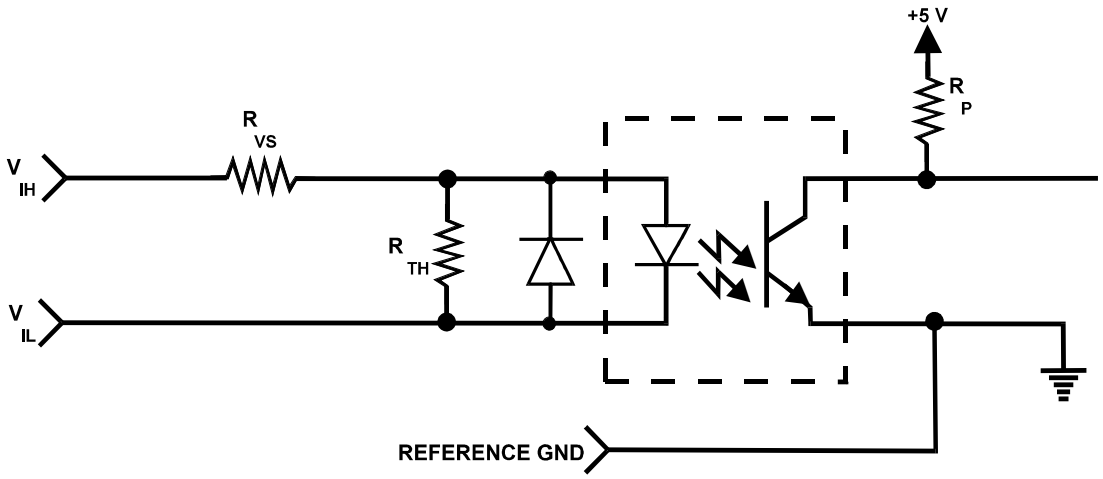


Figure 2-2 Typical Voltage Sense Input

Table 2-1 External Voltage

External Voltage	Channels Affected	P1 Pin
VEXT 0	Input Channels 0 through 7	21
VEXT 1	Input Channels 8 through 15	3

Address Selection

The VMICPCI-1335 board occupies 64 byte (16 longwords) of I/O and memory space. The choice of 64 bytes is dictated by some PCI hosts which do not properly recognize less. In fact, only the first four bytes (1 longword) are of interest The remaining 15 longwords are just copies of the first. The actual absolute I/O address space is found at location 14h offset and the actual absolute memory address space is found at location 18h of the configuration space (along with all other CompactPCI devices) as per PCI and CompactPCI requirements.

Connector Configuration

The panel input connector (P1) on the VMICPCI-1335 board is a standard subminiature 37-pin male D-Shell. Figure 2-4 on page 40 shows the pin layout of the P1 connector. Table 2-3 on page 40 details the connector pin assignments. The J1 connector on the VMICPCI-1335 is a 2 mm Din 32-bit, 5 V, CompactPCI bus connector. The metal shell (row F) of the J1 connector is connected to chassis ground. See the figure and table below for the J1 connector pinout.

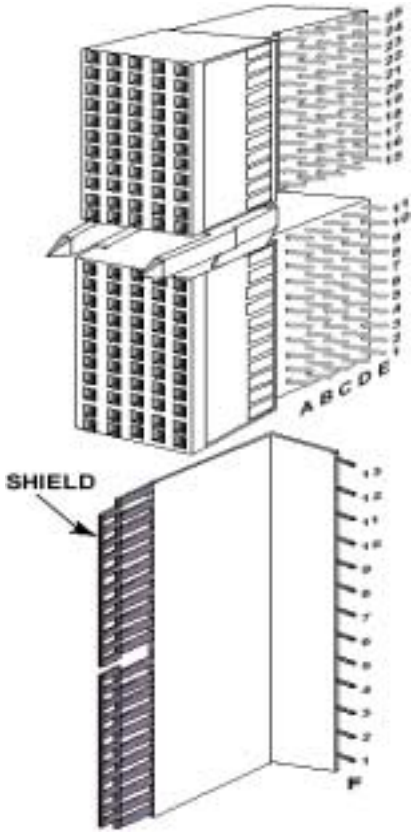


Figure 2-3: J1 Connector

Table 2-2: J1 Connector Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
25	+5 V	N/C	N/C	N/C	+5 V	GND
24	IN_AD[1]	+5 V	+5 V	IN_AD[0]	N/C	N/C
23	N/C	IN_AD[4]	IN_AD[3]	+5 V	IN_AD[2]	GND
22	IN_AD[7]	GND	N/C	IN_AD[6]	IN_AD[5]	N/C
21	N/C	IN_AD[9]	IN_AD[8]	GND	INC/BE[0]	GND
20	IN_AD[12]	GND	N/C	IN_AD[11]	IN_AD[10]	N/C
19	N/C	IN_AD[15]	IN_AD[14]	GND	IN_AD[13]	GND
18	INSERR	GND	N/C	INPAR	INC/BE[1]	N/C
17	N/C	N/C	N/C	GND	INPERR	GND
16	IN_DEVSEL	GND	+5 V	INSTOP#	INLOCK	N/C
15	N/C	IN_FRAME	INIRDY	GND	INTRDY	GND
12 through 14 are lost to the keying area						
11	IN_AD[18]	IN_AD[17]	IN_AD[16]	GND	INC/BE[2]	GND
10	IN_AD[21]	GND	N/C	IN_AD[20]	IN_AD[19]	N/C
9	INC/BE[3]	INIDSEL	IN_AD[23]	GND	IN_AD[22]	GND
8	IN_AD[26]	GND	+5 V	IN_AD[25]	IN_AD[24]	N/C
7	IN_AD[30]	IN_AD[29]	IN_AD[28]	GND	IN_AD[27]	GND
6	N/C	GND	N/C	CLK	IN_AD[31]	N/C
5	N/C	N/C	INRST	GND	N/C	GND
4	N/C	GND	+5 V	N/C	N/C	N/C
3	INTA	N/C	N/C	+5 V	N/C	GND
2	N/C	+5 V	N/C	N/C	N/C	N/C
1	+5 V	N/C	N/C	N/C	+5 V	GND

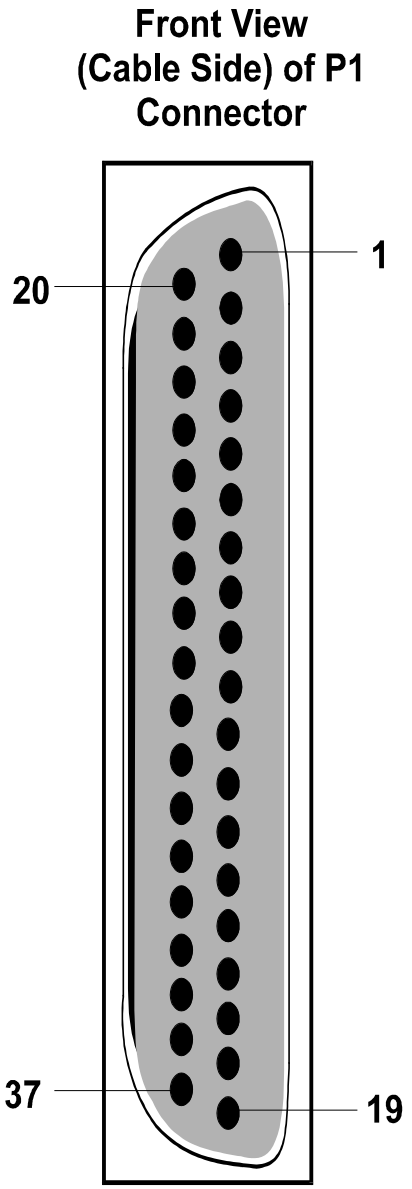


Figure 2-4 P1 Connector Pin Layout

Table 2-3 :P1 Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
20	N/C	1	REF GND
21	VEXT 0	2	N/C
22	LOW IN 15	3	VEXT 1
23	LOW IN 14	4	HIGH IN 15
24	LOW IN 13	5	HIGH IN 14
25	LOW IN 12	6	HIGH IN 13
26	LOW IN 11	7	HIGH IN 12
27	LOW IN 10	8	HIGH IN 11
28	LOW IN 9	9	HIGH IN 10
29	LOW IN 8	10	HIGH IN 9
30	LOW IN 7	11	HIGH IN 8
31	LOW IN 6	12	HIGH IN 7
32	LOW IN 5	13	HIGH IN 6
33	LOW IN 4	14	HIGH IN 5
34	LOW IN 3	15	HIGH IN 4
35	LOW IN 2	16	HIGH IN 3
36	LOW IN 1	17	HIGH IN 2
37	LOW IN 0	18	HIGH IN 1
		19	HIGH IN 0
Shield			GND

CHAPTER 3

Programming

Contents

Introduction

The VMPCPCI-1335 board requires very little software. Although the VMICPCI-1335 reserves 64 bytes in I/O and memory space, only 4 bytes (1 Longword) are used. User Register 1 is composed of the Data Register and the Control Status Register (CSR) as shown in Figure 3-1 below, and can be in either I/O or memory space.

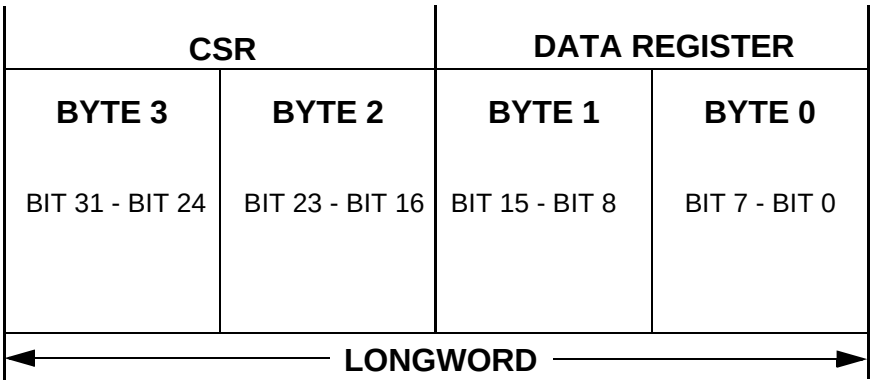


Figure 3-1 User Register 1

Control and Status Register (CSR)

Bytes 3 and 2 of the I/O address space comprise the Control and Status Register for the VMICPCI-1335 board. The CSR is a 16-bit register that is used to control the board's Fail LED and Debounce timer for all channels. Table 3-1 shows the position of the bits used to perform these functions.

Table 3-1 Control and Status Register Bit Map (User Register 1)

Control and Status Register, Byte 3, Fail LED (Read/Write)							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Reserved							LED

Control and Status Register, Byte 2, Debounce Timer (Read/Write)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved					DD 2	DD 1	DD 0

Control and Status Register Bit Definition

Bits 31 to 25:Reserved These bits are reserved and will always read back as low. Data written to these locations will be lost and has no effect on the board. However, these bits should be written to 0 to maintain software compatibility for possible future enhancements which may utilize any one of them.

Bit 24: LED **Fail LED Bit**. Writing this bit high will turn the Fail LED off. At powerup or reset, the bit is set low and the Fail LED is on.

Bits 23 to 19:Reserved These bits are reserved and will always read back as low. Data written to these locations will be lost and has no effect on the board. However, these bits should be written to 0 to maintain software compatibility for possible future enhancements which may utilize any one of them.

Bits 18 to 16:DD 2-0 **Debounce Delay Bits 2-0**. These three bits control the Debounce timer for all 16 inputs. They are used to select one of the eight possible debounce delays for the opticoupled inputs. At powerup or reset, these bits will default to 000 (1 µs delay). Table 3-2 on page 43 lists the delays selected by the different bit combinations.

Table 3-2 Debounce Delay

CSR Bits			Debounce Delay
18	17	16	
0	0	0	1.0 µs
0	0	1	128 µs
0	1	0	256 µs
0	1	1	512 µs
1	0	0	3.07 ms
1	0	1	6.14 ms
1	1	0	9.22 ms
1	1	1	12.29 ms

Note

Inputs to the VMICPCI-1335 board are debounced by one of the selected debounce times shown above. The data is registered and delayed, again by the debounce time interval before the data is presented to the user. In some tests, this gives the impression that the actual time interval is twice as long as it really is.

Input Register Bit Definitions

Table 3-3 lists the input channels and their associated register bit locations. The Input Data Register can be read as a Byte, Word, or Longword.

Table 3-3 Input Data Register Bit Map (User Register 1)

Input Data Register, Byte 1 (Read-Only)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08

Input Data Register, Byte 0 (Read-Only)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

Data Polarity

The VMICPCI-1335 board has negative I/O data polarity. This means that when the applied input voltage causes the optocoupler to be active (turned on) it will result in a zero (0) being seen at the CPCI bus.

A logic HIGH (1) (voltage applied) on an voltage sensing input results in a logic LOW (0) being read from the register.

A logic HIGH (1) (relay open) on a contact sensing input results in a logic LOW (0) being read from the register.

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

1. Software
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

VMIC's Customer Service can be reached by any of the following:

Direct: 256-650-8398

Toll-Free Direct: 800-240-SRVC (7782)

FAX: 256-650-7245

Email: Customer.Service@vmic.com

Maintenance Prints

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.