VMICPCI-2140
8-Channel Triac-Driven Optically Coupled CompactPCI AC Output Board

Product Manual

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Overview

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Introduction

The VMICPCI-2140 8-Channel Triac Driven Optically Coupled AC Output board is designed to provide isolation between the 120/250 VAC lines and the CompactPCI chassis. The eight optically coupled outputs provide a sustained 1 kV of system isolation to the CompactPCI backplane. The VMICPCI-2140 can be used to control resistive, inductive, or capacitive loads, including motors, solenoids, high current thyristors or triacs and relays. Applications include solid-state relays and industrial controls.

The VMICPCI-2140 board has several features as specified below.

- Full hot swap CompactPCI compliant and high availability
- Eight optically coupled Triac-Driven outputs
- High isolation potential
  -- 1 K VACrms sustained (channel-to-PCI bus)
- Galvanic (channel-to-channel) isolation to 600 V
- 8-, 16-, or 32-bit data transfers (single or burst modes)
- Memory addressing
- 250 Vrms maximum output voltage
- 300 mA current sinking outputs (RMS)
- Channel Status LEDs
- Fail LED
- 3U Eurocard front panel with removable screw terminals
- Field replacable fuses
- Complies with *PCI specification Version 2.2 (V2.2)*
- Complies with *Hot Swap CompactPCI Specification PICMG 2.1 R1.0*

Functional Description

The output circuitry of the VMICPCI-2140 board is designed around eight identical zero voltage crossing Triac Driver Optocouplers. There are no pull-up resistors on the output channels. The VMICPCI-2140 implements the Siemens IL420 zero crossing Triac, which can only be triggered during the zero crossing of the AC voltage Sine wave. This prevents current spikes, e.g., when turning on cold lamps or capacitive loads. The user supplies voltage to pins 1 through 16 on the front panel interface connector (P1).

The VMICPCI-2140 has an independent register for each channel, allowing control of the ON/OFF state of the outputs and providing control for the Fail LED. Writing a one (1) to bit 7 of the channel offset address turns the channel ON. Writing a zero (0) to bit 7 of the channel offset address turns the channel OFF. The Fail LED is a status indicator under user software control. The default reset condition of the Fail LED is ON. This does not indicate a failure of the board.

Reference Material List

Refer to *PCI Local Bus Specification* for a detailed explanation of the PCI Local bus. The PCI Local bus Specification is available from the following source:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
U.S.: (800) 433-5177
International: (503) 797-4207
FAX: (503) 234-6762

For a detailed explanation of the CompactPCI™ bus and its characteristics, refer to the *CompactPCI™ Specification, 2.0 R2.1* from:

PCI Industrial Manufacturers Group
(PICMG)
301 Edgewater Place
Suite 220
Wakefield, MA 01880 USA
(617) 224-1100
(503) 797-4207 (International)
Fax: (617) 224-1239
Web: http://www.PICMG.ORG

For a detailed explanation of the PLX PCI 9054 Interface IC, refer to the *PCI 9054 Data Book Version 1.0 Order Number: 1030-54000-DTB* from:

PLX Technology, INC.
390 Potrero AVE
Sunnyvale, CA 94089
(800) 759-3735
(408) 774-9060
Web: http://www.plxtech.com

For a detailed explanation of the Infineon Technologies IL410 Triac Outputs, refer to the *Infineon Technologies, Corp Optoelectronics (April 1999)* from:

Infineon Technologies, Corp, Optoelectronics Division
Cupertino, CA
(800) 777-4363
Web: http://www.infineon.com/opto

Physical Description and Specifications

Refer to 800-652140-000 specification, available from VMIC.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

Safety Symbols Used in This Manual

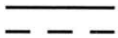
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

STOP The STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING WARNING calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION CAUTION calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE NOTE calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER 1

Theory of Operation

Contents

Introduction

The following sections describe the functionality of the VMICPCI-2140 board. This discussion includes the VMICPCI-2140's role in the system hardware architecture as well as important individual registers located on the board itself.

Operational Overview

The VMICPCI-2140 board is designed to provide eight optically coupled Triac outputs as well as isolation between the AC voltage output channels and the CompactPCI bus. The output voltage and current levels are determined by the system hardware to which it is connected (250 Vrms max).

The VMICPCI-2140 board address is assigned by the system BIOS during system power-up per the PCI specification. By executing a write cycle to the data registers, data is steered from the backplane to the Output Data Registers (ODR). The data stored in these registers is used to drive the Triac output and the status LED to the field.

Figure 1-1 is a block diagram of the basic functions of the VMICPCI-2140 board. These blocks will be discussed in more detail in the following sections.

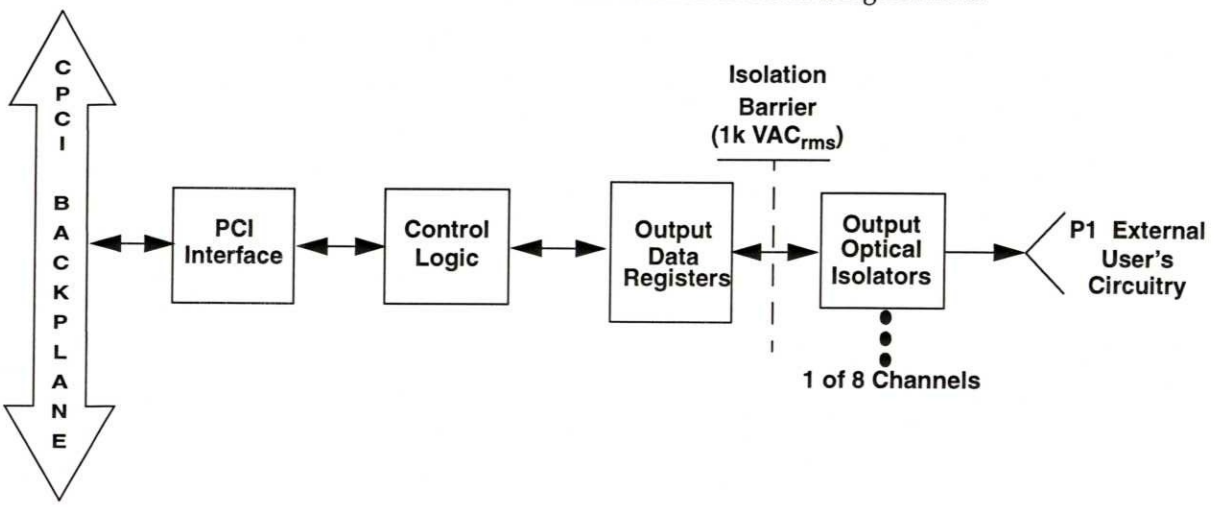


Figure 1-1 VMICPCI-2140 Functional Block Diagram

CompactPCI Hot Swap Compliance

This product conforms with all requirements of a fully hot swappable board as defined by the *Hot Swap Specification PICMG 2.1 R1.0*. Futhermore, it is capable of operating in a high availability system.

PCI Local Bus Compliance

The VMICPCI-2140 board is a *PCI Specification 2.2* compliant add-on slave board. The board occupies 256 bytes of memory space and can be mapped into any PCI memory space. The board does not utilize interrupts or DMA access and the hardware does not require a "wait state."

Data Polarity

The VMICPCI-2140 board has positive true output data polarity. On the PCI bus, when a one (1) is written to an output, the Triac output transistor will be active (turned on).

Channel Control Registers

The Channel Control Registers can be accessed with 8-, 16-, or 32-bit data transfers (single or burst mode). Refer to the table below for the Channel Control register definitions and offset addresses.

31	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFFF	0	0	1	0	0	0	0	1	R/W	0	0	0	0	0	0	0

Bit-7 of the individual channel offset address controls the Triac outputs. A logic HIGH (1) turns the Triac output ON. A logic LOW (0) turns the Triac output OFF. Default is zero (0). A reset will cause the Triac outputs to be inactive (zero (0)).

Bits 8 through 15 will always read $21, which is the upper bits of the Board ID register.

Table 1-1 Channel Control Registers Offset Addresses

Channel No.	Offset Address
0	$40 (Bit-7) only
1	$44 (Bit-7) only
2	$48 (Bit-7) only
3	$4C (Bit-7) only
4	$50 (Bit-7) only
5	$54 (Bit-7) only
6	$58 (Bit-7) only
7	$5C (Bit-7) only

Status LEDs

The Channel Control registers control the Status LEDs. Bit 7 of the Individual Channel Offset Address controls the Triac outputs and the Individual Channel Status LED. A logic LOW (0) turns the Triac and the corresponding status LED off. A logic HIGH (1) turns the Triac and status LED on. The Default configuration is a logic LOW (0) off.

Output Circuitry

Figure 1-2 shows the basic topology of each output. The information stored in the Output Data Register from a PCI bus write is gated to the LED of the optocoupler, which turns the channels output ON or OFF.

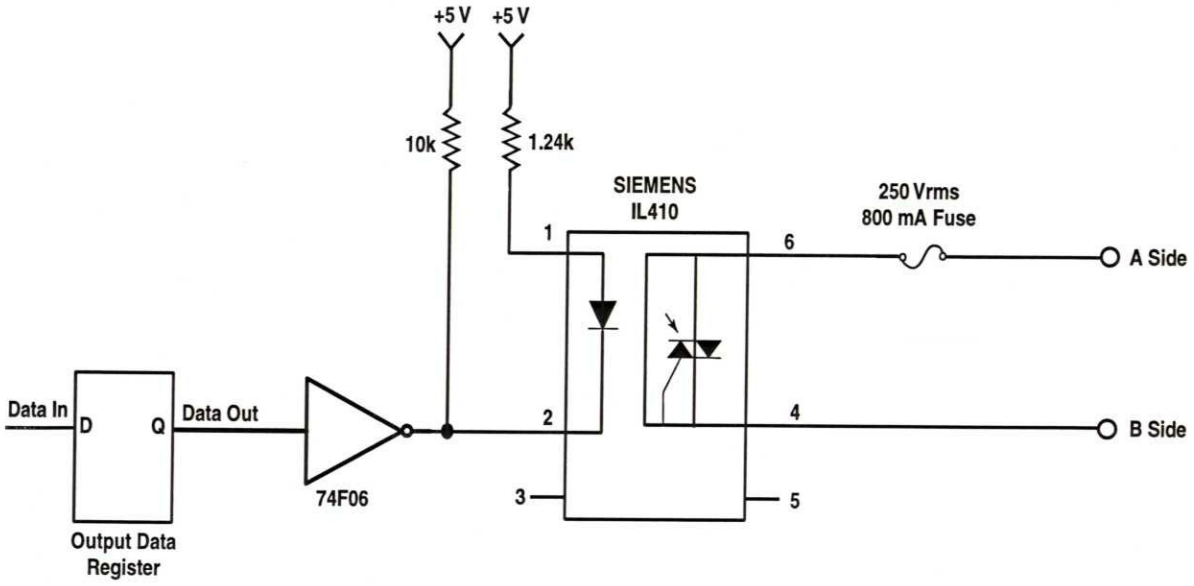


Figure 1-2 Typical Output Configuration

Output Types

The VMICPCI-2140 implements the Siemens IL410 Zero Crossing Triac Driver Optocoupler for each of the eight current sinking outputs. The outputs withstand switching of a maximum voltage of 250 Vrms and 300 mA rms on state current. The outputs also provide a very low leakage current of 10 µA typical in the off state. Typical Turn-On/Turn-Off time is 35 µs and 50 µs respectively.

The IL410 with a zero voltage switch can only be triggered during zero crossing of the sine AC voltage. This prevents current spikes when turning ON cold lamps or capacitive loads.

Fuses

Each Triac output is protected with a field replaceable fuse rated for 250 Vrms at 800 mA. Replacement fuses can be obtained from VMIC (part number 343-000015-080) or from Wickmann (Vendor part number 370-0800041).

CHAPTER 2

Configuration and Installation

Contents

Introduction

This chapter describes the setup and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for:

- broken components
- damaged circuit board(s)
- heat damage
- Any visible contamination.

All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

This board can be installed in any slot position with a circle on the backplane; the slot with a triangle on the backplane is reserved for the system controller.

This symbol identifies the System Controller slot.

This symbol identifies the slots in which the VMICPCI-2140 can be installed.

Before Applying Power: Checklist

Before installing the board in a CompactPCI system, check the following items to ensure that the board is ready for the intended application.

1. Verify that the sections pertaining to theory and programming, Chapters 1 and 3, have been reviewed and applied to system requirements.
2. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to *Connector Configuration* section on page 29 for connector descriptions.

After the checklist above has been completed, the board can be installed in a CompactPCI system.

Physical Installation and Hot Swap

The VMICPCI-2140 is a Hot Swap compliant device. Hot Swap functionality allows the orderly insertion and removal of boards without adversely affecting system operation. The VMICPCI-2140 uses two signals, ENUM# and LEDon/LEDin, to implement the hardware aspect of the Hot Swap functionality, and also the Hot Swap Capabilities register (**Hot Swap Control and Status Register – HS_CSR**) to implement the software aspects of the Hot Swap capabilities.

Board Removal, Ejector Switch and Blue LED

A microswitch (switch), located in the card-ejector mechanism of the VMICPCI-2140 is used to signal the impending removal of a board. This signal asserts ENUM#. The operator normally activates the switch, waits for the Blue LED illumination to indicate it is okay to remove the board and then removes the board.

Board Insertion

Upon insertion, the Blue LED is automatically illuminated by the VMICPCI-2140 hardware until the hardware connection process is completed. After the connection process is completed and the 2140 board has been configured, the Blue LED is extinguished and remains OFF until the software uses it to indicate extraction is permitted.

ENUM# and LEDon/LEDin Signals

ENUM# is a signal provided on the backplane that notifies the host that a board has been freshly inserted or is about to be removed. This signal informs the user that configuration of the system has changed. The user then performs any necessary maintenance such as installing a device driver upon board insertion or quiescing a device driver prior to board extraction.

ENUM# is an open collector bused CompactPCI signal with a pull-up on the Host. It can drive an interrupt or be polled by the system software. The CompactPCI Hot Swap System Driver on the system host manages the ENUM# sensing.

LEDon/LEDin is a signal in the VMICPCI-2140 board that senses the position of the ejector handle on the front panel.

When a board is inserted into the system and reset, the VMICPCI-2140 acknowledges the state of the ejector switch. If this switch is open (ejector closed) the VMICPCI-2140 asserts ENUM# and sets the ENUM# Status Indicator for board insertion bit (HS_CSR[7]).

When a board is about to be removed, the VMICPCI-2140 acknowledges the ejector switch is closed (ejector open), asserts ENUM#, and sets the ENUM# Status Indicator for board removal bit (HS_CSR[6]). The user software turns ON the blue LED; the operator can then completely remove the board from the chassis.

Address Selection

The VMICPCI-2140 board occupies 256 bytes (64 Longwords) of memory space. The actual absolute memory address space is assigned at configuration time (along with all other PCI devices) as per PCI requirements.

The Base Address of the PLX 9054 is located at offset $10 (Base Address 0) of the Configuration registers.

The Base Address of the VMICPCI-2140 is found in offset $18 (Base Address Register 2) of the Configuration registers. Once the VMICPCI-2140 board's base address is obtained, the Channel Control registers, Board ID register, and the Fail LED register can be found using the Memory Space map below.

Memory Space Definition

The VMICPCI-2140 board reserves 256 bytes of memory space. Table 2-1 shows the VMICPCI-2140 Memory Space Map window. All registers except for the Board ID register (Read-Only) can be written to or read from using Byte, Word, or Longword (Lword) accesses. Burst mode is also supported.

Table 2-1 VMICPCI-2140 Memory Space Map

Register	PCI Offset Address	Description	Mnemonic	Value at Reset
Board ID	$04	Board ID	BID	$2140
Fail LED	$10 (Bit 7)	Fail LED	Fail_LED	$2180
Channel 0	$40 (Bit 7)	Channel Control 0	CCR0	$2100
Channel 1	$44 (Bit 7)	Channel Control 1	CCR1	$2100
Channel 2	$48 (Bit 7)	Channel Control 2	CCR2	$2100
Channel 3	$4C (Bit 7)	Channel Control 3	CCR3	$2100
Channel 4	$50 (Bit 7)	Channel Control 4	CCR4	$2100
Channel 5	$54 (Bit 7)	Channel Control 5	CCR5	$2100
Channel 6	$58 (Bit 7)	Channel Control 6	CCR6	$2100
Channel 7	$5C (Bit 7)	Channel Control 7	CCR7	$2100
---	$60 through $FF	Reserved	---	---

Fuses

The VMICPCI-2140 uses field replaceable fuses. Each channel has a corresponding fuse. The fuses are 250 VAC, with a 800 mA rating. The following figure illustrates the location of the fuses.

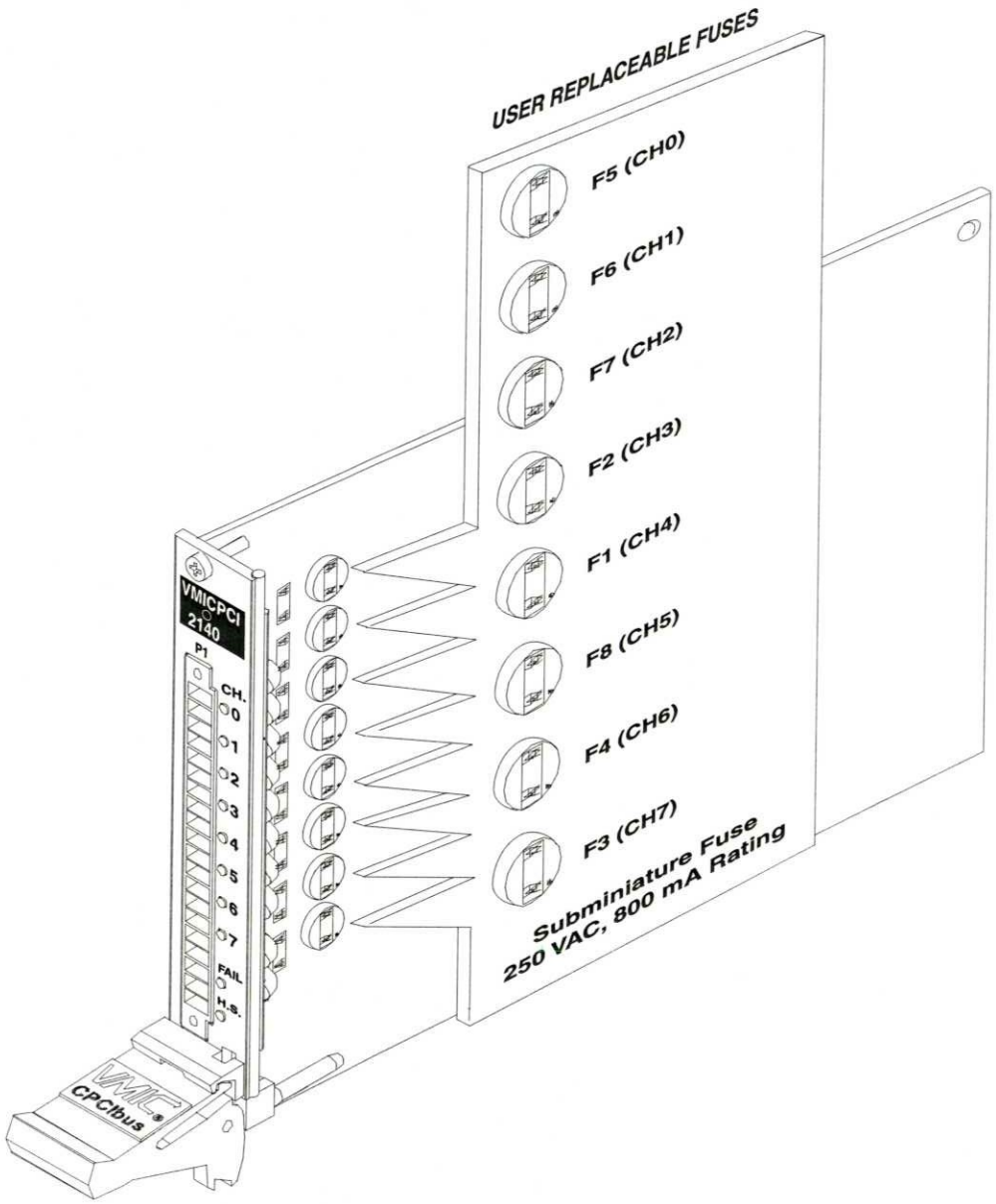


Figure 2-1 Location of User Replaceable Fuses

NOTE: Replacement fuses can be obtained from VMIC (part number 343-000015-080) or from Wickmann (Vendor part number 370-0800041).

Front Panel LED

The VMICPCI-2140 has ten LEDs on the front panel: Eight corresponding to a particular channel (one per channel), one Fail LED, and the Hot Swap LED. Figure 2-2 is an illustration of the front panel

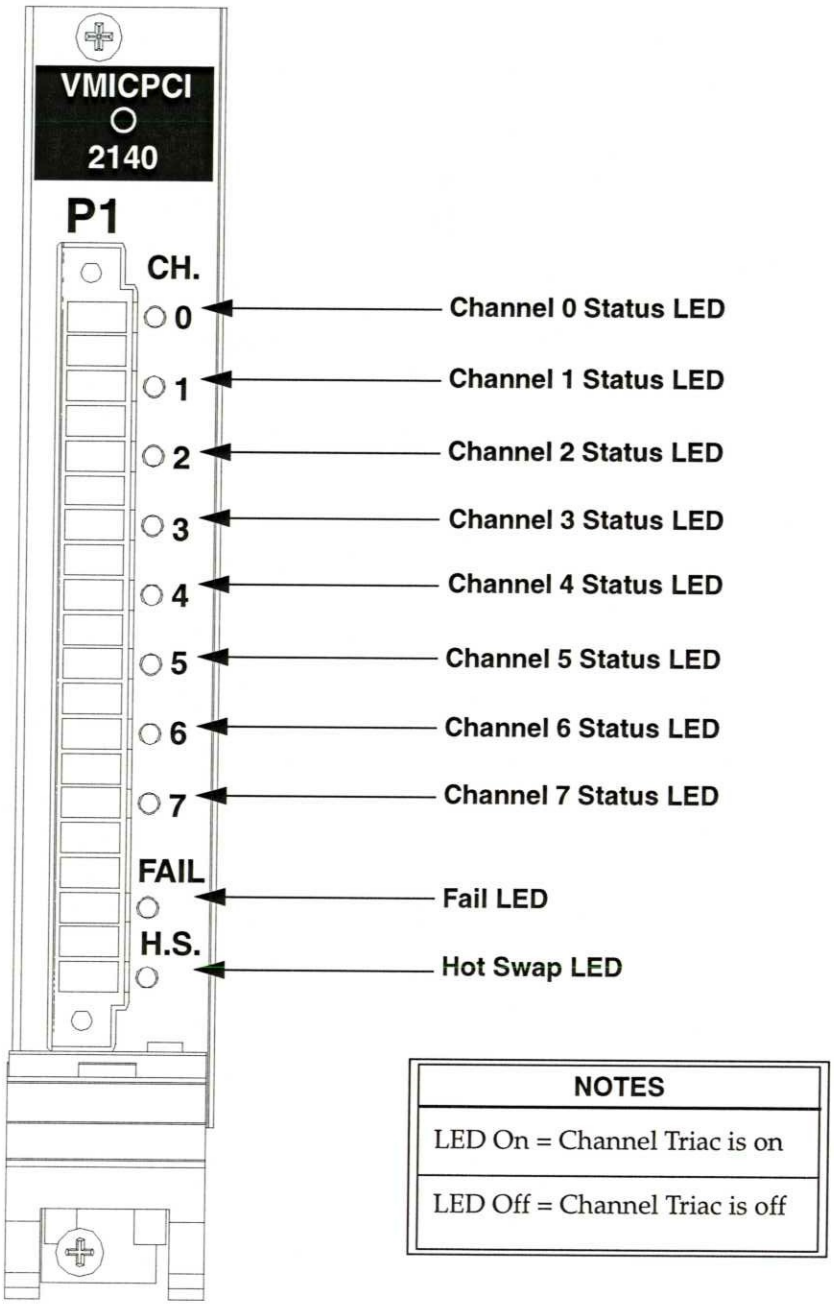


Figure 2-2 VMICPCI-2140 Front Panel

Connector Configuration

P1 Connector and Pinout

The front panel input connector (P1) on the VMICPCI-2140 board is a Mini-Combicon header. Figure 2-3 shows the pin layout of the P1 connector. Table 2-2 details the connector pin assignments.

Table 2-2 P1 Pin Assignments

Pin No.	Signal Description
1	Channel 0 Side A
2	Channel 0 Side B
3	Channel 1 Side A
4	Channel 1 Side B
5	Channel 2 Side A
6	Channel 2 Side B
7	Channel 3 Side A
8	Channel 3 Side B
9	Channel 4 Side A
10	Channel 4 Side B
11	Channel 5 Side A
12	Channel 5 Side B
13	Channel 6 Side A
14	Channel 6 Side B
15	Channel 7 Side A
16	Channel 7 Side B
17	Not Used
18	Not Used
19	Not Used
20	Not Used

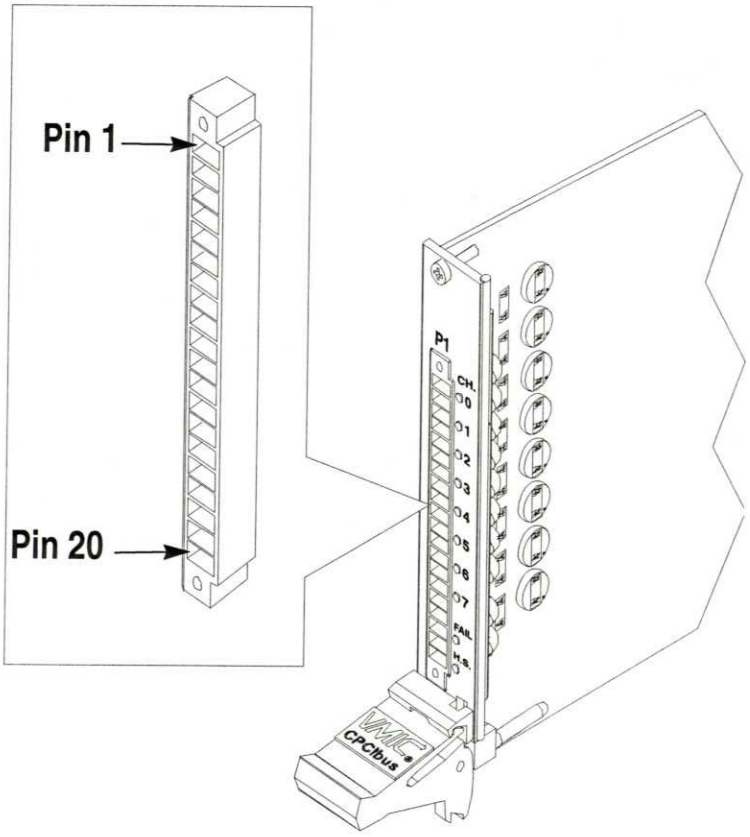


Figure 2-3 P1 Connector

P1 Mating Connector

The mating connector is a Mini-Combicon 20 position mating screw terminal plug. VMIC recommends using a high quality wire that meets or exceeds the following:

Connection Capacity (Wire)

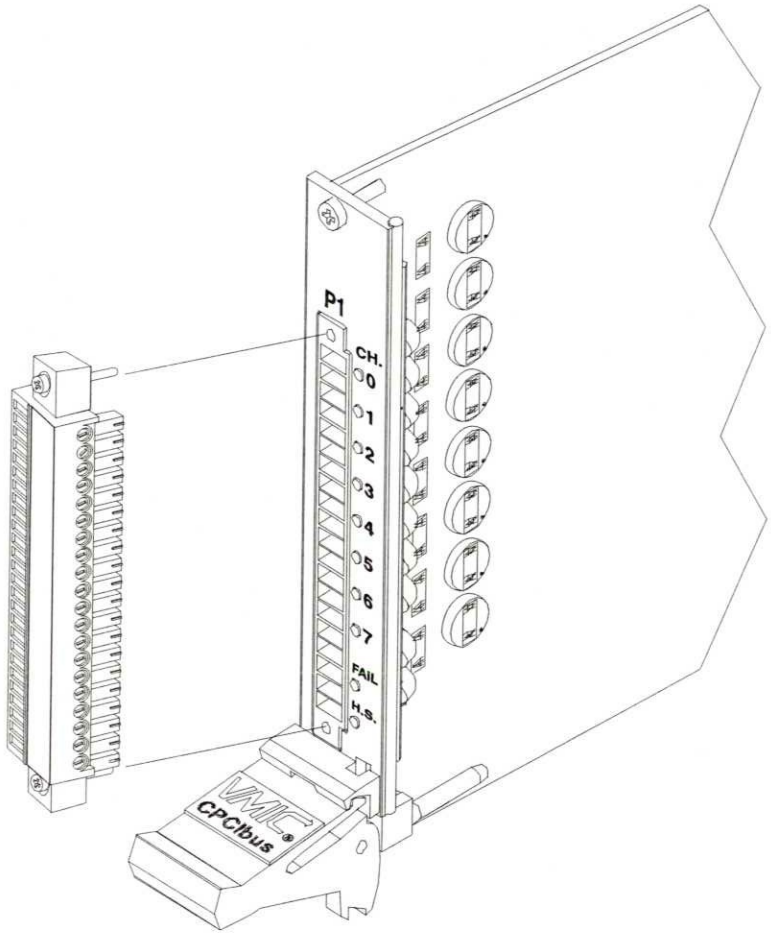
Solid or Stranded wire 28 to 16 AWG (0.14 to 1.5 mm)

Stripping Length - 7 to 9 mm

Internal Cylindrical Gage (IEC 947-1:1988) - A1

Mating Connector Screw Thread - M2

Mating Connector Screw Torque - 0.22 to 0.25 Nm



NOTE: Each VMICPCI-2140 is supplied with one mating screw terminal plug. Additional mating screw terminal plugs can be obtained from VMIC or Phoenix Contact. Phoenix Contact P/N 1847301 or VMIC P/N 321-000340-020.

Figure 2-4 VMICPCI-2140 with the Female Mini-Combicon 20-Position Header with Screw Terminals

CompactPCI Connector J1

The J1 connector on the VMICPCI-2140 is a 2 mm DIN 32-bit, 5 V, CompactPCI bus connector. The metal shell (row F) of the J1 connector is connected to chassis ground. See the figure and table below for the J1 connector and pinout.

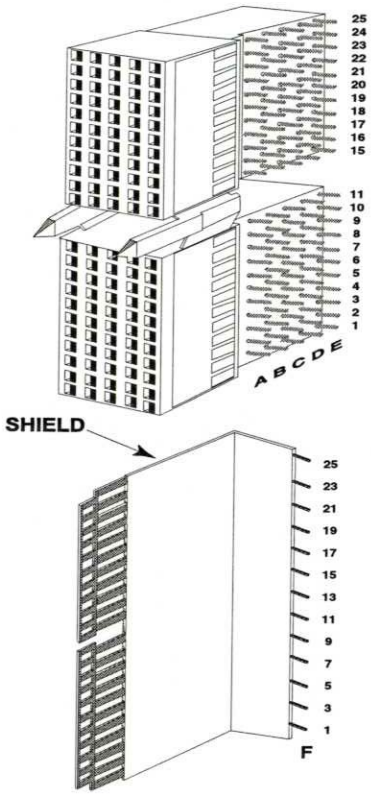


Figure 2-5 J1 Connector

Table 2-3 J1 Connector Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
25	+5 V	N/C	ENUM#	N/C	+5 V	GND
24	IN_AD[1]	+5 V	+5 V	IN_AD[0]	N/C	N/C
23	3.3 V	IN_AD[4]	IN_AD[3]	+5 V	IN_AD[2]	GND
22	IN_AD[7]	GND	N/C	IN_AD[6]	IN_AD[5]	N/C
21	3.3 V	IN_AD[9]	IN_AD[8]	GND	INC/BE[0]	GND
20	IN_AD[12]	GND	N/C	IN_AD[11]	IN_AD[10]	N/C
19	3.3 V	IN_AD[15]	IN_AD[14]	GND	IN_AD[13]	GND
18	INSERR	GND	N/C	INPAR	INC/BE[1]	N/C
17	3.3 V	N/C	N/C	GND	INPERR	GND
16	IN_DEVSEL	GND	+5 V	INSTOP#	INLOCK	N/C
15	N/C	IN_FRAME	INIRDY	GND	INTRDY	GND
12 through 14 are lost to the keying area						
11	IN_AD[18]	IN_AD[17]	IN_AD[16]	GND	INC/BE[2]	GND
10	IN_AD[21]	GND	N/C	IN_AD[20]	IN_AD[19]	N/C
9	INC/BE[3]	INIDSEL	IN_AD[23]	GND	IN_AD[22]	GND
8	IN_AD[26]	GND	+5 V	IN_AD[25]	IN_AD[24]	N/C
7	IN_AD[30]	IN_AD[29]	IN_AD[28]	GND	IN_AD[27]	GND
6	N/C	GND	N/C	CLK	IN_AD[31]	N/C
5	N/C	N/C	INRST	GND	N/C	GND
4	N/C	GND	+5 V	N/C	N/C	N/C
3	N/C	N/C	N/C	+5 V	N/C	GND
2	N/C	+5 V	N/C	N/C	N/C	N/C
1	+5 V	N/C	N/C	N/C	+5 V	GND

CHAPTER 3

Programming

Contents

Introduction

The VMICPCI-2140 board requires very little software. After performing any initialization, the user can perform write operations to the appropriate output register to modify the state of the field.

Where appropriate, information on programming these registers is provided. All values are in hexadecimal unless otherwise indicated.

VMICPCI-2140 Register Sets

To operate the VMICPCI-2140 board, the user must recognize that there are two separate registers sets, the PCI Configuration registers and the VMICPCI-2140 Channel Status registers. The method of accessing the registers differs for the two groups and each of the two groups has a separate memory map.

The CompactPCI Specification has additional register sets, the Local Configuration and the Runtime registers. In the case of the VMICPCI-2140 board these registers are not implemented and therefore are RESERVED and SHOULD NOT be altered.

PCI Configuration registers - This group of registers is defined by the PCI Specification and is similar for all PCI boards from any vendor. PCI Configuration registers can only be accessed through the PCI bus with Configuration Type 0 cycles. Configuration Type 0 cycles require special software code and are not the same as the standard memory or I/O read/write code. The Configuration registers are preloaded during power up from an on-board serial PROM and then modified by the system BIOS during initialization. Many of the Configuration registers are read-only and are rarely, if ever, modified by user programs. The one exception may be the Hotswap Control and Status registers.

There are two registers within the Configuration register that have a significant influence on the remaining registers:

- Base Address Register 0 (PCIBAR0)
- Base Address Register 2 (PCIBAR2)

Base Address Register 0 contains the starting address for memory mapped access to the Local Configuration. Base Address Register 2 contains the starting address for memory mapped access of the VMICPCI-2140 Channel Status register. The values in the two Base Address registers are assigned by the system BIOS and will vary from system to system. User programs must have the capability to read these two registers.

VMICPCI-2140 Channel Status registers - Unlike the previous groups of registers, the VMICPCI-2140 Channel Status registers do not reside in the PLX 9054 device. Instead, they reside in a CPLD device that interfaces to the PLX 9054 through the Local bus. For the PLX 9054 the Local bus is configured in one of three ways:

1. M mode
2. C mode
3. J mode

The VMICPCI-2140 operates in the C mode. The Channel Status registers implement the features unique to the VMICPCI-2140 operation. It is this group of registers that the user routines access to operate the board. Unlike the previous register groups, the Channel Status registers are not preloaded to specific values through an serial PROM. Instead, the registers within the CPLD are hardwired to assume default states when any event causes a reset to the CPLD.

Local Configuration registers (Not Applicable) - This group of registers is located within the PLX 9054 interface device and define the basic mode(s) of operation for the particular board on which the device resides. Like the PCI Configuration registers, the Local Configuration registers are preloaded during power up by an on-board serial PROM. The Local Configuration registers are rarely changed from their initial values.

The PLX 9054 is a universal PCI interface, which supports many modes of operation and requires a large number of Local Configuration registers to support those modes. The VMICPCI-2140 is a direct slave (PCI Target) only board. Therefore, many of the Local Configuration registers are not applicable to the VMICPCI-2140 board and should not be altered.

Runtime registers (Not Applicable) - These registers are a subset of the Local Configuration registers. The Runtime registers differ from the other Local Configuration registers in that their contents are subject to frequent changes during operation of the device. A large portion of the Runtime registers is not applicable to VMICPCI-2140 operation and should not be altered.

Configuration Space Organization

This section defines the organization of Configuration Space registers and imposes a specific record structure or template on the 256-byte space. This space is divided into a predefined header region and a device-dependent region. Devices implement only the necessary and relevant registers in each region. A device's configuration space must be accessible at all times, not just during system boot. The predefined header region has a size of 64 bytes and every device must support the register layout of this region. This region consists of fields that uniquely identify the device and allow the device to be generically controlled. See Table 3-1 below.

Table 3-1 PCI Configuration Registers

PCI Configuration Register Address	To ensure compatibility with other versions of the PLX 9054 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 24 23 16 15 8 7 0	PCI Writable	Serial EEPROM Writable
$00	**Device ID** / **Vendor ID**	N	Y
$04	**Status** / **Command**	Y	N
$08	**Class Code** / **Revision ID**	N	Y
$0C	**BIST** / **Header Type** / **PCI Bus Latency Timer** / **Cache Line Size**	Y	N
$10	**PCI Base Address 0: used for Memory-Mapped Configuration Registers (PCIBAR0)**	Y	N
$14	PCI Base Address 1: used for I/O-Mapped Configuration Registers (PCIBAR1)	Y	N
$18	**PCI Base Address 2: used for Local Address Space 0 (PCIBAR2)**	Y	N
$1C	PCI Base Address 3: used for Local Address Space 1 (PCIBAR3)	Y	N
$20	Unused Base Address (PCIBAR4)	N	N
$24	Unused Base Address (PCIBAR5)	N	N
$28	Cardbus CIS Pointer (Not Supported)	N	N
$2C	Subsystem ID / Subsystem Vendor ID	N	Y
$30	PCI Base Address for Local Expansion ROM	Y	N
$34	Reserved / New Capability Pointer	N	N
$38	Reserved	N	N
$3C	Max_Lat / Min_Gnt / Interrupt Pin / Interrupt Line	Y [7:0]	Y
$40	Power Management Capabilities / Next_Cap Pointer / Capability ID	Y	N
$44	Data / PMCSR Bridge Support Extensions / Power Management Control/Status Register	Y	N
$48	**Reserved** / **Control/Status Register** / **Next_Cap Pointer** / **Capability ID**	PCI [23:16]	Y [15:0]
$4C	F / VPD Address / Next_Cap Pointer / Capability ID	PCI [31:16]	N
$50	VPD Data	Y	N

NOTE: Refer to *PCI Specification v2.2* for definitions of these registers. Registers that are highlighted with bold face type are used by the VMICPCI-2140 board. Registers that are not highlighted are reserved and should not be changed.

Configuration Space Functions

PCI has the potential for greatly increasing the ease with which systems may be configured. To realize this potential, all PCI devices must provide certain functions that system configuration software can utilize. This section also lists the functions that need to be supported by PCI devices by way of registers defined in the predefined header portion of the configuration space. The exact format of these registers (that is, number of bits implemented) is device-specific. However, some general rules must be followed. All registers must be capable of being read back, and the data returned must indicate the value that the device is actually using.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions. Its use should be restricted to initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers.

Device Identification

There are five fields in the predefined header that pertain to the device identification. All PCI bus devices are required to implement these fields. Generic configuration software will be able to determine what devices are available on the system's PCI bus(es). All of these registers are read-only.

Vendor ID This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. $114A is VMIC's vendor ID.

Device ID This field identifies the particular device. This identifier is allocated by the vendor. The Device ID for the VMICPCI-2140 is $2140.

Revision ID This register specifies a device-specific revision identifier. The value is chosen by the vendor. $01 is the default.

Header Type This byte identifies the layout of location $10 through $3F in configuration space and whether or not the device contains multiple functions. Bit 7 in this register is used to identify a multifunction device. If the bit is 0, then the device has multiple functions. Bits 6 through 0 specify the layout of locations $10 through $3F. One encoding, $00, is defined and specifies the layout shown in Table 3-1 on page 36. All other encoding are reserved.

Class Code The Class Code Register is used to identify the generic function of the device. The register is broken into three byte-size fields. The upper byte (at offset $0B) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset $0A) is a subclass code which identifies more specifically the function of the device. The lower byte (at offset $09) identifies a specific register-level programming interface (if any) so that device-independent software can interact with the device. The VMICPCI-2140 Class Code value is $1180.

Hot Swap Control and Status Register (HS_CSR)

The VMICPCI-2140 incorporates the PLX 9054, which supports Hot Swap directly. A Control and Status Register is provided in Configuration Space. The Hot Swap Control and Status Register (HS_CSR) provides status read-back for the Hot-Plug system driver to determine which board is driving ENUM#. This register is also used to control the Hot Swap Blue Status LED on the front panel and to de-assert ENUM#.

Table 3-2 Hot Swap Control and Status Register Bit Map

Hot Swap Control and Status Register (HS_CSR): PCI Configuration Register ($48), Read/Write			
Bits 31 Through 24	**Bits 23 Through 16**	**Bits 15 Through 8**	**Bits 7 Through 0**
Reserved	Control	Next_Cap Pointer	Hot Swap ID

Hot Swap Control and Status Register Bit Definitions

Bits 31 through 24: **Reserved** - These bits are currently reserved and should not be used. Write to zero.

Bits 23 through 16: **Control. Bits [23:16]** - This eight-bit control register is defined as follows.

Bit	Bit Description
23	ENUM# Status – Insertion (1 = board is inserted)
22	ENUM# Status – Removal (1 = board is being removed)
21	Not used
20	Not used
19	LED state (1 = LED on, 0 = LED off)
18	Not used
17	ENUM# interrupt enable (1 = de-assert, 0 = enable interrupt)
16	Not used

Bits 15 through 8: **Next_Cap Pointer. Bits [15:8]** - These bits either point to the next new capability structure, or are set to zero (0) if this is the last capability in the structure.

Bits 7 through 0: **Hot-Swap ID – Bits [7:0]** - These bits are set to a default value of $06.

Board ID Register (BID)

This is a read-only register that can assist in determining if the board is functioning properly. This register always reads $2140 after a system reset.

Table 3-3 Board ID Register Bit Map

Board ID Register (BID): Relative Offset $04, Read-Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
0	0	1	0	0	0	0	1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	1	0	0	0	0	0	0

FAIL LED Register

This register controls the Fail LED. Writing a one (1) to this bit turns the Fail LED ON. At power up or reset, this bit is set high causing the LED to be ON.

Table 3-4 Fail LED Register Bit Map

Fail LED Register (Fail_LED): Relative Offset $10, Read/Write, Byte							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
0	0	1	0	0	0	0	1

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R/W	Reserved						

Fail LED Register Bit Definitions

Bits 15 through 8: These upper eight bits reflect the Board ID's upper bits.

Bit 7: **Fail LED Control Bit:**

1 = LED ON
0 = LED OFF

Bits 6 through 0: **Reserved** - These bits are currently reserved and should not be used. Write to zero.

Channel Status Registers

Table 3-5 lists the channels and their associated register bit locations. Bit 7 of the Channel Status Register controls the output circuitry for that channel.

Table 3-5 Channel Status Register 0 Bit Map

Channel Status Register 0 (CCR0): Relative Offset $40, Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
0	0	1	0	0	0	0	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH00	Reserved 0						

Channel Status Register 0 Bit Definitions

Bits 15 through 8: These upper eight bits reflect the Board ID's upper bits.

Bit 7: **Channel 00 Output Control Bit** - If bit 7 of this register is set to a one (1), the output circuitry for Channel 00 is active.

Bits 6 through 0: **Reserved** - These bits are currently reserved and should not be used. These bits will always show zero (0).

Channels 1 through 7 are identical to channel 0 and follow the same format as channel 0.

Channel 0 Write Example

1. Obtain the VMICPCI-2140 Base Address from the PCI Configuration register at address $18.
2. Add a relative offset of $40 to the Base Address obtain in step 1.
3. Write $80 to Channel Control Register 0 (CCR0) address obtain in step 2.

Channel 0 (Triac) should now be active and Channel 0 Status LED should also be ON.

Table 3-6 VMICPCI-2140 Memory Space Map

Register	PCI Offset Address	Description	Mnemonic	Value at Reset
Board ID	$04	Board ID	BID	$2140
Fail LED	$10 (Bit 7)	Fail LED	Fail_LED	$2180
Channel 0	$40 (Bit 7)	Channel Control 0	CCR0	$2100
Channel 1	$44 (Bit 7)	Channel Control 1	CCR1	$2100
Channel 2	$48 (Bit 7)	Channel Control 2	CCR2	$2100
Channel 3	$4C (Bit 7)	Channel Control 3	CCR3	$2100
Channel 4	$50 (Bit 7)	Channel Control 4	CCR4	$2100
Channel 5	$54 (Bit 7)	Channel Control 5	CCR5	$2100
Channel 6	$58 (Bit 7)	Channel Control 6	CCR6	$2100
Channel 7	$5C (Bit 7)	Channel Control 7	CCR7	$2100
---	$60 through $FF	Reserved	---	---

PCI Configuration Registers

All registers may be written to or read from using Byte, Word, or Lword accesses.

PCI Configuration ID Register (PCIIDR; PCI:$00)

Table 3-7 PCI Configuration ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX ($10B5) if blank or if no serial EEPROM is present.	Yes	No	$114A
31:16	Device ID. Identifies particular device. Defaults to PLX part number for PCI interface chip ($9054) if blank or no serial EEPROM is present.	Yes	No	$2140

PCI Command Register (PCICR; PCI:$04)

Table 3-8 PCI Command Register

Bit	Description	Read	Write	Value after Reset
0	I/O Space. Writing a 1 allows the device to respond to I/O space accesses. Writing a 0 disables the device from responding to I/O space accesses.	Yes	Reserved	1
1	Memory Space. Writing a 1 allows the device to respond to Memory Space accesses. Writing a 0 disables the device from responding to Memory Space accesses.	Yes	Reserved	1
2	Master Enable. Writing a 1 allows a device to behave as a Bus Master. Writing a 0 disables the device from generating Bus Master accesses.	Yes	Reserved	0
3	Special Cycle. **Not Supported.**	Yes	No	0
4	Memory Write and Invalidate Enable. Writing a 1 enables Memory Write and Invalidate mode for Direct Master and DMA. (Refer to the DMA Mode register(s), DMAMODE0[13] and/or DMAMODE1[13].)	Yes	Reserved	1
5	VGA Palette Snoop. **Not Supported.**	Yes	No	0
6	Parity Error Response. Writing a 0 indicates parity error is ignored and the operation continues. Writing a 1 indicates parity checking is enabled.	Yes	Reserved	0
7	Wait Cycle Control. Controls whether a device does address/data stepping. Writing a 0 indicates the device never does stepping. Writing a 1 indicates the device always does stepping. (Hardcoded to 0.)	Yes	No	0
8	SERR# Enable. Writing a 1 enables SERR# driver. Writing a 0 disables SERR# driver.	Yes	Reserved	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. Writing a 1 indicates fast back-to-back transfers can occur to any agent on the bus. Writing a 0 indicates fast back-to-back transfers can only occur to the same agent as in the previous cycle. (Hardcoded to 0.)	Yes	No	0
15:10	Reserved	Yes	No	$0

PCI Status Register (PCISR; PCI:$06)

Table 3-9 PCI Status Register

Bit	Description	Read	Write	Value after Reset
3:0	Reserved	Yes	No	$0
4	New Capability Functions Support. Writing a 1 supports new capabilities functions. If enabled, the first new capability function ID is located at PCI Configuration offset [$40]. Can only be written from the local bus. Read-only from the PCI bus.	Yes	No	0
5	Reserved	Yes	Yes	0
6	If set to 1, this device supports User Definable Functions. Can only be written from the Local bus. Read-only from the PCI bus.	Yes	No	0
7	Fast Back-to-Back Capable. Writing a 1 indicates an adapter can accept fast back-to-back transactions. **NOTE**: Hardcoded to 1.	Yes	No	1
8	Master Data Parity Error Detected. Set to 1 when three conditions are met: 1) PLX 9054 asserted PERR# or acknowledged PERR# asserted; 2) PLX 9054 was bus master for operation in which error occurred; 3) Parity Error Response bit is set (PCICR[6]=1). Writing a 1 clears this bit to 0.	Yes	Reserved	0
10:9	DEVSEL# Timing. Indicates timing for DEVSEL# assertion. Writing a 01 sets this bit to medium. **NOTE**: Hardcoded to 1.	Yes	No	01
11	Target Abort. When set to 1, indicates the PLX 9054 has signaled a Target Abort. Writing a 1 clears this bit to 0.	Yes	Reserved	0
12	Received Target Abort. When set to 1, indicates the PLX 9054 has received a Target Abort signal. Writing a 1 clears this bit to 0.	Yes	Reserved	0
13	Received Master Abort. When set to 1, indicates the PLX 9054 has received a Master Abort signal. Writing a 1 clears this bit to 0.	Yes	Reserved	0
14	Signal System Error. When set to 1, indicates the PLX 9054 has reported a system error on SERR#. Writing a 1 clears this bit to 0.	Yes	Reserved	0
15	Detected Parity Error. When set to 1, indicates the PLX 9054 has detected a PCI bus parity error, even if parity error handling is disabled (the parity Error Response bit in the Command register is clear). One of these conditions can cause this bit to be set: 1) PLX 9054 detected parity error during PCI Address phase; 2) PLX 9054 detected data parity error when it was the Target of a write; 3) PLX 9054 detected data parity error when performing Master Read operation. Writing a 1 clears this bit to 0.	Yes	Reserved	0

PCI Revision ID Register (PCIREV; PCI$08, LOC: $08)

Table 3-10 PCI Revision ID Register

Bit	Description	Read	Write	Value after Reset
7:0	Revision ID. Silicon revision of the PLX 9054.	Yes	No	Current Rev

PCI Class Code Register (PCICCR; PCI:$09-$0B)

Table 3-11 PCI Class Code Register

Bit	Description	Read	Write	Value after Reset
7:0	Register Level Programming Interface. None defined.	Yes	No	$00
15:8	Subclass Code. Other data acquisition/signal processing controller (Per Revision 2.2 of PCI specification.)	Yes	No	$80
23:16	Base Class Code. Data acquisition and signal processing controller (Per Revision 2.2 of PCI specification.)		No	$11

PCI Header Type Register (PCIHTR; PCI:$0E)

Table 3-12 PCI Header Type Register

Bit	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies layout of bits $10 through $3F in configuration space. Only one encoding, $0, is defined. All other encoding are reserved.	Yes	No	$0
7	Header Type. Writing a 1 indicates multiple functions. Writing a 0 indicates single function.	Yes	No	$0

PCI Base Address Register for Memory Accesses to Local and Runtime Registers (PCIBAR0; PCI:$10)

Table 3-13 PCI Base Address Register for Memory Accesses to Local and Runtime Registers

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. Hardcoded to 0.	Yes	No	$0
2:1	Location of Register. Values: 00-Locate anywhere in 32-bit Memory Address space 01-locate below 1 Mbyte Memory Address space 10-Locate anywhere in 64-bit Memory Address space 11-Reserved Hardcoded to 00	Yes	No	00

Table 3-13 PCI Base Address Register for Memory Accesses to Local and Runtime Registers (Continued)

Bit	Description	Read	Write	Value after Reset
3	Prefetchable. Writing a 1 indicates there are no side effects on reads. Does not affect operation of the PLX 9054.	Yes	No	$0
7:4	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers (requires 256 bytes). Hardcoded to $0	Yes	No	XX See Note
31:8	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers.	Yes	Yes	XX See Note

NOTE: Assigned by system BIOS during initialization.

PCI Base Address Register for Memory Accesses to Local Address Space 0 (PCIBAR2; PCI:$18)

Table 3-14 PCI Base Address Register for Memory Accesses to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. Specified in the LAS0RR register..	Yes	No	0
2:1	Location of Register (If memory Space). Values: 00 - Locate anywhere in 32-bit Memory Address space 01 - Locate below 1 Mbyte Memory Address space 10 - Locate anywhere in 64-bit Memory Address space 11 - Reserved (Specified in the LAS0RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 No bit 2 Yes	00
3	Prefetchable (If Memory Space). Writing a 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect operation of the PLX 9054. Prefetching functions of this address space are controlled by the associated Bus Region Description register. (Specified in LAS0RR register.) If I/O Space, bit 3 is included in the base address.	Yes	No	$0
31:4	Memory Base Address. Memory base address for access to Local Address Space 0. PCIBAR2 can be enabled or disabled by setting or clearing the Space 0 Enable bit (LAS0BA[0]).	Yes	Yes	X See Note

NOTE: Assigned by system BIOS during initialization.

Hot Swap Control Register (HS_CNTL; PCI:$48)

Table 3-15 Hot Swap Control Register

Bit	Description	Read	Write	Value after Reset
7:0	Hot Swap ID	Yes	No	$06

Hot Swap Next Capability Pointer Register (HS_NEXT; PCI:$49)

Table 3-16 Hot Swap Next Capability Pointer Register

Bit	Description	Read	Write	Value after Reset
7:0	Next_Cap Pointer. Points to the location of the next item in the capabilities linked list. If Hot Swap is the last item in the list, then this register should be set to zero	Yes	No	$4C

Hot Swap Control/Status Register (HS_CSR; PCI:$4A)

Table 3-17 Hot Swap Control/Status Registers

Bit	Description	Read	Write	Value after Reset
0	Reserved	Yes	No	0
1	ENUM# Interrupt Clear. Writing a 0 enables the interrupt. Writing a 1 clears the interrupt.	Yes	PCI Yes/Clr	0
2	Reserved	Yes	No	0
3	LED Software On/Off Switch. Writing a 1 turns on the LED. Writing a 0 turns off the LED	Yes	PCI	0
4	Reserved	Yes	No	0
5	Reserved	Yes	No	0
6	ENUM# Status Indicator for Board Removal. Writing a 1 reports the ENUM# assertion for removal process	Yes	PCI Only	0
7	ENUM# Status Indicator for Board Insertion. Writing a 1 reports the ENUM# assertion for insertion process.	Yes	PCI Only	0
15:8	Reserved	Yes	No	$0

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

VMIC's Customer Service can be reached by any of the following:

Direct: 256-650-8398

Toll-Free Direct: 800-240-SRVC (7782)

FAX: 256-650-7245

Email: customer.service@vmic.com

Maintenance Prints

The fuses on the VMICPCI-2140 are user replaceable, all other user-level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.