VMICPCI-2335 CompactPCI 16-Channel Optically Coupled Digital Output board

Product Manual

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500-652335-000 Rev.B

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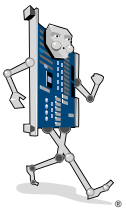

(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

VMIC

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Overview

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Introduction

The VMICPCI-2335 CompactPCI 16-Channel Optically Coupled Digital Output board is designed to provide isolation between the field and the CompactPCI chassis. There are 16 optically coupled outputs. The outputs provide a sustained 1.5 kV of system isolation to the CompactPCI backplane.

The VMICPCI-2335 board has several features as specified below.

- 16 optically coupled voltage sourcing or current sinking outputs
- Pull-up resistors for the voltage sourcing output
- External voltage may be applied on byte boundaries to supply power for Voltage Sourcing Mode
- On-board Built-in-Test Logic for fault detection and isolation
- Front panel with standard 37-pin female connector
- 8-, 16-, or 32-bit data transfers
- Output ranges to a maximum of 50 V per channel
- Output range to a maximum 300 mA per channel
- Fail LED
- 3U Eurocard, with optional 6U front panel
- Compliance with PCI specification Revision 2.1
- Compliance with CompactPCI specification Revision 2.1

Functional Description

The output circuitry of the VMICPCI-2335 board has two configurations: **Voltage Sourcing** or **Current Sinking**. For the Voltage Sourcing Option, pull-up resistors are installed on the optically coupled, open-collector outputs. The user supplies voltage to the **VEXT** pins on the interface connector, P1. The Current Sinking Option has no pull-up resistors installed. These output functions may be selected on byte boundaries.

This board supports Built-in-Test (BIT) of most of the active components. This allows the host to write data to a register, read it back, and compare the two to determine the health of the board. After the integrity of the board has been determined, the board may be changed from off-line to on-line mode.

A Control and Status Register (CSR) is used to control and monitor the state of the board. This register allows independent control of the on-line / off-line state of the outputs and provides control for the Fail LED. The purpose of the Fail LED is for status indication under user software control. The default reset condition of the Fail LED is ON. This does not indicate a failure of the board because the board does not contain any self-test capabilities.

Physical Description and Specifications

Refer to VMIC product specification description **No. 800-652335-000**.

Reference Material List

For a detailed explanation of the PCI local bus and its characteristics, refer to the *PCI Local Bus Specification* from:

PCI Local Bus Specification, Revision 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)

For a detailed explanation of the CompactPCI bus and its characteristics, refer to the *CompactPCI Specification, 2.0 R2.1* from:

PCI Industrial Manufacturers Group
(PICMG)
301 Edgewater Place
Suite 220
Wakefield, MA 01880 USA
(617) 224-1100
(503) 797-4207 (International)
Fax: (617) 224-1239
Web: www.PICMG.ORG

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

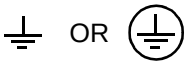
Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

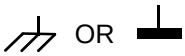
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



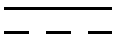
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

The STOP symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER
1

Theory of Operation

Contents

Introduction

The following sections are designed to describe the functionality of the VMICPCI-2335 board. This discussion includes the VMICPCI-2335's role in the system hardware architecture as well as important individual registers located on the board itself.

Operational Overview

The VMICPCI-2335 board is designed to provide isolation between the 16 digital output channels. The output voltage level is determined by the system hardware to which it is connected.

The VMICPCI-2335 board's address is assigned by the system BIOS during system powerup per the PCI specification. By executing a write cycle to the data registers, data is steered from the backplane to the Output Data Register (ODR). The data stored in this register is used to drive the open-collector output to the field.

The VMICPCI-2335 board has Built-in-Test (BIT) registers. They are used to check the health of the board. In order to prevent interaction with the field during BIT, the host first takes the board off-line to isolate the outputs, then simply writes data to the register to be checked. Then, by reading the register and comparing the data read to the data written, the user can determine if the board is functioning correctly. In order to maintain isolation between the field and the PCI bus, the Built-in-Test can only verify the circuitry associated with the PCI bus side of the board. Figure 1-1 is a block diagram of the basic functions of the VMICPCI-2335 board. These blocks will be discussed in more detail in the following sections.

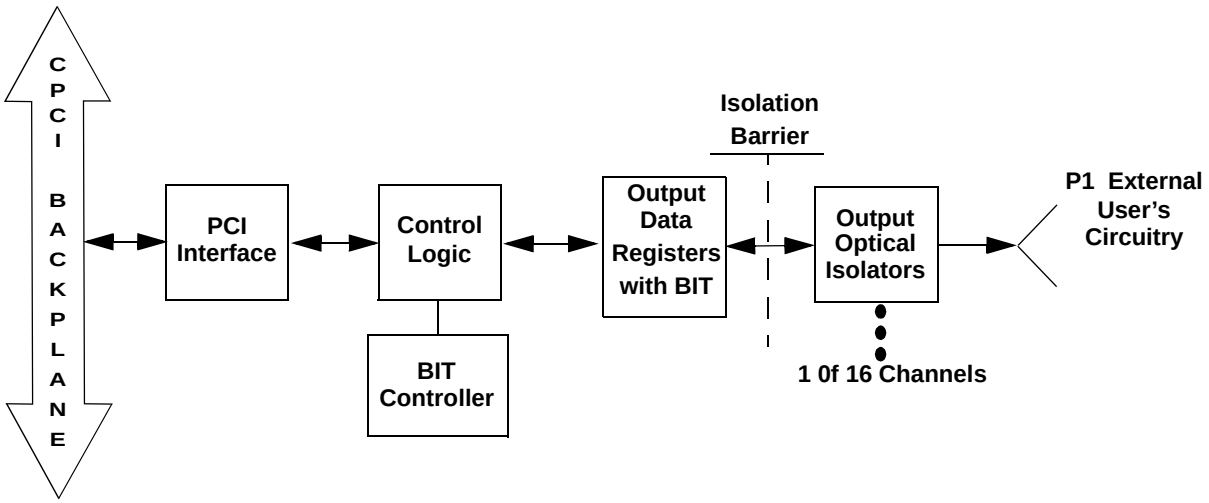


Figure 1-1 VMICPCI-2335 Board's Functional Block Diagram

PCI Compatibility

The VMICPCI-2335 board is a PCI Specification 2.1-compliant add-on slave card. The board occupies 64 byte of contiguous I/O space and can be mapped into any PCI I/O space. The board does not utilize interrupts or DMA access and the hardware does not require a "wait state."

Data Polarity

The VMICPCI-2335 board has positive true output data polarity. On the PCI bus, when a one is written to an output, the open-collector output transistor will be active (turned on).

HIGH IN = LOW OUT in voltage sourcing mode.

HIGH IN = current on in current sinking mode.

Output Data Registers

The Output Data Registers may be read back to check for proper functioning of the VMICPCI-2335 board. This allows the user to simply write to and then read from the port to be checked. Data stored in the Output Data Register can be read back to the PCI bus.

Output Circuitry

Figure 1-2 shows the basic topology of each output. The information stored in the Output Data Register from a PCI bus write is gated to the LED of the optocoupler. The output of the optocoupler biases the output transistors ON or OFF.

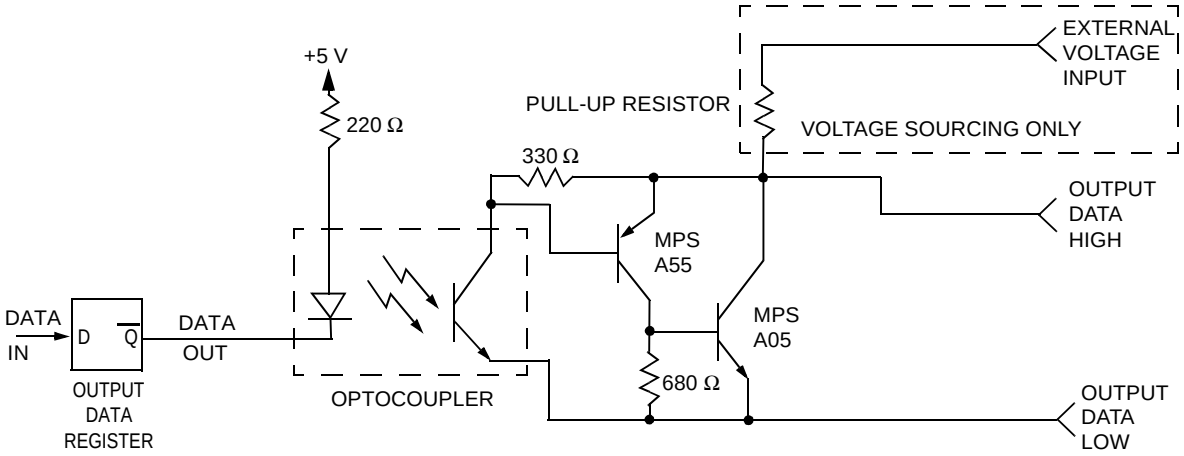


Figure 1-2 Typical Output Configuration

Output Types

The open-collector outputs can be configured for one of two types, either voltage sourcing or current sinking. Current sinking outputs do not have pull-up resistors installed. Pull-up resistors are present if the outputs are configured for voltage sourcing. These pull-up resistors may be supplied by an external voltage supplied by the user. There are two such external voltage inputs, one for each byte. Output channels 0 through 7 may be pulled up with VEXT0 (pin 36). Output channels 8 through 15 may be pulled up with VEXT1 (pin 17).

Configuration Space

This portion of the theory of operation defines the programming model and usage rules for the configuration register space in PCI-compliant devices. The intent of the PCI configuration space definition is to provide an appropriate set of configuration *hooks* which satisfy the needs of current and anticipated system configuration mechanisms.

Configuration Space Organization

This section defines the organization of configuration space registers and imposes a specific record structure or template on the 256-byte space. This space is divided into a predefined header region and a device-dependent region. Devices implement only the necessary and relevant registers in each region. A device's configuration space must be accessible at all times, not just during system boot. The predefined header region has a size of 64 byte and every device must support the register layout of this region. This region consists of fields that uniquely identify the device and allow the device to be generically controlled. See Figure 1-3 below.

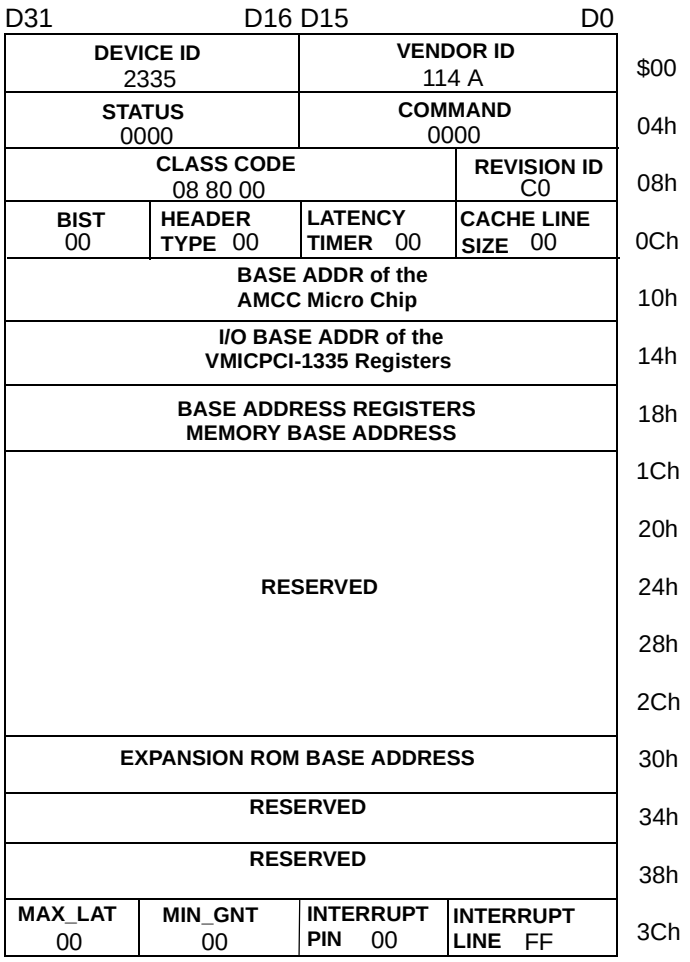


Figure 1-3 Configuration Space Header

All PCI-and CompactPCI-compliant devices must support the Vendor ID, Device ID, Command, and Status Fields in the header. Implementation of other registers is optional (that is, they can be treated as reserved registers) depending on device functionality. If a device supports the function that the register is concerned with, the device must implement it in the defined location and with the defined functionality.

Configuration Space Functions

PCI has the potential for greatly increasing the ease in which systems may be configured. To realize this potential, all PCI devices must provide certain functions that system configuration software can utilize. This section also lists the functions that need to be supported by PCI devices by way of registers defined in the predefined header portion of the configuration space. The exact format of these registers (that is, number of bits implemented) is device-specific. However, some general rules must be followed. All registers must be capable of being read back and the data returned must indicate the value that the device is actually using.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions. Its use should be restricted to initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers.

Device Identification

Five fields in the predefined header deal with device identification. All PCI bus devices are required to implement these fields. Generic configuration software will be able to easily determine what devices are available on the system's PCI bus(es). All of these registers are read-only.

Vendor ID This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. $114A is VMIC's vendor ID.

Device ID This field identifies the particular device. This identifier is allocated by the vendor. The Device ID for the VMICPCI-2335 is $2335.

Revision ID This register specifies a device-specific revision identifier. The value is chosen by the vendor. C0 is the default.

Header Type This byte identifies the layout of location $10 through $3F in configuration space and also whether or not the device contains multiple functions. Bit 7 in this register is used to identify a multifunction device. If the bit is 0, then the device has multiple functions. Bits 6 through 0 specify the layout of locations $10 through$3F. One encoding, $00, is defined and specifies the layout shown in Figure 1-3 on page 22. All other encodings are reserved.

Class Code The Class Code Register is used to identify the generic function of the device. The register is broken into three byte-size fields. The upper byte (at offset $0B) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset $0A) is a subclass code which identifies more specifically the function of the device. The lower byte (at offset $09) identifies a specific register-level programming interface (if any) so that device-independent software can interact with the device.

Device Control

The Command Register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command Register may or may not be implemented depending on a device's functionality. For instance, devices that do not implement an I/O space probably will not implement a writable element at bit location zero of the Command Register. Devices typically come up with all zeros in this register. Figure 1-4 shows the layout of the register and Table on page 25 explains the definitions of the different bits in the Command Register.

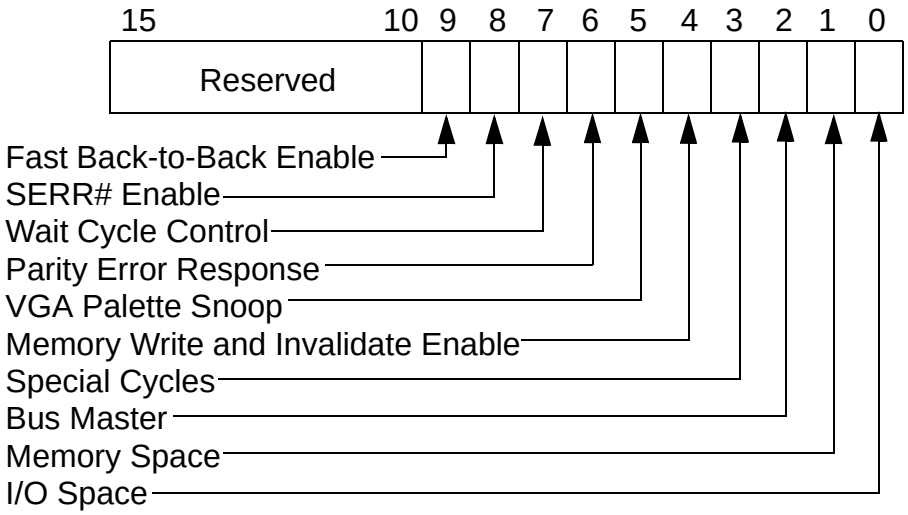


Figure 1-4 Command Register Layout

Table 1-1 Command Register Bits

Bit Location	Bit Definitions
0	Controls a device's response to I/O space accesses. A value of zero disables the device response. A value of one allows the device to respond to I/O space accesses. State after RST# is zero.
1	Controls a device's response to memory space accesses. A value of zero disables the device response. A value of one allows the device to respond to memory space accesses. State after RST# is zero.
2	Controls a device's ability to act as a master on the PCI bus. A value of zero disables the device from generating PCI accesses. A value of one allows the device to behave as a bus master. State after RST# is zero.
3	Controls a device's action on Special Cycle Operations. A value of zero causes the device to ignore all Special Cycle Operations. A value of one allows the device to monitor Special Cycle Operations. State after RST# is zero.
4	This is an enable bit for using the Memory Write and Invalidate Command. When this bit is one, masters may generate the command. When this bit is zero, Memory Write must be used instead. State after RST# is zero. This bit must be implemented by master devices that can generate the Memory Write and Invalidate Command.
5	This bit controls how VGA-compatible devices handle accesses to VGA palette registers. When this bit is one, special palette snooping behavior is enabled (that is, device must not respond). When the bit is zero, the device should treat palette accesses like all other accesses. VGA-compatible devices should implement this bit.
6	This bit controls the device's response to parity errors. When the bit is set (1), the device must take its normal action when a parity error is detected. When the bit is zero, the device must ignore any parity errors that it detects and continue normal operation. This bit's state after RST# is zero. Devices that check parity must implement this bit. Devices are still required to generate parity even if parity checking is disabled.
7	This bit is used to control whether or not a device does address/data stepping. Devices that never do stepping must have this bit hardwired to zero. Devices that always do stepping must have this bit hardwired to one. Devices that can do either should make this bit read/write and have it initialize to one after RST#.
8	This bit is an enable bit for the SERR# driver. A value of zero disables the SERR# driver. A value of one enables the SERR# driver. This bit's state after reset is zero. All devices that have an SERR# pin must implement this bit. This bit (and bit 6) must be ON to report address parity errors.
9	This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of one means the master is allowed to generate fast back-to-back transactions to different agents. A value of zero means fast back-to-back transactions are only allowed to the same agent.
10 through 15	Reserved

Device Status

The Status Register is used to record status information for PCI bus-related events. The definition of each of the bits is given in Table 1-2 on page 27, and the layout of the register is shown in Figure 1-5 below. Devices would not need to implement all bits, depending on device functionality. For instance, a device that acts as a target but will never signal target-abort, would not implement Bit 11.

Reads to this register behave normally. Writes are slightly different in that the bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear Bit 14 and not affect any other bits, write the value `0100_0000_0000_0000b` to the register.

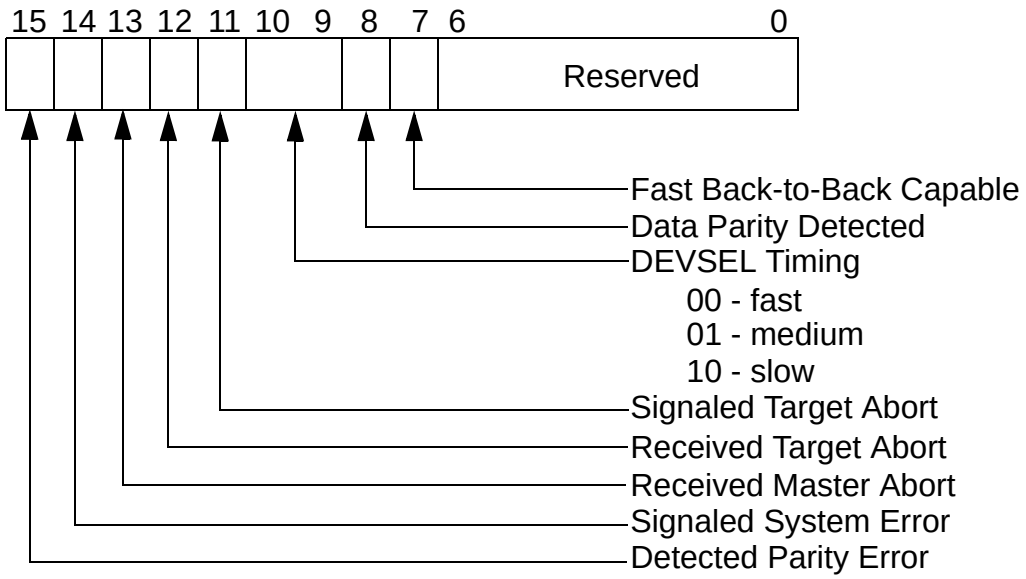


Figure 1-5 Status Register Layout

Table 1-2 Status Register Bits

Bit Location	Descriptions
0 through 6	Reserved
7	This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to one if the device can accept these transactions, and must be set to zero otherwise.
8	This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response Bit (Command Register) is set.
9 and 10	These bits encode the timing of DEVSEL#. The bits are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.
11	This bit must be set by a target device whenever the target terminates a transaction with a Target-Abort. All master devices must implement this bit.
12	This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
13	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
14	This bit must be set whenever the device asserts SERR#. Devices which will never assert SERR# do not need to implement this bit.
15	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled as controlled by Bit 6 in the Command Register.

Interrupt Line

The VMICPCI-2335 board does not utilize interrupts.

Base Addresses

One of the most important functions for enabling superior configurability and ease-of-use is the ability to relocate PCI devices in the address spaces. At system powerup, device-independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM. Each of these areas is covered in the following sections.

Address Maps (Memory and I/O Space)

Powerup software needs to build a consistent address map before booting the machine to an operating system. This means it must determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, powerup software can map the I/O controllers into reasonable locations and proceed with system boot. In order to do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space.

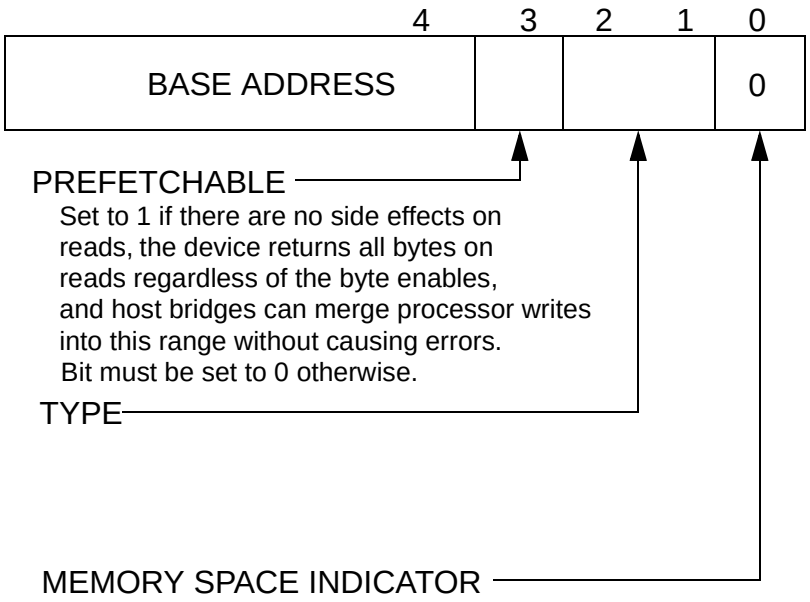


Figure 1-6 Base Address Register for Memory

Bit 0 in all base registers is read-only and used to determine whether the register maps into memory or I/O space. Base registers that map to memory space must return a zero in Bit 0. Base registers that map to I/O space must return a one in Bit 0.

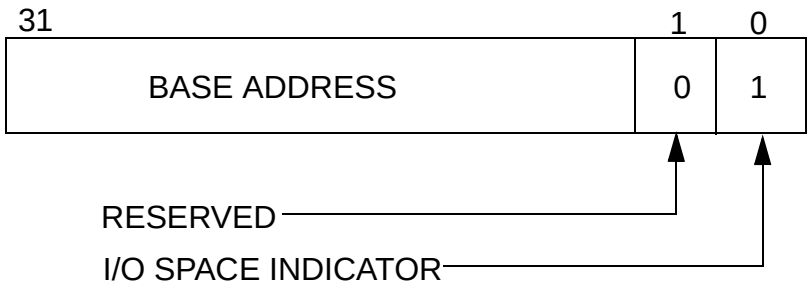


Figure 1-7 Base Address Register for I/O

Base registers that map into I/O space are always 32-bit with: Bit 0 hardwired to a one, Bit 1 reserved and must return zero on reads, and the other bits used to map the device into I/O space.

Base registers that map into memory space (Figure 1-6 can be 32-bit wide to support mapping into a 64-bit address space) have Bit 0 hardwired to a zero. For memory base registers, Bits 2 and 1 have an encoded meaning as shown in Table 1-3 below. Bit 3 should be set to one if the data is prefetchable, and reset to zero otherwise. A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bits 0 through 3 are read-only.

Table 1-3 Bits 2/1 Encoding

Bits 2/1	Definition
00	Base Register is 32 bit wide and mapping can be done anywhere in the 32 bit memory space.
01	Base Register is 32 bit wide, but must be mapped below 1 Mbyte in memory space.
10	Base Register is 64-bit wide and can be mapped anywhere in the 64-bit address space.
11	Reserved

The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. A device that wants a 1 Mbyte memory address space (using a 32-bit Base Address Register) would build the top 12 bit of the address register hardwiring the other bits to zero.

Powerup software can determine how much address space the device requires by writing a value of all ones to the register and then reading the value back. The device will return zeros in all *don't care* address bits, effectively specifying the address space required.

This design implies that all address spaces used are a power of two in size, and are naturally aligned. Devices are free to consume more address space than required, but decoding down to a 4 Kbyte space for memory and 256 bytes for I/O is suggested for devices that need less than those amounts. Devices that do consume more address space than they use are not required to respond to the unused portion of that address space.

Six DWORD locations are allocated for Base Address Registers starting at offset $10 in configuration space. The first Base Address Register is always located at offset $10. The second register may be at offset $14 or $18 depending on the size of the first. The offsets of subsequent Base Address Registers are determined by the size of previous Base Address Registers. Base Address Registers are located at offset $10 for the AMCC chip, and $14 in configuration space for the VMICPCI-2335.

A typical device will require one memory range for its control functions. Some graphics devices may use two ranges, one for control functions and another for a frame buffer. A device that wants to map control functions into both memory and I/O space at the same time must implement two base registers (one Memory, one I/O).

The driver for that device might only use one space in which case the other space will be unused. Devices should always allow control functions to be mapped into memory space.

Note

Any device that has a range that behaves like normal memory, but doesn't participate in PCI's caching protocol, should mark the range as prefetchable. A linear frame buffer in a graphics device is an example of a range that should be marked prefetchable.

Refer to the *PCI Local Bus Specification Revision 2.1* for detailed information about PCI bus. The contact information to order the *PCI Local Bus Specification Revision 2.1* is given on page 14 of this manual.

CHAPTER
2

Configuration and Installation

Contents

Introduction

The VMICPCI-2335 16-Channel Digital Output Board with Built-in-Test is designed to provide isolation between the system hardware and the CPCI backplane. The board can be either current sinking or voltage sourcing, depending on the option ordered.

Unpacking Procedures

Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

Physical Installation

Do not install or remove the board while power is applied.

De-energize the equipment and locate the appropriate CompactPCI slot. While ensuring that the card is properly aligned with the card guides, press the board smoothly into the mating connector until firmly seated.

Board Configuration

The VMICPCI-2335 board can be factory configured for current sinking or voltage sourcing outputs. Pull-up resistors for the outputs are installed if the voltage sourcing configuration is ordered. The outputs for voltage sourcing are configured with one external voltage pin for every eight channels.

Output Topology

Figure 2-1 shows the circuit topology for voltage sourcing outputs. Figure 2-2 shows the circuit topology for the current sinking configuration. Table 2-1 shows the two external voltage inputs and the output channels affected by each.

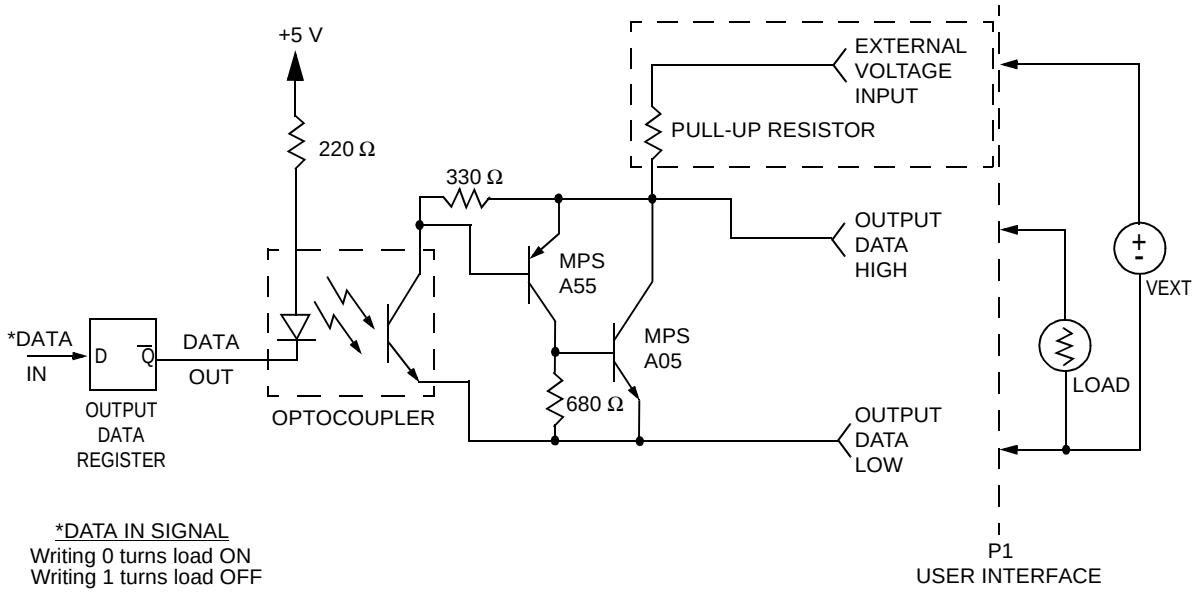


Figure 2-1 Typical Voltage Sourcing Output Configuration

Table 2-1 External Voltage

External Voltage	Channels Affected	P1 Pin
VEXT 0	Output Channels 0 through 7	36
VEXT 1	Output Channels 8 through 15	17

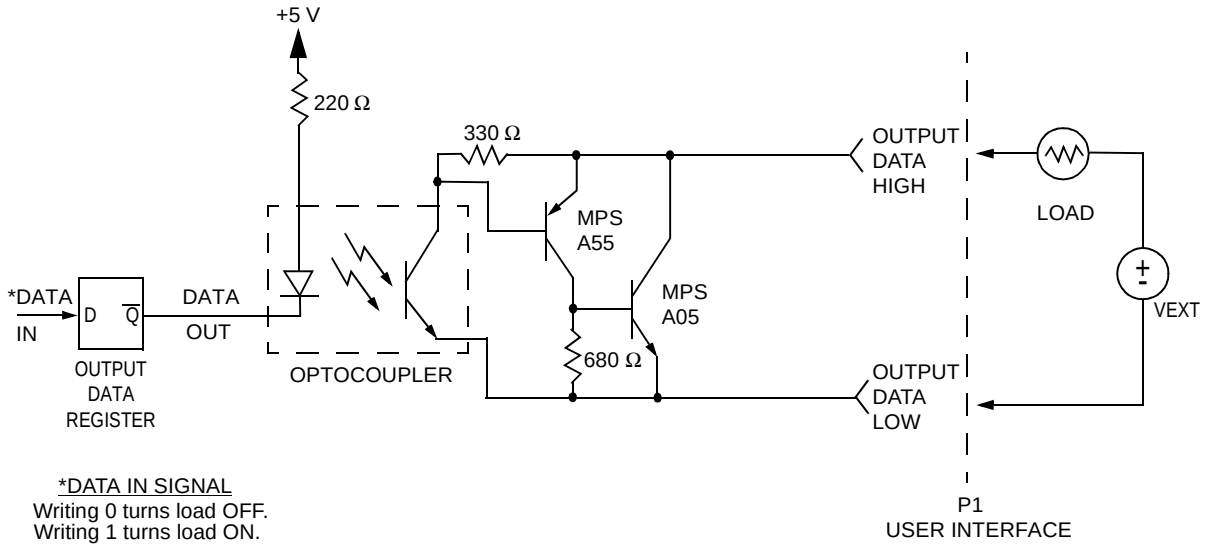


Figure 2-2 Typical Current Sinking Output Configuration

Address Selection

The VMICPCI-2335 board occupies 64 byte (16 Longwords) of I/O space. The choice of 64 bytes is dictated by some PCI hosts which do not properly recognize less. In fact, only the first four bytes (1 longword) are of interest, the remaining 15 longwords are just copies of the first. The actual absolute I/O address space is assigned at configuration time (along with all other PCI devices) as per PCI requirements.

The Base Address of the AMCC Micro Chip is located at offset 10h (Base Address 0).

The Base Address of the VMICPCI-2335 is found in offset 14h (Base Address Register 1).

Before Applying Power: Checklist

Before installing the board in a CompactPCI system, check the following items to ensure that the board is ready for the intended application.

1. Verify that the sections pertaining to theory and programming, Chapters 1 and 3, have been reviewed and applied to system requirements. _____
2. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to *Connector Configuration* section on page 37 for connector descriptions. _____

After the checklist above has been completed, the board can be installed in a CompactPCI system.

Do not install or remove the board while power is applied.

Connector Configuration

The panel input connector (P1) on the VMICPCI-2335 board is a standard subminiature 37-pin male D-Shell. Figure 2-4 on page 40 shows the pin layout of the P1 connector. Table 2-3 on page 38 details the connector pin assignments. The J1 connector on the VMICPCI-2335 is a 2 mm DIN 32-bit, 5 V, CompactPCI bus connector. The metal shell (row F) of the J1 connector is connected to chassis ground. See the figure and table below for the J1 connector pinout.

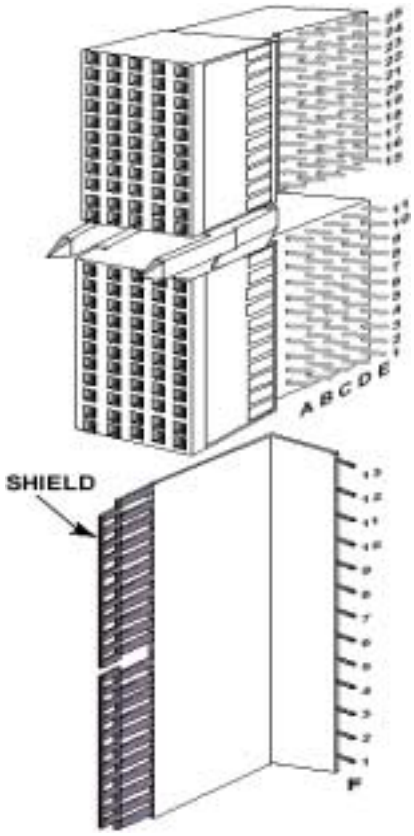


Figure 2-1 J1 Connector

Table 2-2 J1 Connector Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
25	+5 V	N/C	N/C	N/C	+5 V	GND
24	IN_AD[1]	+5 V	+5 V	IN_AD[0]	N/C	N/C
23	N/C	IN_AD[4]	IN_AD[3]	+5 V	IN_AD[2]	GND
22	IN_AD[7]	GND	N/C	IN_AD[6]	IN_AD[5]	N/C
21	N/C	IN_AD[9]	IN_AD[8]	GND	INC/BE[0]	GND
20	IN_AD[12]	GND	N/C	IN_AD[11]	IN_AD[10]	N/C
19	N/C	IN_AD[15]	IN_AD[14]	GND	IN_AD[13]	GND
18	INSERR	GND	N/C	INPAR	INC/BE[1]	N/C
17	N/C	N/C	N/C	GND	INPERR	GND
16	IN_DEVSEL	GND	+5 V	INSTOP#	INLOCK	N/C
15	N/C	IN_FRAME	INIRDY	GND	INTRDY	GND
12 through 14 are lost to the keying area						
11	IN_AD[18]	IN_AD[17]	IN_AD[16]	GND	INC/BE[2]	GND
10	IN_AD[21]	GND	N/C	IN_AD[20]	IN_AD[19]	N/C
9	INC/BE[3]	INIDSEL	IN_AD[23]	GND	IN_AD[22]	GND
8	IN_AD[26]	GND	+5 V	IN_AD[25]	IN_AD[24]	N/C
7	IN_AD[30]	IN_AD[29]	IN_AD[28]	GND	IN_AD[27]	GND
6	N/C	GND	N/C	CLK	IN_AD[31]	N/C
5	N/C	N/C	INRST	GND	N/C	GND
4	N/C	GND	+5 V	N/C	N/C	N/C
3	N/C	N/C	N/C	+5 V	N/C	GND
2	N/C	+5 V	N/C	N/C	N/C	N/C
1	+5 V	N/C	N/C	N/C	+5 V	GND

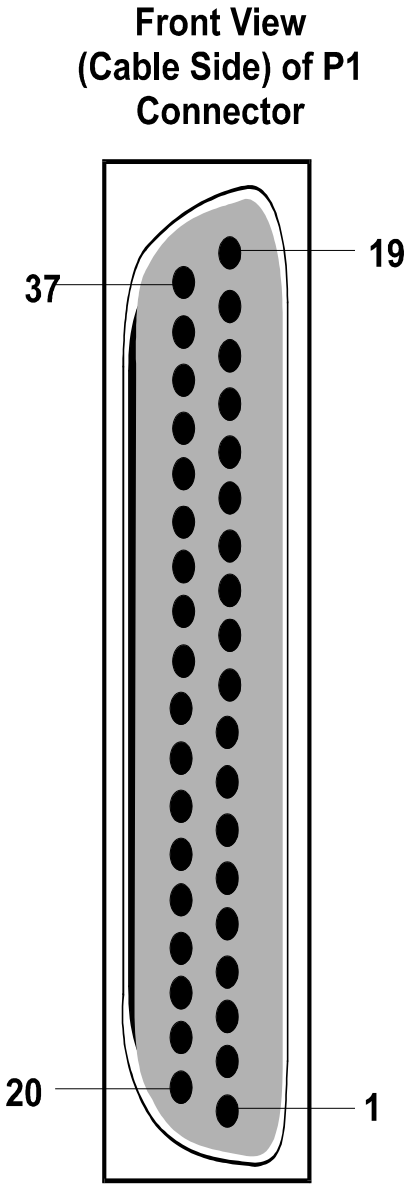


Figure 2-3 P1 Connector Pin Layout

Table 2-3 P1 Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
37	N / C	19	N / C
36	VEXT 0	18	N / C
35	LOW OUT 15	17	VEXT 1
34	LOW OUT 14	16	HIGH OUT 15
33	LOW OUT 13	15	HIGH OUT 14
32	LOW OUT 12	14	HIGH OUT 13
31	LOW OUT 11	13	HIGH OUT 12
30	LOW OUT 10	12	HIGH OUT 11
29	LOW OUT 9	11	HIGH OUT 10
28	LOW OUT 8	10	HIGH OUT 9
27	LOW OUT 7	9	HIGH OUT 8
26	LOW OUT 6	8	HIGH OUT 7
25	LOW OUT 5	7	HIGH OUT 6
24	LOW OUT 4	6	HIGH OUT 5
23	LOW OUT 3	5	HIGH OUT 4
22	LOW OUT 2	4	HIGH OUT 3
21	LOW OUT 1	3	HIGH OUT 2
20	LOW OUT 0	2	HIGH OUT 1
		1	HIGH OUT 0
Shield			Chassis GND

CHAPTER
3

Programming

Contents

Introduction

The VMICPCI-2335 board requires very little software. After performing any initialization or off-line testing, the user enters on-line mode by writing to the Control and Status Register (CSR). The user may then perform a write operation to the appropriate output register to modify the state of the field.

Where appropriate, information on programming these registers is provided. All values are in hexadecimal unless otherwise indicated.

The programming model for these register definitions includes a table with five lines. Line one is the base address offset of the register and the number of bits defined in the table. Line two shows the bits defined by this table. Line three defines the name of the register or the name of the bits in the register. Line four defines the operations possible on the register bits as follows:

R	This bit is a read-only status bit.
R/W	This bit is readable and writable.
W	This bit is a write-only control bit.
WC	This bit is a write-to-clear control bit.

Line five defines the state of the bit following a reset as defined below:

P	The bit is set to the default state by a powerup reset.
S	The bit is set to the default state by a SYSRESET.
L	The bit is set to the default state by a local reset.
X	The bit is **not** affected by reset.

I/O Space Definition

The VMICPCI-2335 board reserves 64 bytes of I/O and Memory space. Of each of these 64 bytes, only 4 bytes (1 longword) are of interest. Figure 3-1 shows the definition for this longword.

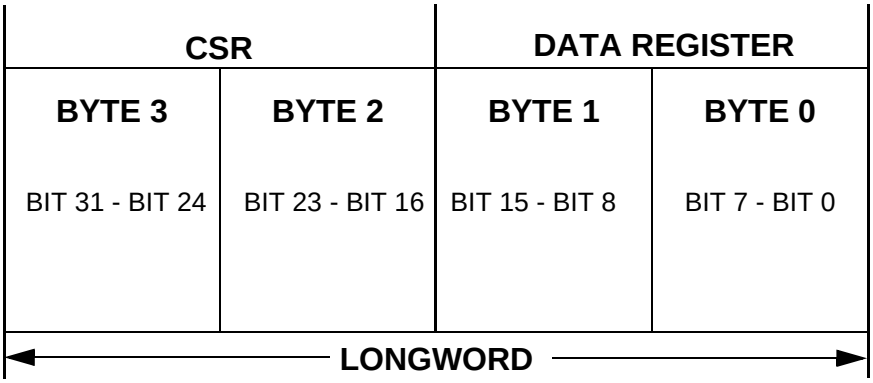


Figure 3-1 I/O and/ or Memory Space Definition

Control and Status Register (CSR)

Bytes 3 and 2 of the I/O address space are comprise of the Control and Status Register (CSR). The CSR is a 16-bit register that is used to control the board's Fail LED and online/off-line status. Table 3-1 shows the position of the bits used to perform these functions. All control bits (31 through 16) will be LOW on powerup or after a PCI bus reset. This ensures that the board is in the off-line mode, and prevents the board from interacting with the field until it receives a command from the host. This will also cause the Fail LED to illuminate.

The Base Address value is assigned by the system at powerup or after a resets Base Address Register 1. This value can be seen when reading the configuration space. This value plus the offset value must be used to access the CSR and Data Registers. For example, the base address could be FBC1 at powerup. Then to access CSR Byte 3, the address would be FBC3.

Base Address Register 1 would read FBC1 (1 = I/O space), the 1 should **NOT** be used when obtaining address and offset.

Table 3-1 Control and Status Register's Bit Map (Byte 3)

Control and Status Register, Byte 3, Offset: 0x0003 (Read/Write)							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Reserved			EN_LB	Reserved		EN_UB	Fail_LED

Bits 31 to 29: Reserved These bits are reserved and will always read back as 0. Data written to these locations will be lost and has no effect on the board. However, these bits should be written to 0 to maintain software compatibility for possible future enhancements which may utilize any one of them.

Bit 28: EN_LB **Enable/Disable Lower Byte (Data 0-7)**. Controls the ON/OFF status of data lines 0 through 7. Writing a 0 to this bit places these lines in the on-line mode and enables PCI bus writes to control the state of output lines 0 through 7. Writing a 1 to this bit places these lines in the off-line mode and disables output lines 0 through 7 from being controlled from the PCI bus. At powerup or reset, this bit is set low.

Bits 27 to 26: Reserved These bits are reserved and will always read back as 0. Data written to these locations will be lost and has no effect on the board. However, these bits should be written to 0 to maintain software compatibility for possible future enhancements which may utilize any one of them.

Bit 25: EN_UB **Enable/Disable Upper Byte (Data 8-15)**. Controls the ON/OFF status of data lines 8 through 15. Writing a 0 to this bit places these lines in the on-line mode and enables PCI bus writes to control the state of output lines 8 through 15. Writing a 1 to this bit places these lines in the off-line mode and disables output lines 8 through 15 from being controlled from the PCI bus. At powerup or reset, this bit is set low.

Bit 24: **FAIL_LED Fail LED Bit**. Controls the Fail LED. Writing a 1 to this bit will turn the Fail LED OFF. At powerup or reset, this bit is set low causing the LED to be ON.

Table 3-2 Control and Status Register's Bit Map (Byte 2)

Control and Status Register, Byte 2, Offset: 0x0002 (Read/Write)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved							

Bits 23 to 16: Reserved These bits are reserved and will always read back as 0. Data written to these locations will be lost and has no effect on the board. However, these bits should be written to 0 to maintain software compatibility for possible future enhancements which may utilize any one of them.

Output Data Register Bit Definitions

Table 3-3 and Table 3-4 list the channels and their associated register bit locations. Byte 1 of the Output Data Register contains the upper byte of output data; Byte 0 contains the lower byte of output data. The Output Data Register can be read as a Byte or Word.

Table 3-3 Output Data Register's Bit Map (Byte 1)

Output Data Register Byte 1, Offset: 0x0001, Word/Byte, (Read/Write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
CH15	CH14	CH13	CH12	CH11	CH10	CH09	CH08

Bit 15: CH 15 **Channel 15 Output Control Bit**. This bit directly corresponds to Channel 15. If Bit 25 of the CSR is set (1) and Bit 15 of the Output Data Register Byte 1 is set (1), the output circuitry for Channel 15 is active. Bits 14 to 08 will follow the same format for their respective channels.

Bit 14: CH 14 **Channel 14 Output Control Bit**. See description for Bit 15.

Bit 13: CH 13 **Channel 13 Output Control Bit**. See description for Bit 15.

Bit 12: CH 12 **Channel 12 Output Control Bit**. See description for Bit 15.

Bit 11: CH 11 **Channel 11 Output Control Bit**. See description for Bit 15.

Bit 10: CH 10 **Channel 10 Output Control Bit**. See description for Bit 15.

Bit 09: CH 09 **Channel 09 Output Control Bit**. See description for Bit 15.

Bit 08: CH 08 **Channel 08 Output Control Bit**. See description for Bit 15.

Table 3-4 Output Data Register's BitTable Map (Byte 0)

Output Data Register Byte 0, Offset 0x0000, Word/Byte (Read/Write)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH07	CH06	CH05	CH04	CH03	CH02	CH01	CH00

Bit 07: CH 07 **Channel 07 Output Control Bit**. This bit directly corresponds to Channel 07. If Bit 28 of the CSR is set (1) and Bit 07 of the Output Data Register Byte 0 is set (1), the output circuitry for Channel 07 is active. Bits 06 to 00 will follow the same format for their respective channels.

Bit 06: CH 06 **Channel 06 Output Control Bit**. See description for Bit 07.

Bit 05: CH 05 **Channel 05 Output Control Bit**. See description for Bit 07.

Bit 04: CH 04 **Channel 04 Output Control Bit**. See description for Bit 07.

Bit 03: CH 03 **Channel 03 Output Control Bit**. See description for Bit 07.

Bit 02: CH 02 **Channel 02 Output Control Bit**. See description for Bit 07.

Bit 01: CH 01 **Channel 01 Output Control Bit**. See description for Bit 07.

Bit 00: CH 00 **Channel 00 Output Control Bit**. See description for Bit 07.

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Maintenance Prints

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.