VMICPCI-3322
16-Channel, 16-bit Analog-to-Digital Converter (ADC) Board

Product Manual

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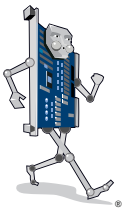

(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

VMIC

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Overview

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Introduction

The VMICPCI-3322 16-Channel, 16-bit Analog-to-Digital Converter (ADC) board is a 16-channel analog input board with 16-bit digitizing resolution on a 3U CompactPCI form factor. The VMICPCI-3322 is jumper-selectable, supporting several input ranges. Also through factory-installed options, differential or single-ended modes, and optional low pass input filters can be accommodated.

The VMICPCI-3322 automatically scans and digitizes (autoscans) up to 16 inputs at a rate of 10.05 µs per channel and stores the results in consecutive SRAM locations. The host PC may then read the results from the SRAM through the PCI bus at an independent rate. In addition to the 16 SRAM locations, the VMICPCI-3322 contains a single Control and Status Register (CSR) which is used to enable the basic functions and report status.

The following is a brief overview of the VMICPCI-3322 board:

- 16 differential or single-ended analog inputs
- 16-bit ADC autoscanning conversion
- 10.05 µs per channel conversion time
- Programmable 16 or 8 channels per scan cycle
- ADC ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, and 0 to +10 V
- Optional low pass input filters
- Poll Mode, when enabled, continually samples and converts a selected input channel

Functional Description

A functional block diagram of the VMICPCI-3322 16-Channel 16-bit Analog-to-Digital Converter (ADC) board is shown in Figure 1 on page 13. The major sections of the circuitry include 16 pairs of input buffers, a 16-channel differential multilplexer, an instrumentation amplifier, a 16-bit Analog-to-Digital Converter, 32 SRAM registers, timing and control circuitry, and a PCI bus interface. The PCI interface is incorporated in a single PCI-compliant device. In addition, all timing and control circuitry, including the CSR, is located in one EPLD device.

Through the CSR you can:

- Select the output data format
- Turn the Fail LED OFF or ON
- Select the number of inputs (16 or 8) to scan / convert
- Enable autoscan
- Issue a software reset
- Select a channel to be continuously scanned and converted by enabling Poll Mode

Upon powerup, system reset, or software reset, the ADC performs a self-calibration which takes approximately 41 ms. Also upon reset, the CSR is cleared and the autoscan cycle is disabled. The autoscan cycle remains disabled until an enable bit in the CSR is set. While the autoscan cycle is disabled, the SRAM can be verified through a series of PCI bus reads and writes.

Normally the CSR is written at least once to select the number of inputs to scan, select the output data format, and to enable the autoscan cycle. Once the autoscan is enabled, the VMICPCI-3322 sequentially samples the selected number of inputs, converts each conditioned sample to a 16-bit digital value, and stores the result in the corresponding SRAM location. Arbitration circuitry permits the host PC to read any of the SRAM locations at any time without affecting the autoscan and digitization timing.

Poll Mode is entered by writing a one (**1)** to the POLLENA bit in the CSR, and selecting a channel to be continuously polled by writing ones (**1)** to the proper PB bits in the CSR. After enabling Poll Mode, the selected channel is repeatedly sampled and converted into a digital value and stored in the selected channel number location in SRAM.

To achieve the sample rate of 10.05 µs per channel, the sample and conversion process is pipelined. Prior to converting each sample, an integral sample-and-hold within the ADC device switches to hold. Then while the ADC is converting one channel, the Analog Mux and Instrumentation Amplifier are switched to the next input to slew and settle. Likewise, the SRAM write of each conversion result is written while the ADC is converting the next channel.

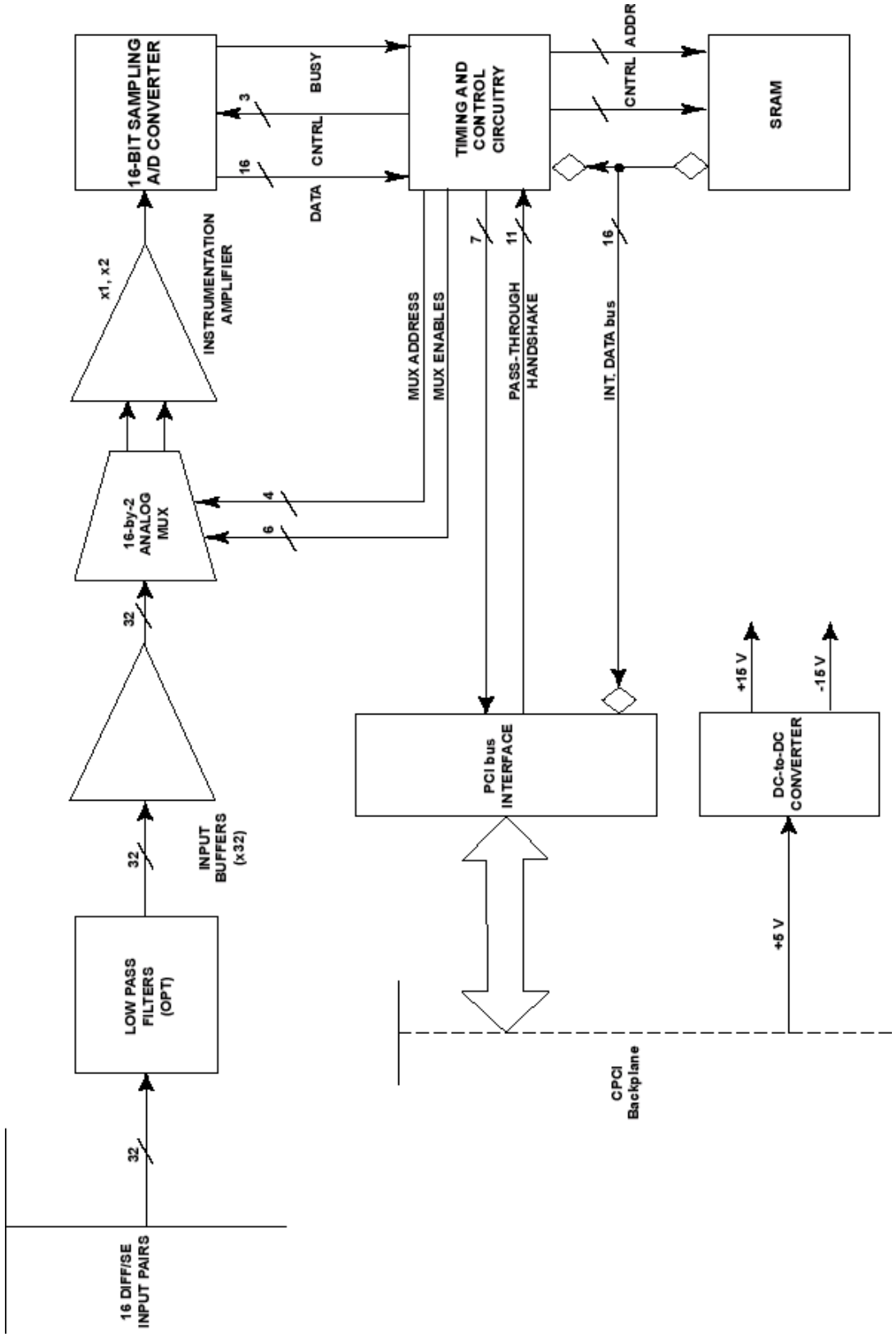


Figure 1 VMICPCI-3322 Functional Block Diagram

Related Documents

For a detailed explanation of the PCI local bus and its characteristics, refer to the *PCI Local Bus Specification* from:

PCI Local Bus Specification, Revision 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)

For a detailed explanation of the CompactPCI™ bus and its characteristics, refer to the *CompactPCI™ Specification, 2.0 R2.1* from:

PCI Industrial Manufacturers Group
(PICMG)
301 Edgewater Place
Suite 220
Wakefield, MA 01880 USA
(617) 224-1100
(503) 797-4207 (International)
Fax: (617) 224-1239
Web: http://www.PICMG.ORG

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

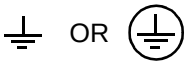
Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

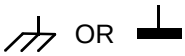
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



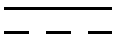
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

The STOP symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER
1

Theory of Operation

Contents

Introduction

This section describes the internal operation of the VMICPCI-3322 board and reviews the general principles of operation. The information in this section is supplemented by programming details in Chapter 3 and by the schematic diagrams in Appendix A. The VMICPCI-3322 board contains the following principal hardware functions, as shown in Figure 1 on page 13:

1. PCI bus Interface
2. SRAM
3. Power Converter
4. Optional Low Pass Input Filters

5. Analog Input Buffers
6. Analog Multiplexer
7. Instrumentation Amplifier
8. Analog-to-Digital Converter (ADC)
9. Timing and Control Circuitry

The above topics are discussed in greater detail in the following subsections.

PCI bus INTERFACE

The VMICPCI-3322 board is implemented with a PCI bus-compliant interface device. The VMICPCI-3322 operates as a PCI bus I/O *target* and supports simple *plug-and-play* capability. On one side, the PCI bus device contains the proper signals and timing to operate on the PCI local bus. On the other side, the PCI device provides an *add-on* interface to which the desired function specific circuitry is connected. In addition, the PCI bus interface device contains the full complement of predefined configuration registers.

PCI bus Configuration Registers

Any PCI bus interface, which is compliant with the PCI bus specification, contains a predefined group of configuration registers. This group of registers implements the primary PCI bus functions of identification, PCI bus command/status, and board configuration. Several of the standard registers, though present in the PCI bus interface device, do not apply to the VMICPCI-3322 board. However, registers that do apply are listed in Table 1-1 below.

For a detailed explanation of the PCI local bus and its characteristics refer to the *PCI Local Bus Specification, Revision 2.1 (See Related Documents* on page 14*).*

Table 1-1 PCI Configuration Registers

Offset Address (HEX)	Register	Mnemonics	VMICPCI-3322 Value (HEX)	Access
00 through 01	Vendor Identification	VID	114A	Read-Only
02 through 03	Device Identification	DID	3322	Read-Only
04 through 05	PCI Command Register	PCICMD	0001	Read/Write
06 through 07	PCI Status Register	PCISTS	Varies	Read/*Write
08	Revision ID Register	RID	Varies	Read-Only
09 through 0B	Class Code Register	CLCD	FF	Read-Only
10 through 13	Base Address Register 0	BADR0	Varies	Read/Write
14 through 17	Base Address Register 1	BADR1	Varies	Read/Write
18 through 21	Base Address Register 2	BADR2	Varies	Read/Write

Any write to the PCISTS register clears the register.

PCI bus Operation Registers

Base Address Register 0 contains a 32-bit address, which points to a second group of 16 DWORD (32-bit) registers. These registers are called the PCI bus Operation Registers; they are not involved in the basic VMICPCI-3322 operation.

VMICPCI-3322 Function Registers

The VMICPCI-3322 has both I/O and memory mapped configuration registers. Both of the PCI bus configuration registers, called Base Address Register 1 (BADR1), and (BADR2) contain a 32-bit address, which is the base address of the function specific registers that apply to the VMICPCI-3322 board. Either of these registers can be read as the main configuration register, since writes to one are automatically updated in the other register. The main reason for two such registers is that it offers application programmers more flexibility as to the method of controlling access to the board. Both function in an identical fashion with I/O mapping at offset 14h and memory mapping at offset 18h. A group of 128-byte addresses are dedicated to these functions. Within the 128-byte address space, only the even addresses are used, since all VMICPCI-3322 function specific registers are organized as 16 bits wide. Any of the first 8 even addresses, with offsets `$0` through `$E`, access the VMICPCI-3322 Control and Status Register (CSR). The next 32 even addresses, with offsets `$10` through `$4E`, access 32 SRAM locations. The first 16 of these SRAM locations store the digital values that represent the 16 analog inputs. The last 16 SRAM locations are spares. All the remaining byte address with offsets `$40` through `$7F` are reserved.

SRAM

The VMICPCI-3322 board contains 32, 16-bit wide SRAM locations accessible by the user. While the autoscan cycle is operating, the lower 16 locations of the SRAM store the conversion results of the corresponding input channels. The upper 16 SRAM locations, though accessible, have no specific function. The SRAM is PCI bus accessible by way of the even relative addresses `$10` through `$4E` (the relative addresses are with respect to the contents of the Base Address Register 1.) All the SRAM locations may be written and read by way of the PCI bus. However, while the autoscan cycle is operating, the first 16 locations are also periodically written with conversion results. Therefore, while performing a memory test on the SRAM, the autoscan should be disabled. See Table 3-1 on page 56 for the memory map covering the SRAM relative addresses.

Power Converter

The ±15 V power for the analog circuitry is supplied by an on-board DC-to-DC Converter, which is sourced by +5 V from the CompactPCI backplane.

Low Pass Filters

The VMICPCI-3322 board's inputs utilitize a single-pole passive low pass filters (optional) to minimize the effects of system noise and eliminate high-frequency signals, which would otherwise cause accuracy problems. The input filters also limit the upper frequency of the signal that can accurately be converted. Therefore, the filter options should be chosen with both the signal characteristics and system requirements in mind.

The VMICPCI-3322 offers four low pass filter options based on the -3 dB or corner frequency.

Those options are:

1. No filter
2. -3 dB at 50 Hz
3. -3 dB at 100 Hz
4. -3 dB at 500 Hz

The above cutoff frequencies apply to differential inputs. When the inputs are single-ended, the corner frequencies double.

Input Buffers

Each of the 16 differential inputs has a dedicated pair of input buffers. The input buffers eliminate errors resulting from high or varying source impedance. In addition, the buffers maintain high input impedance and minimize channel interaction while also permitting high sample rates.

Analog Multiplexer (MUX)

The Analog Multiplexer is a 16-channel differential structure, configured in two tiers. The first tier is composed of four multiplexers. Each of the multiplexers in the first tier can select one of four differential buffered pairs. The second tier then selects one of the four first tier outputs and gates the resulting selected pair to the input of the Instrumentation Amplifier. The MUX address and enables, which come from the timing and control circuits, are tailored to ensure break-before-make switching and minimal channel interaction.

Instrumentation Amplifier

The Instrumentation Amplifier converts the selected differential signal pair to a single-ended signal referenced to the ADC analog ground (AGND). It provides the high common-mode rejection required to achieve the rated accuracy. The Instrumentation Amplifier has a nominal gain of one, but can be jumpered for a gain of two, which is necessary for the ±2.5 V and 0 to 5.0 V ranges.

Analog-to-Digital Converter (ADC)

The ADC is a 16-bit successive approximation device with integral sample-and-hold and a output data latch. Each conversion takes 10.05 µs. A conversion is initiated by 2.0 µs sample command, during which the sample-and-hold is in the sample mode and the converter clock is inactive. In the remaining 8.05 µs following the end of the sample command, the sample-and-hold switches to hold, and the converter digitizes the analog sample with 17 toggles of the converter clock. Following the rising edge of the 17th clock, a 16-bit output data latch is updated to the digital representation of the sampled analog signal. The output latch will then maintain this digital word until the completion of the next conversion. Figure 1-1 on page 29 shows the VMICPCI-3322 board's autoscan timing, which focuses on the ADC timing.

The combination of the sample-and-hold and the output data latch permits pipelining of the conversion cycle. Once the sample-and-hold has switched to hold and the ADC begins the conversion process, the input Multiplexer and Instrumentation Amplifier are switched to the next channel to slew and settle. Likewise, the result of each conversion is not written into the SRAM until the ADC is digitizing the next sample.

The ADC contains a self-calibration feature to achieve and maintain the 16-bit accuracy. Upon system reset or a software issued reset, a calibration signal is asserted to the ADC. Then for the next 85,530 converter clock cycles (approximately 41 ms), the ADC performs a self-calibration. An ADC calibration busy flag is available in the Status Register if needed. The flag alerts the user that calibration is complete.

Timing and Control Circuitry

All timing and control circuitry is located in a single EPLD device. This includes the Control and Status Register (CSR), the state machine, the signal lines that controls PCI bus accesses, the state machine signal lines that controls the analog MUX switching, ADC conversion, and the circuitry involved with ADC calibration timing. Figure 1-1 on page 29 shows the VMICPCI-3322 board's autoscan timing.

Control and Status Register (CSR)

The Control and Status Register is accessible through any even relative addresses $0 through $E. The control register has 11 of the possible 16 bits used. Three of four bits control the Fail LED, the software reset, and the autoscan enable. A fourth control bit selects the data format between two's complement or straight / offset binary. The fifth control bit is a self-test flag, which only echoes back into the Status Register. The next two control bits enable Poll Mode and select the number of channels to autoscan. The next 5 bits in the control word are reserved and should be written as zero. The last four bits are used during Poll Mode to select the channel to continually poll. Any PCI bus read of relative addresses $0 through $E yields a status word. The status word echoes back the corresponding control register bits and also contains a calibration busy bit. The unused status word bits are reserved and read as zero.

Poll Mode is a feature of the VMICPCI-3322 board when enabled allows the user to select one of the 16 possible input channels and continuously sample and convert that channel's analog sample to a digital value then store that value in SRAM. Poll Mode is entered by writing a one (**1)** to the POLLENA bit in the CSR and writing ones (**1)** to the corresponding PB bits to select the desired channel to be repeatedly sampled.

The SCANENA and the POLLENA bits in the CSR should never be written HIGH at the same time. Writing both of these bits HIGH simultaneously will produce an inoperable condition for the VMICPCI-3322.

SRAM Arbitration

The possibility of both the autoscan state machine and the PCI bus attempting to access the SRAM at the same time does exist. The timing and control circuitry includes arbitration logic to prevent such access collisions from causing erroneous operation. Either of the two that the start second access is delayed until the first access is complete. If the PCI bus access is the latter, the delay might cause access to exceed a 16 PCI bus clock limit. In that event, the PCI bus interface device issues a PCI bus *retry* request and the PCI bus controller repeats the access. The retry process is, for the most part, transparent to the user. Also, regardless of the arbitration, the overall autoscan timing is unaffected.

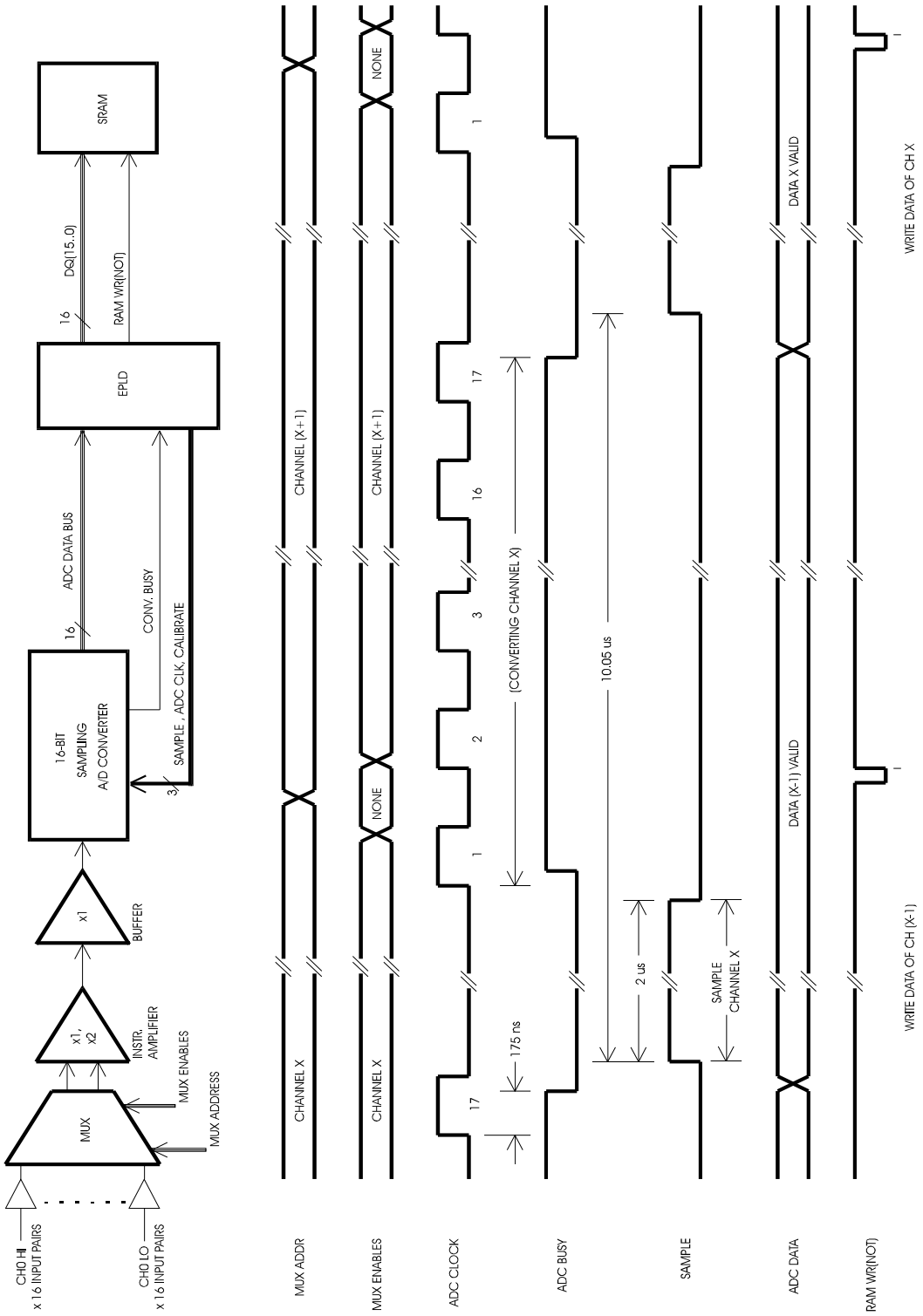


Figure 1-1 VMICPCI-3322 Timing Diagram

CHAPTER 2

Configuration and Installation

Contents

Introduction

The VMICPCI-3322 is designed to operate on the industrial standard 5 V CompactPCI Backplane, and supports up to 16 channels of differential or single-ended inputs within the full-scale range of ±2.5 to ±10 V. The board continuously scans the selected inputs, converts each sample to a digital value, and stores the results in dual-ported data registers. The data format of channels scanned is program-selectable between straight/offset binary and two's complement.

The VMICPCI-3322 converts at an aggregate rate of 99.5 kHz. The individual channel sample rate is 99.5 kHz divided by the number of channels scanned.

The scan rate per channel is: 6.218 kHz if all 16 channels are scanned

12.437 Hz if 8 channels are scanned

99.5 kHz if a single channel is being scanned

Unpacking Procedures

Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that may have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. This board can be installed in any slot position with a circle above the handle and also on the backplane, the slot with a triangle above the handle is reserved for the system controller.

This symbol identifies the System Controller slot

This symbol identifies the slot in which the VMICPCI-3322 can be installed

Do not install or remove the board while power is applied.

Prior to installing the board, verify that the jumpers are configured as described in *Operational Configuration* section on page 35.

Before Applying Power: Checklist

Before applying power to a board in a CompactPCI system, check the following items to ensure that the board is ready for the intended application:

1. Review the *Connector Configuration* and *Operational Configuration* sections of this manual. Apply all system requirements found there. _____
2. Review and apply the sections pertaining to theory and programming. _____
3. Correctly install the jumpers as described in the section, *Operational Configuration* section on page 35. _____
4. Correctly install the I/O cable with the proper mating connector on port P1. Refer to *Connector Descriptions* section on page 51 for a description of compatible mating connectors. _____
5. Ensure the calibration is correct. Calibration for the ±10 VDC range has been performed at the factory. If recalibration should be required, refer to *Calibration* section on page 38. _____
6. Ensure that all system cable connections are correct. ____

After the checklist above has been completed, the board can be powered on in a CompactPCI system.

Operational Configuration

As with other PCI bus cards, the I/O address space, through which the VMICPCI-3322 board operates, is assigned dynamically by the system BIOS and is not predefined by jumpers. The VMICPCI-3322 does provide four jumpers that determine the input range and type. Location and function of the VMICPCI-3322 jumpers are shown in Figure 2-2 on page 35 and listed in Table 2-1 below.

Table 2-1 Programmable Jumper Functions

Jumper	Function When Installed	Factory Conf.
E3: pins 1,2	±2.5 V, 0 to 5 V, ±5 V, 0 to +10 V Ranges	Omitted
E3: pins 2,3	±10 Range	Installed
E4: pins 1,2	Bipolar Operation	Installed
E4: pins 2,3	Unipolar Operation	Omitted
E1: pins 1,2	Instrumentation Amp. (x2) multiplier (paired with E2)	Omitted
E2: pins 1,2	Instrumentation Amp. (x2) multiplier (paired with E1)	Omitted

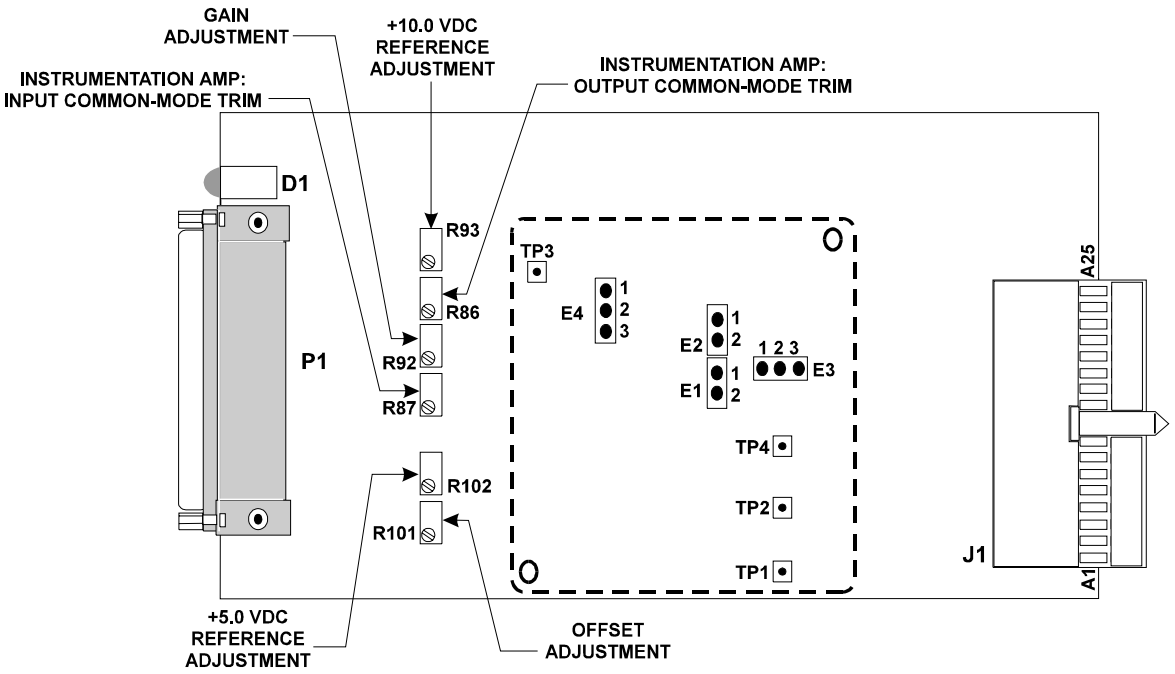


Figure 2-2 Location of Test Points, Potentiometers, and Jumpers

Factory-Installed Jumpers

Each VMICPCI-3322 board is configured at the factory with a specific jumper arrangement as shown in Table 2-1 on page 35. The factory configuration establishes the following functional baseline for the VMICPCI-3322 board, and ensures that all essential jumpers are installed.

- ±10 V input range
- Differential inputs

The VMICPCI-3322 has an RF Shield covering the jumpers and test points. The shield must be removed before configuration of the jumpers is possible. Figure 2-3 below illustrates the removal and installation of the RF Shield.

Do not install or remove the RF Shield while power is applied.

Perform the following steps:

1. Using a #1 Phillips Screwdriver, remove the two Phillips Head Screws holding the RF Shield to the PC board.
2. Carefully remove the shield from the PC board. To install the shield, reverse the order that the shield was removed.

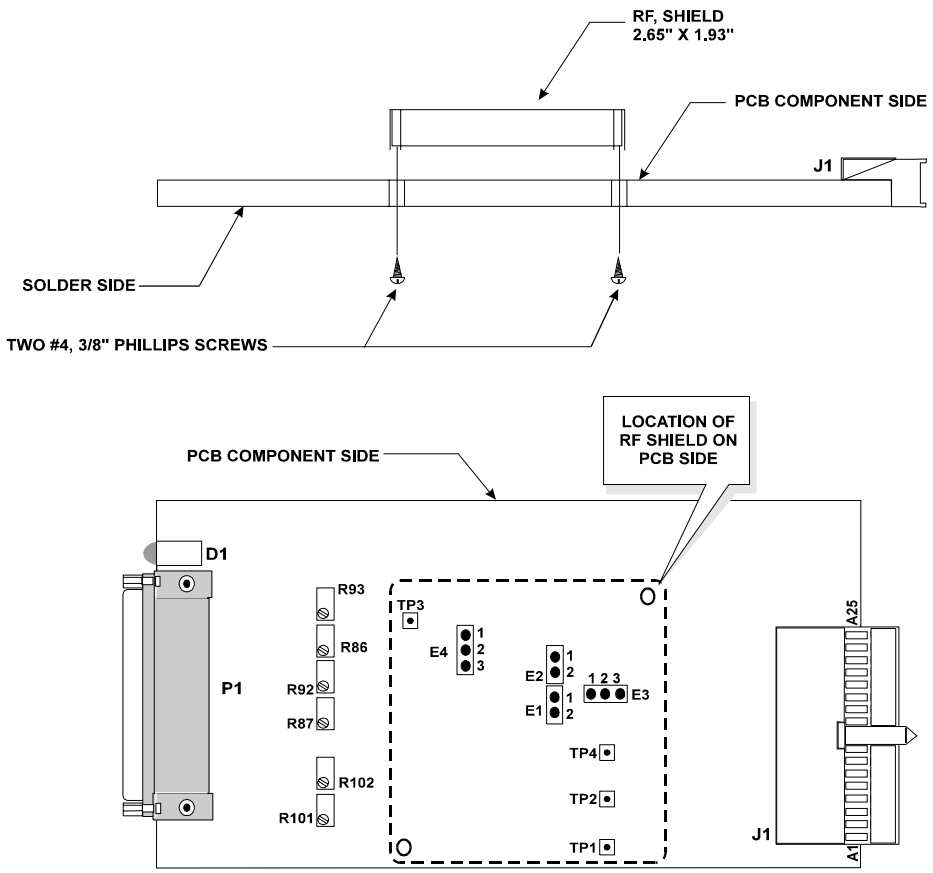


Figure 2-3 RF Shield Installation and Removal

Conversion Range Selection

The conversion range of the VMICPCI-3322 board is configured using the jumper combinations shown in Table 2-2 below. See Figure 2-2 on page 35 for jumper locations.

Table 2-2 Conversion Range Selection

Jumper	Input Voltage Range				
	±10 V	±5 V	±2.5 V	0 to +10 V	0 to +5 V
E3	2,3	1,2	1,2	1,2	1,2
E4	1,2	1,2	1,2	2,3	2,3
E1	Removed	Removed	Installed	Removed	Installed
E2	Removed	Removed	Installed	Removed	Installed

Input Configuration

The analog inputs are configured as single-ended or differential by the factory installation of resistor networks. Each active input, both HIGH and LOW, is referenced to on-board analog ground through a 22 MΩ resistor. The 22 MΩ resistors provide floating input protection while still maintaining high input impedance. In addition, each active input has a 3.9 kΩ series resistor to limit current in overvoltage conditions and to partially implement the input low pass filter. When the inputs are configured as single-ended, the 3.9 kΩ series resistor in the LOW input paths are omitted and, instead, the LOW paths are tied to analog ground through separate resistor networks. When the board is configured in the single-ended mode, the P1 connector pins corresponding to LOW inputs are not connected to any board circuitry.

Calibration

Before delivery from the factory, the VMICPCI-3322 board is fully calibrated and conforms to all factory specifications. Should recalibration be required, however, perform the appropriate procedures in *Base Address Determination* section on page 39 with the test equipment listed in the *Equipment Required* section below. The locations of all adjustments and test points are shown in Figure 2-2 on page 35. Adjustment potentiometers and their functions are listed in Table 2-3 below.

Table 2-3 Adjustment Potentiometers

Potentiometers	Function
R92	Gain Adjustment
R87	Instrumentation Amp: Input common-mode trim
R86	Instrumentation Amp: Output common-mode trim
R101	Offset Adjustment
R93	+10.0 VDC Reference Adjustment
R102	+5.0 VDC Reference Adjustment

Equipment Required

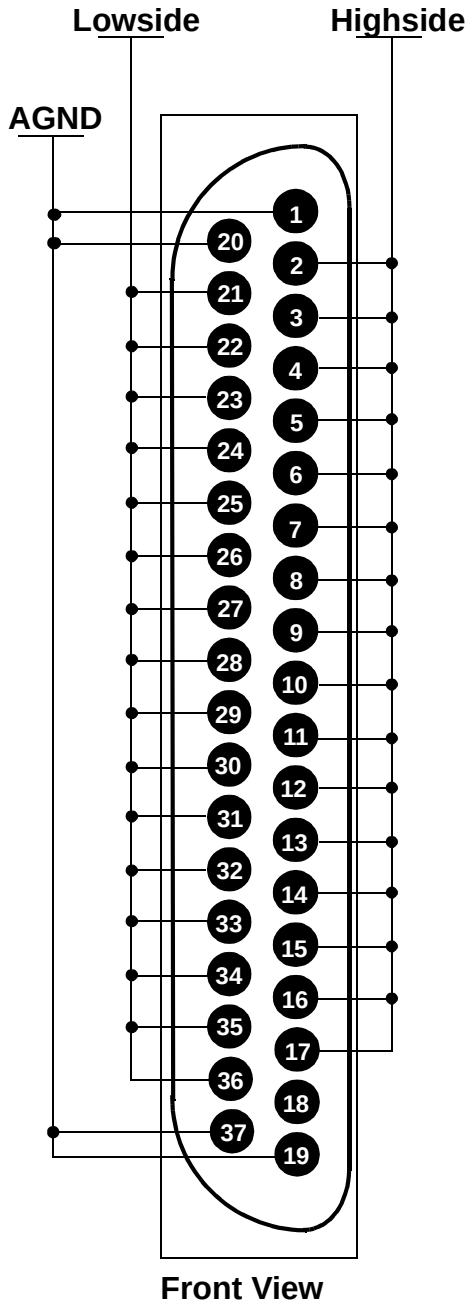
The following is a required list of equipment:

1. **Digital Multimeter (DMM):** ±1.00000 VDC and ±10.0000 VDC ranges; 6 or more digits; ±0.003 percent of reading voltage measurement accuracy; 10 MΩ minimum input impedance.
2. **Digital Voltage Source:** 10.0000 VDC ±0.0001 VDC voltage source, 7-digit setting resolution and ±0.003 percent accuracy, 10 Ω maximum source resistance.
3. **CompactPCI Host System:** The CompactPCI Host System requires a minimum of one open 5 V slot, one 3.5-inch floppy diskette drive and interface, a monitor, a keyboard, and the associated power supply.
4. **CompactPCI Extender Board:** Depending on the configuration of the CompactPCI host system, it may be necessary to use a CompactPCI extender board to ensure access to the adjustment potentiometers.
5. **Test Cables:** Test leads for the equipment listed above. Three short (not longer than 6 inches) test leads with mini-clips or alligator clips on both ends.
6. **Test Adapter:** A 37-pin D-shell male connector with the high inputs of all 16 channels tied together, the LOW inputs of all 16 channels tied together, and the AGND inputs tied together. The group of high inputs tied together will be called the *high side*; the group of low inputs tied together will be called the *low side*. An illustration of the test adapter is shown in Figure 2-4 on page 40.
7. **Test Software:** A test routine which repeatedly reads the ADC's results of 96 or more conversions, displays an average, and deviation spread is the preferred means of calibration. As shown in Table 3-1 on page 56, the ADC's results are located in the SRAM at relative addresses $10 through $2E. Lacking a software

routine of this caliber, a software routine which repeatedly displays the results of all 16 input conversions at a rate of 1 or 2 times per second is suggested. The user must then estimate the average.

Base Address Determination

With the VMICPCI-3322 16-Channel 16-bit Analog-to-Digital Converter (ADC) board installed in the CompactPCI™ Host System, using a protected-mode debugger or equivalent software for calibration, *find* where in the short I/O space the system BIOS has located the VMICPCI-3322 Base Address Register 1. The three parameters required to find the base addresses are the VENDOR ID ($114A) , the DEVICE ID ($3322), and the REV ID which is 0. Base Address Register 1 and the information in Table 3-1 on page 56 establishes the location of the CSR and SRAM locations which are necessary to operate this board. All addresses stated in the following sections are relative addresses in relation to the base address in the Base Address Register 1.



Male 37-Pin Test Adapter

Pinout	Signal	Pinout	Signal
20	AGND	1	AGND
21	CH0 L	2	CH0 H
22	CH1 L	3	CH1 H
23	CH2 L	4	CH2 H
24	CH3 L	5	CH3 H
25	CH4 L	6	CH4 H
26	CH5 L	7	CH5 H
27	CH6 L	8	CH6 H
28	CH7 L	9	CH7 H
29	CH8 L	10	CH8 H
30	CH9 L	11	CH9 H
31	CH10 L	12	CH10 H
32	CH11 L	13	CH11 H
33	CH12 L	14	CH12 H
34	CH13 L	15	CH13 H
35	CH14 L	16	CH14 H
36	CH15 L	17	CH15 H
37	AGND	18	N/C
		19	AGND

Figure 2-4 Male 37-PinTest Adapter

Note

This test adapter is used when calibration of the VMICPCI-3322 board is required, it is not supplied by VMIC and must be built by the user.

Calibration Procedures

The following sections provide calibration procedures for all the input voltage ranges of the VMICPCI-3322 16-Channel 16-bit Analog-to-Digital Converter (ADC) board. In the following procedures, the Fail LED Off bit is set to a logical (**1**) and the TWOCOMP bit is set to a logical (**0**), so the output format is offset or straight binary.

Refer to the following sections for the specific calibration procedure:

±10 V Input Range	Refer to *Calibration Procedure for ±10 V Input Range* section on page 42.
±5 V Input Range	Refer to *Calibration Procedure for ±5 V Input Range* section on page 44.
±2.5 V Input Range	Refer to *Calibration Procedure for ±2.5 V Input Range* section on page 45.
0 to 10 V Input Range	Refer to *Calibration Procedure for 0 to +10 V Input Range* section on page 47.
0 to 5 V Input Range	Refer to *Calibration Procedure for 0 to +5 V Input Range* section on page 49.

Calibration of the board to a specific range does not ensure the board shall remain calibrated if the jumpers are then reconfigured.

Calibration Procedure for ±10 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the ±10 V input range as shown in Table 2-2 on page 37.
2. Install the board in a CompactPCI host system, using the CompactPCI™ extender board if necessary.
3. Install the test adapter on the P1 input connector (see Figure 2-4 on page 40).
4. Apply power to the CompactPCI host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted-up and the test software routines may be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input channel 0 remains selected and enabled, through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP2(+) and TP1(-). (See Figure 2-2 on page 35.)
2. Adjust potentiometer R93 for a DMM reading of +10.0000 ±0.00015 VDC.

Common-Mode Adjustments:

Perform the following steps to adjust the Common-Mode Voltage:

1. Program the voltage source for 0.00000 VDC.
2. Connect both the high side and the low side of the test adapter to the (+) lead of the voltage source. Connect the (-) lead of the voltage source to the AGND inputs of the test adapter.

3. Connect the DMM (+) lead to jumper E1 pin 1 and connect the DMM (-) lead to jumper E2 pin 2.
4. Record the DMM reading while the voltage source remains at 0.00000 VDC.
5. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC and adjust potentiometer R87 to obtain the minimum variation in the DMM reading ±0.00005 VDC. Disconnect the DMM when finished.
6. Write $A000 to the CSR at relative address 0. (This sets the Fail LED off and sets SCANENA high.) Then start the software routine which repeatedly displays the averages off the 16 input conversions.
7. Set the voltage source to 0.00000 VDC, and record the average of the readings. The average should be a value close to $8000.
8. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC and adjust potentiometer R86 to obtain the minimum variation in the average of readings. Less than 1 LSB variation in the average reading should be attainable.

Offset Adjustment:

Perform the following steps to adjust the Offset:

1. Disconnect the voltage source from the test adapter. Tie all three of the input sides together. The high side, the low side, and the AGND test adapter inputs should be tied together using test clips.
2. Start the software routine, which repeatedly displays the average or results from all 16 inputs.
3. Adjust potentiometer R101 so that the average reading is $8000.
4. Remove the test clips that tie the test adapter inputs together.

Gain Adjustment:

Perform the following steps to adjust the Gain:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side input and the AGND inputs of the test adapter.
2. Set the voltage source to -9.99512 VDC.
3. Adjust potentiometer R92 so that the average reading is $000F.
4. Set the voltage source to +9.99511 VDC, and verify that the average reading is $FFF0 ±1.
5. Repeat the previous three steps until both averages are within the tolerance.
6. Remove the voltage source and the test adapter.
7. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for ±5 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the ±5 V input range as shown in Table 2-2 on page 37.
2. Install the board in a CompactPCI host system, using the CompactPCI extender board if necessary.
3. Install the test adapter onto the P1 input connector.
4. Apply power to the CompactPCI host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted-up and the test software routine can be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP2(+) and TP1(-). (See Figure 2-2 on page 35.)
2. Install jumper E3 between pins 2 and 3.
3. Adjust potentiometer R93 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper E3 between pins 1 and 2.
5. Adjust potentiometer R102 for a DMM reading of +4.99950 ±0.00005 VDC.

Common-Mode Adjustments:

Perform the following steps to adjust the Common-Mode Voltage:

1. Program the voltage source for 0.00000 VDC.
2. Connect the voltage source (+) lead to both the high and low sides of the test adapter. Connect the (-) lead of the voltage source to the AGND input of the test adapter.
3. Connect the DMM (+) lead to jumper E1 pin 1 and connect the DMM (-) lead to jumper E2 pin 2.
4. Record the DMM reading while the voltage source remains at 0.00000 VDC.
5. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC, adjust potentiometer R87 to obtain the minimum variation in the DMM readings ±0.00005 VDC. Disconnect the DMM when finished.
6. Write $A000 to the CSR at relative address 0. This sets the Fail LED off and sets SCANENA high. Then start the routine which repeatedly displays the averages off the 16 input conversions.
7. Set the voltage source to 0.00000 VDC, and record the average of the reading which results. The average should be a value close to $8000.

8. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC, adjust potentiometer R86 to obtain the minimum variation in the average readings. A variation in the average of ±1 LSB or less should be attainable.

Offset Adjustment:

Perform the following steps to adjust the Offset:

1. Disconnect the voltage source from the test adapter. Tie all three inputs together. The high side, the low side, and the AGND test adapter inputs should be tied together using test clips.
2. Start the software routine, which repeatedly displays the average or results from all 16 inputs.
3. Adjust potentiometer R101 so that the average reading is `$8000`.
4. Remove the test clips that ties the test adapter inputs together.

Gain Adjustment:

Perform the following steps to adjust the Gain:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side input and the AGND inputs of the test adapter.
2. Set the voltage source to -4.99756 VDC.
3. Adjust potentiometer R92 so that the average reading is $000F.
4. Set the voltage source to +4.99756 VDC and verify that the average reading is `$FFF0` ±1.
5. Repeat the previous three steps until both averages are within tolerance.
6. Remove the voltage source and the test adapter.
7. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for ±2.5 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the ±2.5 V input range as shown in Table 2-2 on page 37.
2. Install the board in a CompactPCI host system, using the CompactPCI extender board if necessary.
3. Install the test adapter onto the P1 input connector.
4. Apply power to the CompactPCI host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted up and the test software routine can be loaded.
5. Write `$4000` to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until `SCANENA` is enabled, input channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP2(+) and TP1(-). (See Figure 2-2 on page 35.)
2. Install jumper on E3, between pins 2 and 3.
3. Adjust potentiometer R93 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper on E3, between pins 1 and 2.
5. Adjust potentiometer R102 for a DMM reading of +4.99950 ±0.00005 VDC.

Common-Mode Adjustments:

Perform the following steps to adjust the Common-Mode Voltage:

1. Program the voltage source for 0.00000 VDC.
2. Temporarily remove jumpers E1 and E2.
3. Connect the (+) lead of the voltage source to both the high and low sides of the test adapter. Connect the (-) lead of the voltage source to the AGND input of the test adapter.
4. Connect the DMM (+) lead to the jumper E1 pin 1 and connect the DMM (-) lead to jumper E2 pin 2.
5. Record the DMM reading while the voltage source remains at 0.00000 VDC.
6. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC, adjust potentiometer R87 to obtain the minimum variation in the DMM reading ±0.00005 VDC. Disconnect the DMM when finished.
7. Re-install jumpers E1 and E2.
8. Write $A000 to the CSR at relative address 0. This sets the Fail LED off and sets SCANENA high. Start the software routine which repeatedly displays the average or the results of all 16 input conversions.
9. Set the voltage source to 0.00000 VDC and record the average results. The average should be a value close to $8000.
10. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC, adjust potentiometer R86 to obtain the minimum variation in the average readings. A variation in the average of ±1 LSB or less should be attainable.

Offset Adjustment:

Perform the following steps to adjust the Offset:

1. Disconnect the voltage source from the test adapter. On the test adapter, tie all three inputs together. The high side, the low side, and the AGND test adapter inputs should be tied together using test clips.
2. Start the software routine, which repeatedly displays the average or results from all 16 inputs.
3. Adjust potentiometer R101 so that the average reading is $8000.
4. Remove the test clips that tie the test adapter inputs together.

Gain Adjustment:

Perform the following steps to adjust the Gain:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side input and the AGND inputs of the test adapter.
2. Set the voltage source to -2.49878 VDC.
3. Adjust potentiometer R92 so that the average reading is $000F.
4. Set the voltage source to +2.49878 VDC and verify that the average reading is $FFF0 ±3.
5. Repeat the previous three steps until both averages are within the tolerance.
6. Remove the voltage source and the test adapter.
7. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for 0 to +10 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the 0 to +10 V input range as shown in Table 2-2 on page 37.
2. Install the board in a CompactPCI host system, using the CompactPCI extender board if necessary.
3. Connect the test adapter onto the P1 input connector.
4. Apply power to the CompactPCI host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system may be to booted up and the test software routine can be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input Channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP2(+) and TP1(-). (See Figure 2-2 on page 35.)
2. Install jumper E3, between pins 2 and 3.
3. Adjust potentiometer R93 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper E3, between pins 1 and 2.
5. Adjust potentiometer R102 for a DMM reading of +4.99950 ±0.00005 VDC.

Input Common-Mode Trim (R87):

Perform the following steps to adjust the Input Common-Mode Trim to its center value:

1. Rotate potentiometer R87 clockwise ten turns, this positions the potentiometer to its end value.
2. Rotate potentiometer R87 counterclockwise five turns, this will position the potentiometer to its center value

Output Common-Mode Trim (R86):

Perform the following steps to adjust the Output Common-Mode Trim to its center value:

1. Rotate potentiometer R86 clockwise ten turns, this positions the potentiometer to its end value.
2. Rotate potentiometer R86 counter-clockwise five turns, this will position the potentiometer to its center value.

ADC Adjustment:

Perform the following stepup for the ADC adjustment:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side and the AGND inputs of the test adapter.
2. Set the voltage source for +5.0000 VDC.
3. Start the sofeware routine, which repeatedly displays the average or results from all 16 inputs.
4. Adjust potentiometers R92 and R101 until the average reading is $8000 ±1.
5. Set the voltage source for +0.002441 VDC.
6. Adjust potentiometers R92 and R101 until the average reading is $000F ±1.
7. Set the voltage source for +9.99756 VDC.
8. Adjust potentiometers R92 and R101 until the average reading is FFF0 ±1.
9. Repeat the previous seven steps until all averages are within tolerance.
10. Remove the voltage source and the test adapter.

Calibration Procedure for 0 to +5 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the 0 to +5 V input range as shown in Table 2-2 on page 37.
2. Install the board in a CompactPCI host system, using the CompactPCI™ extender board if necessary.
3. Connect the test adapter to the P1 input connector.
4. Apply power to the CompactPCI host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted up, and the test software routine can be loaded.
5. Write `$4000` to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until `SCANENA` is enabled, input channel 0 remains selected and enabled through to the ADC input.

Input Common-Mode Adjustment (R87):

Perform the following steps to adjust the Input Common-Mode Trim to its center value:

1. Rotate potentiometer R87 clockwise ten turns, this position the potentiometer to its end value.
2. Rotate potentiometer R87 counterclockwise five turns, this will position the potentiometer to its center value.

Output Common-Mode Adjustments (R86):

Perform the following steps to adjust the Output Common-Mode Trim to its center value:

1. Rotate potentiometer R86 clockwise ten turns, this position the potentiometer to its end value.
2. Rotate potentiometer R86 counterclockwise five turns, this will position the potentiometer to its center value.

ADC Adjustment:

Perform the following steps for the ADC adjustment:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side and the `AGND` inputs of the test adapter.
2. Set the voltage source for +2.5000 VDC.
3. Start the software routine, which repeatedly displays the average or results from all 16 inputs.
4. Adjust potentiometer R101 so that the average reading is `$8000`.
5. Set the voltage source for +0.001221 VDC.

6. Adjust potentiometers R92 and R101 until the average reading is $000F ±1.
7. Set the voltage source for +4.99878 VDC.
8. Adjust potentiometers R92 and R101 until the average reading is $FFF0 ±1.
9. Repeat the pervious seven steps until all averages are within tolerance.
10. Remove the voltage source and the test adapter.

Connector Descriptions

The VMICPCI-3322 board has two connectors, P1 and J1. P1 is the external I/O connector and is located on the front panel. J1 is the CompactPCI card edge connector.

CompactPCI Connector (J1)

The CompactPCI motherboard plugs are keyed and the CompactPCI card edge connectors are keyed to ensure compatibility. The VMICPCI-3322 was designed for a 5 V, 32-bit CompactPCI bus system.

I/O Connector (P1)

The P1 connector is a 37-pin female D-shell subminiature receptacle. Figure 2-4 on page 40 details the signal/pin assignment, and Figure 2-5 on page 53 provides a view of the connector.

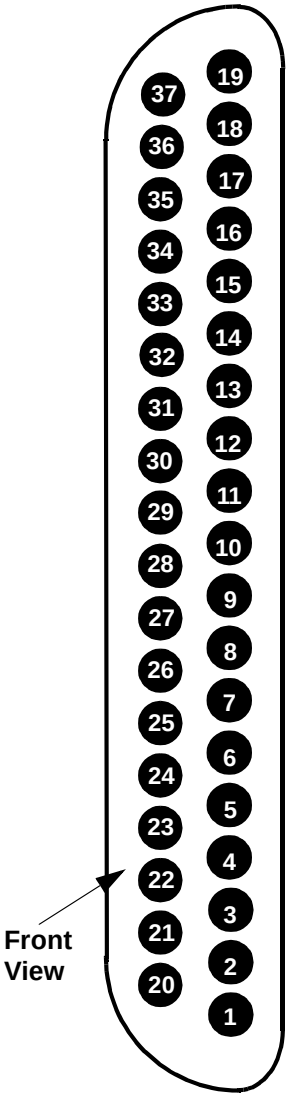
System Considerations

Input Filter Selection

As mentioned in the *Low Pass Filters* section on page 23, the VMICPCI-3322 board offers four factory-installed Low Pass Filter options, which are: no filter, 50 Hz., 100 Hz, and 500 Hz. Selection of the proper filter should be based on knowledge of the input signal characteristics and expected system noise. Selection of a lower frequency filter will increase the attenuation of high-frequency noise, but should also lower the maximum frequency of the signal that can be accurately converted.

Input Cables

Optimum performance is usually obtained if the input cables consist of individually twisted and shielded pairs. Short of individual shielded pairs, twisted pairs with a group or bundle shield is recommended. P1 pins 1, 19, 20, and 37 serve to tie cable shields to the board AGND as well as providing a ground reference for the external signal sources.



Female 37-Pin I/O Connector

Pinout	Signal	Pinout	Signal
37	AGND	19	AGND
36	CH15 L	18	N/C
35	CH14 L	17	CH15 H
34	CH13 L	16	CH14 H
33	CH12 L	15	CH13 H
32	CH11 L	14	CH12 H
31	CH10 L	13	CH11 H
30	CH9 L	12	CH10 H
29	CH8 L	11	CH9 H
28	CH7 L	10	CH8 H
27	CH6 L	9	CH7 H
26	CH5 L	8	CH6 H
25	CH4 L	7	CH5 H
24	CH3 L	6	CH4 H
23	CH2 L	5	CH3 H
22	CH1 L	4	CH2 H
21	CH0 L	3	CH1 H
20	AGND	2	CH0 H
		1	AGND

Figure 2-5 P1 I/O Connector

General Guidelines

The grounding scheme used can have a major affect on system performance. Each system has its own unique interface considerations, but the following general guidelines will apply in most cases.

Long Input Lines:

Long input lines (greater than 10 feet), or inputs from grounded sources (sources which are not floating), should be connected to differential inputs. The overall sheilds should be extended from the input source to as close to the board as possible. Single-ended inputs are susceptible to ground loop errors, and should be used only with high-level floating sources.

Source Impedance:

Use a signal source with the lowest available impedance. Susceptibiltiy to crosstalk and induced interference increases as the source impedance increases.

Floating Signal Sources:

The shield from a floating signal source (RTD, strain gauge, etc.,) should be connected to the LOW (negative) terminal at the source. For low-impedance sources, or for sources which are protected from interference fields, connect the board end of the sheild to analog return (AGND) at the board. For high-impedance sources, connect all shielded terminals of the source together, and leave the board ends of the shields open.

Grounded Signal Sources:

Outputs of grounded sources (sources which are not floating) must be referenced to a common ground, which ensures that the input voltage will not exceed the input range (±10 V) of the board. Shields from grounded sources should be connected to LOW terminal of the sources, and left open at the board.

Unused Inputs:

Unused inputs within each group of eight channels (0 through 7, 8 through 15) should be connected to a common ground to avoid interference with active channels. Grounding of unused groups of 8 channels is not essential, but will assist in minimizing susceptibility to system noise.

CHAPTER
3

Programming

Contents

Introduction

As described in the *Configuration and Installation* on page 31, one of the PCI bus configuration registers, the Base Address Register 1, contains the starting I/O address at which the VMICPCI-3322 16-Channel 16-bit Analog-to-Digital Converter (ADC) board's registers are located. Base Address Register 2 contains the starting memory mapped address. This address is assigned by the system BIOS during the boot process. Starting at the base address, the VMICPCI-3322 reserves the next 128 consecutive byte addresses. Of these addresses, only the even addresses are used due to 16-bit configuration of the VMICPCI-3322. The first eight even addresses, `$0` through `$E`, access the CSR. The next 32 even addresses, `$10` through `$4E`, access the SRAM. The remaining addresses, `$50` through `$7F`, are reserved. Table 3-1 on page 56 details the VMICPCI-3322's memory map.

Table 3-1 VMICPCI-3322 Board's Memory Map

Relative Address (HEX)	Function	Access
00 through 0E	Control and Status (CSR)	Read / Write
10	SRAM Location 0 (Analog Input Channel 0 Data)	Read / Write
12	SRAM Location 1 (Analog Input Channel 1 Data)	Read / Write
14	SRAM Location 2 (Analog Input Channel 2 Data)	Read / Write
16	SRAM Location 3 (Analog Input Channel 3 Data)	Read / Write
18	SRAM Location 4 (Analog Input Channel 4 Data)	Read / Write
1A	SRAM Location 5 (Analog Input Channel 5 Data)	Read / Write
1C	SRAM Location 6 (Analog Input Channel 6 Data)	Read / Write
1E	SRAM Location 7 (Analog Input Channel 7 Data)	Read / Write
20	SRAM Location 8 (Analog Input Channel 8 Data)	Read / Write
22	SRAM Location 9 (Analog Input Channel 9 Data)	Read / Write
24	SRAM Location 10 (Analog Input Channel 10 Data)	Read / Write
26	SRAM Location 11 (Analog Input Channel 11 Data)	Read / Write
28	SRAM Location 12 (Analog Input Channel 12 Data)	Read / Write
2A	SRAM Location 13 (Analog Input Channel 13 Data)	Read / Write
2C	SRAM Location 14 (Analog Input Channel 14 Data)	Read / Write
2E	SRAM Location 15 (Analog Input Channel 15 Data)	Read / Write
30-4E	SRAM Location 16 through 31 (Spare)	Read / Write
50 through 7E	Reserved	Read / Write

Control and Status Register Description

Control Register Bit Assignments

Eleven of the sixteen possible data bits in the Control Register have assigned functions. Those functions are detailed in Table 3-2 below:

Table 3-2 Control Register Bit Map

Control Register (Offset 00 through 0E) Write Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED_OFF	SOFT_RST	SCANENA	TWOCOMP	Reserved	POLLENA	SCANSIZ0	Reserved

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved				PB3	PB2	PB1	PB0

Control Register Bit Definitions

Bit 15 **LED_OFF:** The **Fail LED** is mounted on the VMICPCI-3322's front panel. The LED is turned ON by writing a logical zero (0); the user can extinguish the LED by writing a logical one (1) to this bit.

Bit 14 **SOFT_RST:** The **Software Reset**, resets all sections of the timing and control EPLD, including the CSR itself. The Software Reset is immediate and will interrupt any current autoscan cycle. The reset duration lasts 60 ns and an ADC calibration cycle occurs following the reset. After the Software Reset, the ADC performs a self-calibration which takes approximately 41 ms. Set this bit to a one (1) to initiate a software reset. The SRAM is not affected by a software reset, and is initialized, if necessary, by PCI write cycles.

Bit 13 **SCANENA:** Upon any reset the **SCANENA** bit is low and the autoscan cycle is disabled. Once the SCANENA bit is set, the board autoscans sequentially and repeatedly through the selected number of channels starting with Channel 0. If the autoscan is in process and the SCANENA bit is set low, the board completes the current ADC conversion and then stops.

Note

The **SCANENA** and the **POLLENA** bits in the CSR should never be written HIGH at the same time. Writing both of these bits HIGH simultaneously will produce an inoperable condition for the VMICPCI-3322.

Bit 12 **TWOCOMP:** The **TWOCOMP Control Bit** affects the state of the most significant data bit, D15, as it is being copied from the ADC data output into the SRAM. The output of the ADC itself assumes a two's complement convention. If the TWOCOMP bit is set high, the D15 bit is written unchanged into the SRAM; otherwise, D15 is inverted and the data is considered straight or offset binary.

Bit 11 **Reserved:** This bit is reserved for future expansion, write to zero.

Bit 10 **POLLENA:** When set, this bit enables the POLL MODE on the VMICPCI-3322. POLL MODE allows the user to continually sample any one of the sixteen analog input channels, using the Poll Bits 3..0 (PB), convert the value, and store that value in SRAM.

The POLLENA and the SCANENA bits in the CSR should never be written HIGH at the same time. Writing both of these bits HIGH simultaneously will produce an inoperable condition for the VMICPCI-3322.

Bit 9 **SCANSIZ0:** The SCANSIZ0 bit selects the number of inputs to scan and digitize. The sections are 16 or 8 channels. With any selection, the scan starts with Channel 0, sequences up the channels until the selected number is reached, and then repeats starting at Channel 0. It is recommended that the SCANSIZ0 bit be changed only while the scan cycle is disabled.

The definition of the SCANSIZ0 bit is detailed in Table 3-3 below:

Table 3-3 SCANSIZ0 Bit Definitions

SCANSIZ0	Channels Scanned
0	0 through 15
1	0 through 7

Bits 8 through 4 **Reserved:** These bits are reserved for future expansion, write to zero.

Bits 3 through 0 PB3..0:

These four bits allow the user to select which channel is to be repeatedly sampled and stored during the POLL MODE. The following table correlates the PB bits to each input channel.

Table 3-4 PBx Bit Definitions

PB3	PB2	PB1	PB0	Input Channel
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Status Bit Assignments

All 16 data bits of the status word are defined as either true status or a fixed state. The bit descriptions are detailed below:

Table 3-5 Status Register's Bit Map

Control Register (Offset 00 through 0E) Write Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED_OFF	SOFT_RST	SCANENA	TWOCOMP	TEST1	POLLENA	SCANSIZ0	CALBUSY

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved				PB3	PB2	PB1	PB0

Status Register Bit Definitions

Bit 15 **LED_OFF:** Indicate the status of their respective control register bits.

Bits 14-09 **See Control Register Bit Definitions**

Bit 8 **CALBUSY** High while the ADC is in calibration mode.

Bits 07-04 **Reserved:** These bits are reserved for future use and will be read back as zero (0).

Bits 03-00 **PB03-00:** These four bits indicated the status of their respective control register bits.

ADC Data Formats

The convention for the ADC data represents the most significant bit as D15 and the least significant bit as D0. If the TWOCOMP bit in the CSR is a one, the coding is termed two's complement. If the TWOCOMP bit is zero, the coding is termed straight binary for unipolar ranges and offset binary for bipolar ranges. Table 3-6 below details the relationship of the input voltage to ADC output format for 0 to +10 V and ±10 V ranges. The other ranges have a similar relationship. The Equation for determining the Transfer Function is as follows:

$E_{IN} = E_{LO} + [E_{FSR} \times (N_{ADC} / 65{,}536)]$

Where: E_{IN} =Input Voltage
E_{LO} =Lower End of Input Range
E_{FSR} =Full-Scale Input Range
N_{ADC} =A / D Converter Reading

Table 3-6 ADC Data Formats

Range: Unipolar, 0 to +10 V Output: Straight Binary		
Fraction of Scale	**Equivalent Input Voltage**	**D15.....D0**
Full-Scale	+9.99985 V	1111 1111 1111 1111
Half-Scale	+5.00000 V	1000 0000 0000 0000
Zero Scale	+0.00000 V	0000 0000 0000 0000

Range: Bipolar, -10 to +10 V Output: Offset Binary		
Fraction of Scale	**Equivalent Input Voltage**	**D15.....D0**
+Full-Scale	+9.99969 V	1111 1111 1111 1111
+Half-Scale	+5.00000 V	1100 0000 0000 0000
Zero Scale	+0.00000 V	1000 0000 0000 0000
-Half-Scale	-5.00000 V	0100 0000 0000 0000
-Full-Scale	-10.0000 V	0000 0000 0000 0000

Range: Bipolar, -10 to +10 V Output: Two's Complement		
Fraction of Scale	**Equivalent Input Voltage**	**D15.....D0**
+Full-Scale	+9.99969 V	0111 1111 1111 1111
+Half-Scale	+5.00000 V	0100 0000 0000 0000
Zero Scale	+0.00000 V	0000 0000 0000 0000
-Half-Scale	-5.00000 V	1100 0000 0000 0000
-Full-Scale	-10.0000 V	1000 0000 0000 0000

LSB Bit Weights and Specific Ranges

When describing the input ranges, they are often rounded off for simplicity. Table 3-7 lists the LSB weights and the specific input range that results.

Table 3-7 LSB Bit Weights and Specific Ranges

Input Range	LSB Weight	+Full-Scale (V)	+Half-Scale (V)	Zero Scale (V)	-Half-Scale (V)	-Full-Scale (V)
0 to +5 V	76.2939 µV	+4.99992	+2.50000	0.0	-----	-----
±2.5 V	76.2939 µV	+2.49992	+1.25000	0.0	-1.25000	-2.50000
0 to +10 V	152.588 µV	+9.99985	+5.00000	0.0	-----	-----
±5 V	152.588 µV	+4.99985	+2.50000	0.0	-2.50000	-5.00000
±10	305.176 µV	+9.99969	+5.00000	0.0	-5.00000	-10.00000

Input Frequency Range

If the optional low pass input filters are present, they will dictate the upper frequency limit of the signal that can accurately be converted. Note that the signal's upper frequency limit should be well below the corner frequency of the filters. At the corner frequency, the amplitude of the signal is attenuated to 70.7 percent of its original amplitude. One least significant bit (LSB) of 16-bit conversion is equivalent to approximately 0.001526 percent of full-scale.

If no input filters are present, the input frequency range is limited by either the sample rate or the frequency response of the board amplifiers. A basic rule of analog sampling, called the Nyquist limit, states that the frequency of a signal should not exceed one half the sample rate. Although the VMICPCI-3322 converts at an aggregate rate of one channel every 10.05 µs (or 99.5 kHz), the rate at which each channel is repeatedly sampled is actually 99.5 kHz divided by the number of channels sampled.

The primary reason the VMICPCI-3322 offers a selection in the number of channels scanned per cycle is to improve frequency response. The user can sample higher frequency signals by limiting the number of channels used. Table 3-8 details the frequency range for the two selections in channels scanned.

Table 3-8 Input Frequency Verus Channels Scanned

Channels Used	Channel Sample Rate	Input Frequency Limit	Reason
0 through 15	6.219 kHz	3.109 kHz	Nyquist Limit
0 through 7	12.430 kHz	6.219 kHz	Nyquist Limit
For a Single Channel	99.5 kHz	49.75 kHz	Nyquist Limit

Maintenance

Maintenance

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

1. Software
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components of adjacent boards are disturbed when inserting or removing the board from the CompactPCI™ system chasis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Maintenance Prints

User-level repairs are not recommended.