VMICPCI-4320
CompactPCI 8-Channel Analog Output Board

Product Manual

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500-654320-000 Rev. B

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Overview

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Introduction

The VMICPCI-4320 CompactPCI Analog Output board provides eight high-quality output channels. Five jumper-selectable voltage ranges. With 12-bit resolution supplied by a Digital-to-Analog Converter (DAC). An on-board DC-to-DC Converter is used to supply ±15 V. A functional block diagram of the VMICPCI-4320 is shown in Figure 1 on page 13.

The following brief overview of principal features illustrates the flexibility and the performance available with the VMICPCI-4320 board:

- Eight analog output channels
- 12-bit DAC resolution
- Jumper-selectable voltage ranges
- Output voltage ranges of 0 to +5, 0 to +10, ±2.5, ±5, and ±10 VDC
- On-board DC-to-DC Converter
- Complies with PCI Local bus specification
- Standard 3U form factor with optional 6U front panel
- Front panel Fail LED indicator for initial verification
- Front panel outputs on P1 (female 37-pin D-shell subminiature connector)
- Sixteen SRAM locations with eight as spares

Functional Description

The VMICPCI-4320 is a CompactPCI 8-channel, 12-bit analog output board. The eight channels are user programmable with eight 12-bit Synchronous Random Access Memory (SRAM) locations. Each SRAM location corresponds to an output channel. The VMICPCI-4320 periodically fetches the 12-bit binary values stored in the SRAM and uses the values as the inputs to the on-board Digital-to-Analog Converter (DAC). The output of the DAC is distributed to the sample-and-hold circuits associated with each output channel. The board has a refresh rate of 1.2626 Hz, and provides settling to 0.01 percent for stepped outputs at each update. The maximum settling time to 1 Least Significant Bit (LSB) is 792 µs.

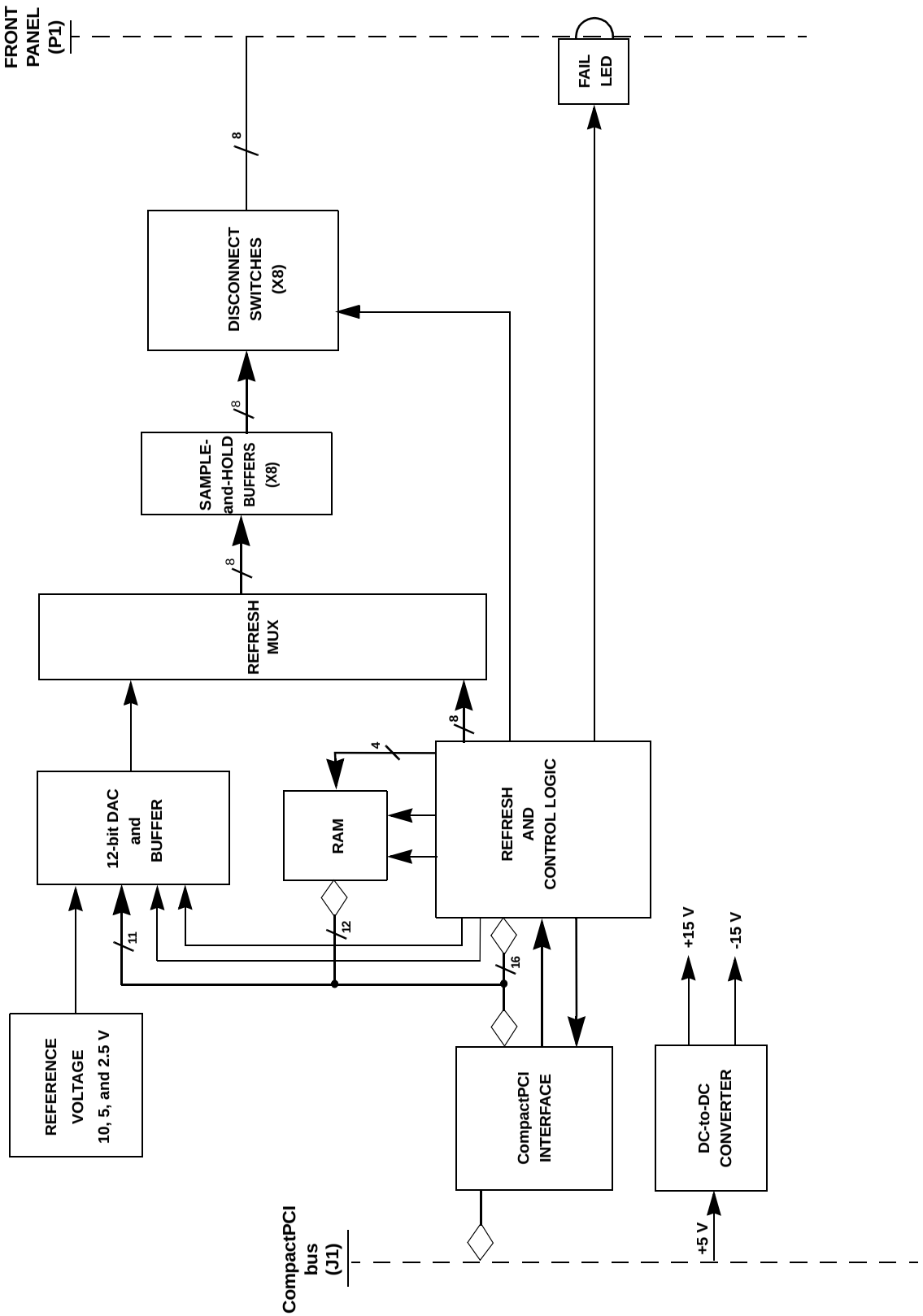


Figure 1 VMICPCI-4320 8-Channel CompactPCI bus Analog Output Board Functional Block Diagram

Related Documents

For a detailed explanation of the CompactPCI local bus and its characteristics, refer to the *PCI Local Bus Specification v2.1* from:

PCI Local Bus Specification, Revision 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)

For a detailed explanation of the CompactPCI bus and its characteristics, refer to the *CompactPCI Specification, 2.0 R2.1* from:

PCI Industrial Manufacturers Group
(PICMG)
301 Edgewater Place
Suite 220
Wakefield, MA 01880 USA
(617) 224-1100
(503) 797-4207 (International)
Fax: (617) 224-1239
Web: www.PICMG.ORG

Intended Audience

Knowledge of CompactPCI bus protocol is assumed. Additionally, the user should be familiar with standard network protocols and configuration of a shared memory interface.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

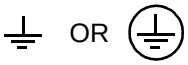
Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

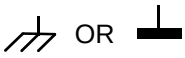
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



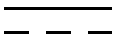
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

STOP STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING WARNING denotes a hazard. It calls attention to a procedure, a practice, or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION CAUTION denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE NOTE highlights important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER
1

Theory of Operation

Contents

Introduction

The VMICPCI-4320 CompactPCI 8-Channel, 12-bit Analog Output board is designed to operate in systems supporting the 5 V PCI Local bus interface.

For the purpose of discussion, the VMICPCI-4320 can be divided into two major blocks; the PCI bus Interface, and the Digital-to-Analog circuitry. The Digital-to-Analog circuitry is further divided into the following sections:

- Data storage
- DAC and analog multiplexer
- Analog output buffers and switches
- Analog output refresh logic

PCI bus Interface

The VMICPCI-4320 board is implemented with a PCI bus-compliant interface device, allowing it to operate as a PCI bus target. The VMICPCI-4320 supports standard PCI bus configuration capabilities.

PCI bus Configuration Registers

Each PCI bus device contains a predefined group of Configuration Registers. This group of registers implements the primary PCI bus functions of identification, PCI bus command and status, and board configuration. Several of the standard registers, though present in the PCI bus interface device, do not apply to the VMICPCI-4320 board. However, registers that do apply are listed in Table 1-1 below. Also reference Figure 3-1 on page 42.

Table 1-1 PCI Configuration Registers

Configuration Address Offset	Abbreviation	Register Name	VMICPCI-4320	Type
$00 to $01	VID	Vendor Identification	$114A	Read-Only
$02 to $03	DID	Device Identification	$4320	Read-Only
$04 to $05	PCICMD	PCI Command Register	$E000	Read / Write
$06 to $07	PCISTS	PCI Status Register	varies	Read / Write to Clear
$08	RID	Revision ID Register	$80	Read-Only
$09 to $0B	CLCD	Class Code Register	$FF00	Read-Only
$10 to $13	BADR0	Base Address Register 0	varies	Read / Write
$14 to $17	BADR1	Base Address Register 1 (I / O)	varies	Read / Write
$18 to $21	BADR2	Base Address Register 2 (Memory)	varies	Read / Write

PCI bus Operation Registers

Base Address Register 0 (BADR0) contains a 32-bit address pointing to a second group of 16 DWORD (32-bit) registers. These registers are called the PCI bus Operation Registers and could or could not be involved in VMICPCI-4320 operations.

VMICPCI-4320 Function Registers

Two of the PCI bus Configuration Registers referred to as Base Address Register 1(BADR1) and Base Address Register 2 (BADR2) contain a 32-bit address. This is the base addresses of the registers that are applicable to the VMICPCI-4320. Two groups of 64-byte addresses are dedicated to these functions. Of the 64-byte addresses, only the 32 even addresses are used since all VMICPCI-4320 function-specific registers reside on a 16-bit boundary. The first eight even byte addresses with offsets $0 through $E are used to access the Control and Status Register (CSR). The next 16 even addresses with offsets $10 through $2E are used to access the 16 SRAM locations. The first set of eight SRAM locations store the digital values representing the eight analog outputs. The second set of eight SRAM locations are spares. All other byte address offsets ($30 through $3F) are reserved. See Table 3-1 on page 42 for all SRAM-related address offsets.

Digital-to-Analog Circuitry

The VMICPCI-4320 board can be divided into the following blocks:

- Refresh and control circuit
- SRAM data registers
- 12-bit Digital-to-Analog Converter (DAC)
- Eight-channel analog multiplexer
- Eight sample-and-hold buffers
- Eight disconnect switches
- Eight corresponding output pins on the P1 connector

Selection of the voltage output ranges are performed through a series of user-configurable jumpers on the board.

A periodic refresh cycle consists of several events:

1. A 12-bit value is read from the appropriate location in SRAM. With all channels of the analog multiplexer open, the SRAM data is written into the DAC, which in turn slews and settles to the new value.
2. Once the DAC output is fully settled, the analog multiplexer gates the output of the DAC to the appropriate sample-and-hold buffer.
3. After an additional settling time, the analog multiplexer is again opened, a channel counter is incremented and the cycle is repeated for the next channel.

In voltage output mode, the output of the sample-and-hold buffers pass through disconnect switches directly to the output connector P1.

Digital-to-Analog Converter (DAC) Circuit

A single 12-bit DAC services all eight outputs. This circuit contains a precision reference voltage that is jumper-selectable as either 2.5, 5, or a 10 V output. In addition, this circuit contains a buffered amplifier with a gain of two and is jumper-selectable for either bipolar or unipolar operations. The jumper configuration sets the available voltage output ranges. All eight channels will have the same range. Range is not selectable on a channel by channel basis.

Analog Multiplexer

The analog multiplexer consists of eight independent analog switches, which are enabled one at a time by the refresh and control circuitry.

Sample-and-Hold Buffers

Each sample-and-hold buffer consisted of a storage capacitor and a low leakage operational amplifier. Each amplifier can supply ±10 mA of current over the full-scale range of ±10 V and can withstand sustained short circuits to ground.

Disconnect Switches

A low resistance, solid state switched network follows each of the sample-and-hold buffers. The switches disconnect the buffers from the P1 outputs. All eight disconnect switches are controlled by a single bit in the CSR. Upon reset, the disconnect switches assume the open state and must be enabled by setting the appropriate bit in the CSR to a logical one (1). See the Control and Status Register bit 09 in the Programming section.

A second analog switch, switches the feedback of the amplifier from the source or load side of the output switch to compensate for voltage drops. Clamping diodes protect the buffers and switches from line transients by shunting voltages above ±15 V to the power supply rails.

Output Refresh Control

The VMICPCI-4320 contains 16 SRAM locations; each location is 12 bits wide. All 16 locations can be both written and read by the CompactPCI bus. However, only the first eight locations correspond to the eight analog outputs. Each CompactPCI bus SRAM access takes approximately 330 ns.

Each channel refresh cycle takes 99.0 µs to complete. To refresh all eight output channels, multiply 8 x 99.0 µs for a value of 792 µs. Therefore, each output is refreshed once every 792 µs. See Figure 1-1 on page 21 for a flowchart of the refresh cycle.

At the beginning of each 99.0 µs refresh cycle, the refresh control circuit reads the SRAM for a period of 450 ns. In the event that both the CompactPCI bus and refresh control circuit attempt to access the SRAM at the same time, an arbitration circuit halts the latter of the two until the first access is finished. If the CompactPCI bus access is the latter, the delay may cause the access to exceed the maximum 16 CompactPCI bus clock cycles. In this event, the CompactPCI bus interface device will issue a Target Requested Retry and the CompactPCI bus master completes the access. Regardless of whether an SRAM access collision occurs or not, each refresh cycle remains 99.0 µs.

Example:

Each refresh cycle (792 µs) consist of:

Read CH 0 SRAM
Write SRAM data to DAC
Switch multiplexer to CH 0

.

.

.

.

.

Read CH 7 SRAM
Write SRAM data to DAC
Switch multiplexer to CH 7

Built-in Power Converter

Power for the VMICPCI-4320 analog circuitry is supplied by a DC-to-DC Converter. 5 Volts received from the CompactPCI bus is regulated and isolated to ±15 VDC. The load current on the +15 V is approximately 260 mA, while the load current on the -15 V is approximately 130 mA.

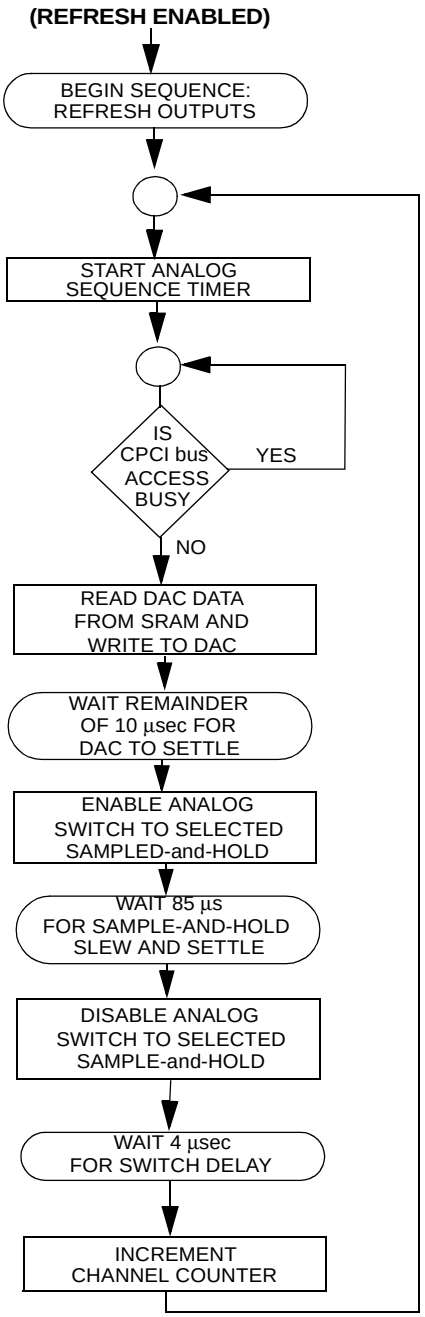


Figure 1-1 Refresh Cycle Timing Diagram

CHAPTER 2

Configuration and Installation

Contents

Introduction

The VMICPCI-4320 provides eight high-quality analog output channels, 12-bit resolution with an on-board DC-to-DC converter.

Data for each analog output channel is written directly into an on-board SRAM location. The data is periodically retrieved from SRAM and converted to an analog voltage which is transferred to one of the eight output sample-and-hold output buffers.

The board is designed with on-board memory that can be tested by executing a memory diagnostic test for operational verification. The Fail LED located on the front panel of the board gives the user an initial verification when installing the board. If an error condition occurs during diagnostic testing, a software-controlled LED is illuminated visually indicating a failure. The LED is illuminated by a system reset at power up and is extinguished by the user upon successful execution of the diagnostic test. The Fail LED is for user defined purposes only, and can be used for whatever purpose the user desires.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that may have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. This board can be installed in any slot position with a circle above the backplane. The slot with the triangle above the backplane is reserved for the system controller.

This symbol identifies the System Controller slot.

This symbol identifies the slot in which the VMICPCI-4320 can be installed.

CAUTION: Do not install or remove the board while power is applied.

Installing the VMICPCI-4320

Perform the following steps for installation:

1. Prior to installing the board, verify that jumpers are configured (for the desired output voltage), jumpers are described in the Configuration and Installation section under '*Jumper Installation on page 26*'.
2. Remove the blank panel corresponding to the CompactPCI slot that the VMICPCI-4320 is going to be installed.
3. CompactPCI systems can conform to one of several standards based on either 5 or 3.3 V operation, with a 32- or a 64-bit CompactPCI bus. The VMICPCI-4320 board is designed for a 5 V, 32-bit CompactPCI system. However, it is also compatible with a 5 V, 64-bit CompactPCI system as well. Refer to the host system documentation for information on compatible CompactPCI card types. The CompactPCI slots are keyed and the CompactPCI bus connectors are keyed to ensure compatibility. Examine the CompactPCI slot where the VMICPCI-4320 is to be installed. Verify that the location of the key in the CompactPCI slot corresponds to the key in the connector.
4. Insert the VMICPCI-4320 card into the desired CompactPCI slot until firmly mated with the connector. Tighten the hold-down screw to secure the board.

Operational Configuration

The I/O and/or memory address space used to operate the VMICPCI-4320 board is assigned dynamically by the system BIOS and is not jumper configurable. The VMICPCI-4320 board has two jumpers that define the output type(s) and voltage range(s).

Jumper Installation

The board is configured at the factory with a default jumper arrangement. The jumpers settings are shown in the figure below.

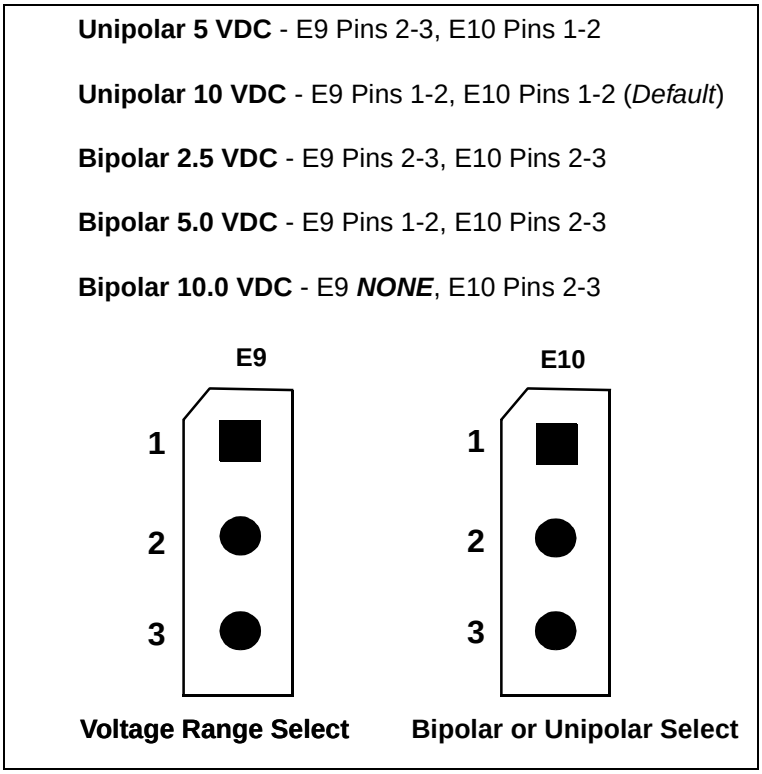


Figure 2-1 Configuring Jumpers for Output Types and Voltage Ranges

Analog Voltage Output Mode

Output Voltage Range

The output voltage range is jumper selectable (jumper E9). The maximum full-scale range is 20 V. To change the full-scale range, configure jumper E9 as indicated in Figure 2-1 above.

Bipolar or Unipolar Operation

Bipolar or Unipolar operation of the analog voltage outputs is selected using jumper E10, as shown in Figure 2-1 above.

Calibration

The VMICPCI-4320 board is calibrated for unipolar 10 VDC (factory default). If recalibration is required, perform the appropriate procedures for the desired voltage range. When calibrating the board you must determine the Base Address (see *'Base Address Determination'*). To calibrated the VMICPCI-4320 you will need test equipment outlined in *'Equipment Required'* below. The location of potentiometers and test points are shown in Figure 2-2 on page 28. Adjustment potentiometers and their functions are listed in Table 2-1.

Table 2-1 Potentiometer Adjustments

VOLTAGE ADJUSTMENTS	
POTENTIOMETER	**FUNCTION**
R27	Bipolar Outputs Zero Adjustment
R35	Unipolar Outputs Zero Adjustment
R32	Voltage Output Gain Adjustment
TP1	DAC Output
TP2	DAC Return

Equipment Required

The following is a list of equipment need for calibration:

1. **Digital Multimeter (DMM):** ±1.0000 and ±10.000 VDC ranges; voltage measurement accuracy of ±0.005 percent, 10 MΩ minimum input impedance, and current measurements at 1 µA resolution; five or more digits.
2. **CompactPCI Host System:** The CompactPCI host system required, as a minimum:
   - One open CompactPCI slot that supports a 3U, 5 V, 32-bit CompactPCI board
   - One 3.5-inch floppy disk drive plus interface
   - Monitor and keyboard
   - Power supply
3. **CompactPCI Extender Board:** Depending on the arrangement of the CompactPCI host system, it may be necessary to use a CompactPCI extender board to ensure access to the adjustment potentiometers and test points.
4. **Test Cables:** Test cables for the equipment listed above.

Base Address Determination

With the VMICPCI-4320 board installed in the CompactPCI host system running a protected-mode debugger or equivalent software, the user must determine where in I/O and memory space the system BIOS has located the Base Address Registers. There are three parameters to determine the base address of the VMICPCI-4320:

- VENDOR ID ($114A)
- DEVICE ID ($4320)
- REV ID ($C0)

Using the Base Address Registers along with information provided in the *Programming* Section (Chapter 3), establish the locations of the Control and Status Register and SRAM registers, these registers are used to operate the VMICPCI-4320.

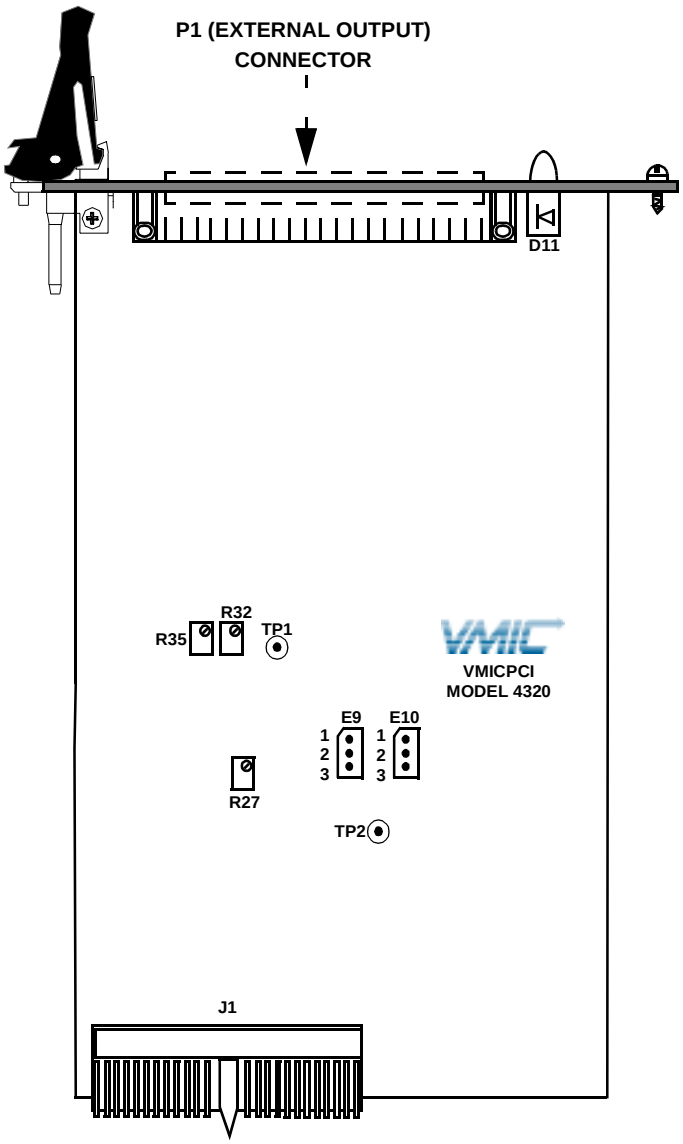


Figure 2-2 Location of Jumpers, Potentiometers, and Test Points

Calibration Procedures

The following is a list of the calibration procedures for the voltage ranges available on the VMICPCI-4320. The calibration procedures are based on the assumption that all jumpers have been configured for the desired voltage range and output mode. During the calibration procedures, the Fail LED off bit (bit 11 of the Control Register) is set to a one (1), and the TWO'S COMP bit (bit 10 of the Control Register) is set to a zero (0).

Refer to the following sections for the specific calibration procedure:

0 to 10 V output range	Refer to *"Calibration Procedure for 0 to 10 V Output Range"* on page 30.
0 to 5 V output range	Refer to *"Calibration Procedure for 0 to 5 V Output Range"* on page 31.
±2.5 V output range	Refer to *"Calibration Procedure for ±2.5 V Output Range"* on page 32.
±5 V output range	Refer to *"Calibration Procedure for ±5.0 V Output Range"* on page 33.
±10 V output range	Refer to *"Calibration Procedure for ±10.0 V Output Range"* on page 34.

NOTE: Recalibration of the outputs must be performed if the jumpers are reconfigured.

NOTE: Word or 16-bit writes to the SRAM does not store the four Most Significant Bits (MSB.) This is due to the fact that the on-board Digital-to-Analog Converter (DAC) only uses 12 bits of data input.

Calibration Procedure for 0 to 10 V Output Range

Setup:

Perform the following steps to initialize the setup:

1. Configure jumper E9 (pins 1 and 2) for the 10 V span, and jumper E10 (pins 1 and 2) for unipolar as shown in Figure 2-1 on page 26.
2. Install the board in a CompactPCI host system using the CompactPCI extender board.
3. Connect the DMM positive (+) lead to pin 1 of the P1 connector (CHOUT0), the output of the sample-and-hold buffer for channel 0. Connect the DMM negative (-) lead to pin 20 of the P1 connector (AGND). Reference Table 2-3 on page 36 for the P1 connector pinout.

NOTE: The P1 connector pins 20 through 35 are local ground reference points.

4. Turn power ON to the CompactPCI host system.

DAC Output Adjustments:

Perform the following steps to adjust the DAC output voltage:

1. Write $0A80 to the CSR at relative address 0. This configures the board for the FAIL LED off, straight binary format and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting. See *Programming* (Chapter 3) for the SRAM relative address.
3. Write $0 to channel 1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to channel 1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +9.9976 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustments (steps 3 and 4); therefore, repeat steps 1 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to the remaining output channels pins. The DMM should read +4.9988 ±0.0010 VDC for all channels. See Table 2-3 on page 36 (P1 connector pinout) for the location of the output channel pins 0 through 7.

Calibration for the 0 to 10 V output range has been completed. Remove power and all test connections. Remove the board from the extender card and installed the board in a CompactPCI host system.

Calibration Procedure for 0 to 5 V Output Range

Setup:

Perform the following steps to initialize the setup:

1. Configure jumper E9 (pins 2 and 3) for a 5 V span, and jumper E10 (pins 1 and 2) for the unipolar mode as described in Figure 2-1 on page 26.
2. Install board in a CompactPCI host system using the CompactPCI extender board.
3. Connect the DMM positive (+) lead to pin 1 of the P1 connector (CHOUT0), the output of the sample-and-hold buffer for channel 0. Connect the DMM negative (-) lead to pin 20 of the P1 connector (AGND). See Table 2-3 on page 36 for the location of the P1 connector pinout.

NOTE: The P1 connector pins 20 through 35 are local ground reference points.

4. Turn power ON to the CompactPCI host system.

DAC Output Adjustments:

Perform the following steps to adjust the DAC output voltage:

1. Write $0A80 to the CSR at relative address 0. This configures the boards for the Fail LED off, straight binary format with voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM channel locations. This sets all outputs to the mid-scale setting.
3. Write $0 to channel 1 SRAM location at relative address $12. See *Programming* (Chapter 3) for the SRAM relative addresses.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to channel 1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +4.9988 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4); therefore, repeat steps 1 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to each of the remaining channel pins (pins 2 through 8). The DMM should read +2.4994 ±0.0010 VDC for all channels.

Calibration for the 0 to 5 V output range has been completed. Remove power and all test connections. Remove the board from the extender card and installed the board in a CompactPCI host system.

Calibration Procedure for ±2.5 V Output Range

Setup:

Perform the following steps to initialize the setup:

1. Configure jumper E9 (pins 2 and 3) for a 5 V span, and jumper E10 (pins 2 and 3) for bipolar as shown in Figure 2-1 on page 26.
2. Install the board into a CompactPCI host system using the CompactPCI extender board.
3. Connect the DMM positive (+) lead to pin 1 of the P1 connector (CHOUT0), the output of the sample-and-hold buffer for channel 0. Connect the DMM negative (-) lead to pin 20 of the P1 connector (AGND). See Table 2-3 on page 36 for the P1 connector pinout.

NOTE: The P1 connector pins 20 through 35 are local ground reference points.

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4. Turn the power ON to the CompactPCI host system.

DAC Output Adjustments:

Perform the following steps to adjust the DAC output voltage:

1. Write $0A80 to the CSR at relative address 0. This configures the boards for the Fail LED off, straight binary format, and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM channel locations. This sets all outputs to the mid-scale setting.
3. Adjust potentiometer R27 for a DMM reading of 0.000 ±0.0010 VDC.
4. Write $0FFF to channel 1 SRAM location at relative address $12.
5. Adjust potentiometer R32 for a DMM reading of +2.4988 ±0.0010 VDC.
6. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4), therefore, repeat steps 1 through 6 as many times as required.
7. To verify that all channels are operational, sequentially move the DMM positive (+) lead to each of the remaining output channel pins (pins 2 through 8). The DMM should read +0.0000 ±0.0010 VDC for all channels.

Calibration for the ±2.5 V output range has been completed. Remove power and all test connections. Remove the board from the extender card and installed the board in a CompactPCI host system.

Calibration Procedure for ±5.0 V Output Range

Setup:

Perform the following steps to initialize the setup:

1. Configure jumper E9 (pins 1 and 2) for a 10 V span, and jumper E10 (pins 2 and 3) for bipolar as shown in Figure 2-1 on page 26.
2. Install the board into a CompactPCI host system using the CompactPCI extender board.
3. Connect the DMM positive (+) lead to pin 1 of the P1 connector (CHOUT0), the output of the sample-and-hold buffer for channel 0. Connect the DMM negative (-) lead to pin 20 of the P1 connector (AGND). See Table 2-3 on page 36 for the P1 connector pinout.

NOTE: The P1 connector pins 20 through 35 are local ground reference points.

4. Turn the power ON to the CompactPCI host system.

DAC Output Adjustments:

Perform the following steps to adjust the DAC output voltage:

1. Write $0A80 to the CSR at relative address 0. This configures the board for the Fail LED off, straight binary format and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM channel locations. This sets all outputs to the mid-scale setting.
3. Adjust potentiometer R27 for a DMM reading of 0.000 ±0.0010 VDC.
4. Write $0FFF to channel 1 SRAM location at relative address $12.
5. Adjust potentiometer R32 for a DMM reading of +4.9976 ±0.0010 VDC.
6. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4), therefore, repeat steps 1 through 6 as many times as required.
7. To verify that all channels are operational, sequentially move the DMM positive (+) lead to each of the remaining output channel pins (pins 2 through 8). The DMM should read +0.0000 ±0.0010 VDC for all channels.

Calibration for the ±5.0 V output range has been completed. Remove power and all test connections. Remove the board from the extender card and installed the board in a CompactPCI host system.

Calibration Procedure for ±10.0 V Output Range

Setup:

Perform the following steps to initialize the setup:

1. Configure jumper E9 (jumper omitted) for a 20 V span, and jumper E10 (pins 2 and 3) for the bipolar range as shown in Figure 2-1 on page 26.
2. Install the board into a CompactPCI host system using the CompactPCI bus extender board if necessary.
3. Connect the DMM positive (+) lead to pin 1 of the P1 connector (CHOUT0), the output of the sample-and-hold buffer for channel 0. Connect the DMM negative (-) lead to pin 20 of the P1 connector (AGND). See Table 2-3 on page 36 for the P1 connector pinout.

NOTE: The P1 connector pins 20 through 35 are local ground reference points.

---

4. Turn power ON to the CompactPCI host system.

DAC Output Adjustments:

Perform the following steps to adjust the DAC output voltage:

1. Write $0A80 to the CSR at relative address 0. This configures the board for the Fail LED off, straight binary format and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Adjust potentiometer R27 for a DMM reading of 0.000 ±0.0010 VDC.
4. Write $0FFF to CH1 SRAM location at relative address $12.
5. Adjust potentiometer R32 for a DMM reading of +9.9951 ±0.0010 VDC.
6. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4), therefore, repeat steps 1 through 6 as many times as required.
7. To verify that all channels are operational, sequentially move the DMM positive (+) lead to the remaining output channel pins (pins 2 through 8). The DMM should read +0.0000 ±0.0010 VDC for all channels.

Calibration for the ±10.0 V output range has been completed. Remove power and all test connections. Remove the board from the extender card and installed the board in a CompactPCI host system.

Connector Descriptions

The VMICPCI-4320 board has two connectors, P1 and J1.

- P1 is the external I/O connector, located on the front panel.
- J1 is the CompactPCI bus backplane connector.

CompactPCI bus Connector (J1)

The VMICPCI-4320 was designed for a 5 V 32-bit CompactPCI system. However, it is also signal compatible with a 5 V 64-bit CompactPCI system.

Refer to your host system documentation for information on compatible CompactPCI card types. Below is an illustrate of the J1 connector along with the connector pinout. Signals marked with N/C have no connection on the VMICPCI-4320.

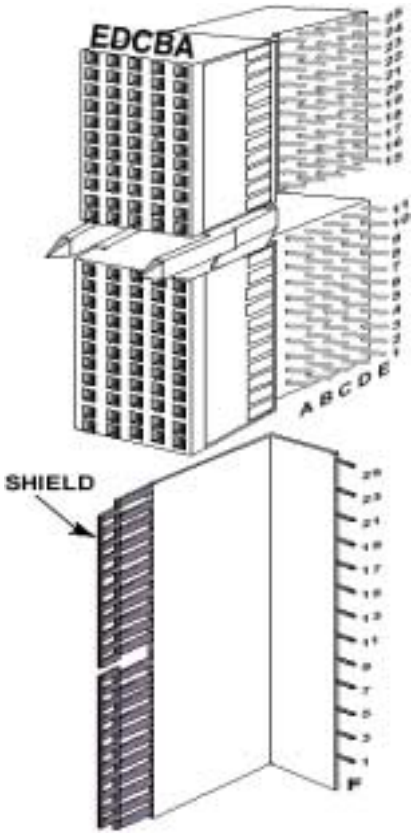

Figure 2-3 J1 Connector

Table 2-2 J1 Connector Pinout

Pin No.	Row E	Row D	Row C	Row B	Row A	Row F
25	+5 V	N/C	N/C	N/C	+5 V	GND
24	N/C	IN_AD[0]	+5 V	+5 V	IN_AD[1]	N/C
23	IN_AD[2]	+5 V	IN_AD[3]	IN_AD[4]	N/C	GND
22	IN_AD[5]	IN_AD[6]	N/C	GND	IN_AD[7]	N/C
21	INC/BE[0]	GND	IN_AD[8]	IN_AD[9]	N/C	GND
20	IN_AD[10]	IN_AD[11]	N/C	GND	IN_AD[12]	N/C
19	IN_AD[13]	GND	IN_AD[14]	IN_AD[15]	N/C	GND
18	INC/BE[1]	INPAR	N/C	GND	INSERR	N/C
17	INPERR	GND	N/C	N/C	N/C	GND
16	INLOCK	INSTOP#	+5 V	GND	IN_DEVSEL	N/C
15	INTRDY	GND	INIRDY	IN_FRAME	N/C	GND
12 through 14 are lost to the keying area						
11	INC/BE[2]	GND	IN_AD[16]	IN_AD[17]	IN_AD[18]	GND
10	IN_AD[19]	IN_AD[20]	N/C	GND	IN_AD[21]	N/C
9	IN_AD[22]	GND	IN_AD[23]	INIDSEL	INC/BE[3]	GND
8	IN_AD[24]	IN_AD[25]	+5 V	GND	IN_AD[26]	N/C
7	IN_AD[27]	GND	IN_AD[28]	IN_AD[29]	IN_AD[30]	GND
6	IN_AD[31]	CLK	N/C	GND	N/C	N/C
5	N/C	GND	INRST	N/C	N/C	GND
4	N/C	N/C	+5 V	GND	N/C	N/C
3	N/C	+5 V	N/C	N/C	N/C	GND
2	N/C	N/C	N/C	+5 V	N/C	N/C
1	+5 V	N/C	N/C	N/C	+5 V	GND

I/O Connector (P1)

P1 is a 37-pin D-Shell Subminiature Connector (female type). The figure below provides a view of the P1 connector and the location of pin 1. Table 2-3 details the connector pinout assignments.

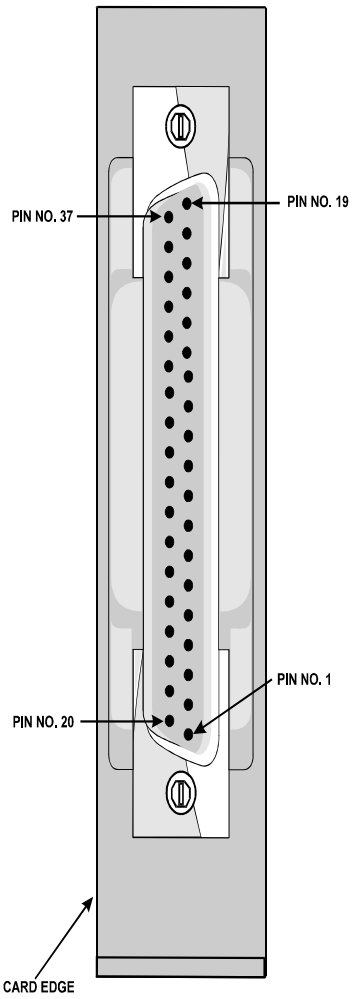

Table 2-3 P1 Connector Pinout

Pin No.	Signal	Function	Pin No.	Signal	Function
37	N/C	N/A	19	N/C	N/A
36	N/C	N/A	18	N/C	N/A
35	AGND	Analog Ground	17	AGND	Analog Ground
34	AGND	Analog Ground	16	N/C	N/A
33	AGND	Analog Ground	15	N/C	N/A
32	AGND	Analog Ground	14	N/C	N/A
31	AGND	Analog Ground	13	N/C	N/A
30	AGND	Analog Ground	12	N/C	N/A
29	AGND	Analog Ground	11	N/C	N/A
28	AGND	Analog Ground	10	N/C	NA
27	AGND	Analog Ground	9	N/C	N/A
26	AGND	Analog Ground	8	CHOUT7	Chan 7 Output
25	AGND	Analog Ground	7	CHOUT6	Chan 6 Output
24	AGND	Analog Ground	6	CHOUT5	Chan 5 Output
23	AGND	Analog Ground	5	CHOUT4	Chan 4 Output
22	AGND	Analog Ground	4	CHOUT3	Chan 3 Output
21	AGND	Analog Ground	3	CHOUT2	Chan 2 Output
20	AGND	Analog Ground	2	CHOUT1	Chan 1 Output
			1	CHOUT0	Chan 0 Output

Figure 2-4 P1 Connector (Female)

System Considerations

Output Cables

Optimum performance is obtained if the cables consist of individually twisted and shielded pairs. Short of individually shielded pairs, twisted pairs with a group or bundle shield is recommended. P1 pins 17 and 20 through 35 serve as signal returns and to tie cable shields to the board AGND.

General Guidelines

The grounding scheme used can have a major effect on system performance. Each system has its own unique interface considerations, but the following general guidelines will apply in most cases:

1. Keep cables short, particularly in voltage output mode with high currents, to avoid voltage drops in cables.
2. Each output should have a separate AGND return to the VMICPCI-4320. An ample number of pins on the P1 connector were devoted to AGND for this purpose.

CHAPTER 3

Programming

Contents

Introduction

The PCI Configuration Registers called Base Address Register #1 (BADR1), and Base Address Register #2 (BADR2) each contain a 32-bit address. This is the base address of the registers that apply to VMICPCI-4320 board. See Figure 3-1 on page 40 for a typical example of the Base Address Register addressing. Two groups of 64-byte addresses are dedicated to these functions. For each of the 64-byte addresses, only the 32 even addresses should be used since all VMICPCI-4320 function-specific registers are organized as 16 bits wide. The first eight even byte addresses with offsets $0 through $E access the VMICPCI-4320 Control and Status Register (CSR). The next sixteen even addresses with offsets $10 through $2E access 16 SRAM locations. The first eight of these SRAM locations store the digital values representing the eight analog outputs. The second eight SRAM locations are spares. The byte address offsets $30 through $3F are reserved. A memory map of the VMICPCI-4320 board is shown in Table 3-1 on page 40.

Table 3-1 VMICPCI-4320 8-Channel CompactPCI bus Analog Output Board's Memory Map

Relative Address	Function	Access Type
$00 Through $0E	Control and Status Register (CSR)	Read / Write
$10	SRAM Location 0 (Analog Output Channel 0 Data)	Read / Write
$12	SRAM Location 1 (Analog Output Channel 1 Data)	Read / Write
$14	SRAM Location 2 (Analog Output Channel 2 Data)	Read / Write
$16	SRAM Location 3 (Analog Output Channel 3 Data)	Read / Write
$18	SRAM Location 4 (Analog Output Channel 4 Data)	Read / Write
$1A	SRAM Location 5 (Analog Output Channel 5 Data)	Read / Write
$1C	SRAM Location 6 (Analog Output Channel 6 Data)	Read / Write
$1E	SRAM Location 7 (Analog Output Channel 7 Data)	Read / Write
$20 Through $2E	SRAM Location 8 through 15 (Spare)	Read / Write
$30 Through $3E	(Reserved)	----------

Example: If either BADR1 or BADR2 contains the address $3040, then the Control and Status Register is found at the address starting at $3040 and proceeds through $304E. The first SRAM location 0, is found at $3050, with SRAM 1 at $3052, SRAM 2 at $3054, ending with SRAM 7 at location $305E. Each of these SRAM address contains a 16-bit data word that indicates the digital input voltage value coming in from the CompactPCI bus. The values are sent to the on-board DAC and ultimately are sent to the analog output pins on the board's P1 connector. These are the analog values of the digital input signals stored in each of the SRAM location.

```
-> f  114a 4320  0

Bus#  =  0                          Device_function# = 68
Dev  ID  =  4320                    Vendor ID = 114a
Status  =  0                        Command = 107
Class Code  =  ff0000               Rev ID = c0
Base Addr Req 0 = fe81
Base Addr Req 1 = fd81
Base Addr Req 2 = ffafff40
Base Addr Req 3 = 0
Base Addr Req 4 = 0
Base Addr Req 5 = 0
Exp ROM Base   = 0
Int pin = 0                         Int line = 0
->
```

Figure 3-1 Typical I/O (Regs 0 and 1) and Memory (Reg 2) Mapped Base Address Registers

Control and Status Register Description

A write to any of the first eight relative addresses (or base address + offset) loads the data into the Control Register. A read of the first eight relative addresses returns the status of the board. Several of the status bits echo the states of the corresponding bits in the Control Register, while other status bits provide additional information or are fixed to a constant one (1) or zero (0) state.

Control Register Bit Assignments

There are 16 data bits in the Control Register, out of the 16 possible data bits only four have assigned functions. Those functions are detailed below:

Table 3-2 Control Register Bit Map

Control Register (Offset $00 Through $0E) Write-Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved				LED_OFF	TWO'S COMP	V OUT ENABLE	Reserved

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
SCAN ENABLE	Reserved						

Control Register Bit Definitions

Bits 15 through 12 — **Reserved:** These bit are reserved and should be written to zero (0).

Bit 11 — **LED_OFF:** When set to a logical one (1), the Fail LED is turned off.

Bit 10 — **Two's Complement:** Setting this bit to a logical zero (0) causes the DAC coding format to be straight binary. A logical one (1) sets the data format to two's complement of data bit 12.

Bit 09 — **V Out Enable:** Setting this bit to a logical one (1) enables the voltage outputs. Setting this bit to a zero disables the voltage outputs.

Bit 08 — **Reserved:** These bit are reserved and should be written to zero (0).

Bit 07 — **Scan Enable:** The refresh (scan) cycle is enabled when this bit is set to a logical one (1).

Bits 06 through 00 — **Reserved:** These bit are reserved and should be written to zero (0).

Status Register Bit Assignments

All 16 data bits of the Status Register are defined as either true status or a fixed state. The bit map and bit descriptions are detailed below:

Table 3-3 Status Register Bit Map

Status Register (Offset $00 Through $0E) Read-Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Fixed High				LED_OFF	TWO'S COMP	V OUT ENA	Reserved

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SCAN ENABLE	Fixed Low				CHAN COUNT		

Status Register Bit Definitions

Bits 15 through 12 — **Fixed High**: These four bits (MSBs) are factory fixed high and each will read as a logical one (1).

Bit 11 — **LED_OFF:** When read, this bit indicates the state of the Control Register bit 11 (Fail LED).

Bit 10 — **Two's Complement:**When read, this bit indicates the state of the Control Register bit 10 (Two's Complement).

Bit 09 — **V Out Enable:** When read, this bit indicates the state of the Control Register bit 09 (V Out Enable).

Bit 08 — **Reserved:** Reserved.

Bit 07 — **Scan Enable:** When read, this bit indicates the state of the Control Register bit 07 (I Out Enable).

Bits 06 through 03 — **Fixed Low:** These four bits (MSBs) are factory-fixed low and each will read as a logical zero (0).

Bits 02 through 00 — **CHAN Count:**When read, the three bits indicate the current state of the channel counter.

When calibrating the board, a value of $0A80 is written to the Control Register at address (relative address) 0. See *Calibration Procedures* starting on page 31. A typical command would be: I/O Write Short (iws) $3040 $0A80..... meaning write to an I/O device at address $3040, the 16-bit data value $0A80. This turns off the LED, selects straight binary format, and enables the voltage output switches. See Status Register bits.

Initialization

When a system reset is applied to the board, all Control Registers are cleared to zero (0). Therefore, the Fail LED will be on, the voltage outputs are disconnected, and the refresh cycle is disabled. The SRAM locations, upon power up, assume unknown states and must be written to using CompactPCI writes prior to asserting the Control Register output enables.

Controlling the Analog Outputs

The eight analog output channels appear to the controlling processor as eight consecutive 12-bit words in the I/O and/or memory space assigned to the VMICPCI-4320 board. The memory map shown in Table 3-1 on page 40 lists the board-relative address of each output channel. Each analog output SRAM location supports both *read* and *write* operations, eliminating the need for corresponding shadow latches in the processor Random Access Memory (RAM) space.

Setting the Analog Outputs

Digital codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four Most Significant Bits (MSBs) (D12 to D15) will be ignored, and will not be retained for read back. Each output will respond to a new code within 792 µs after the code is written to the output register if scan and outputs are enabled. The Digital-to-Analog (D/A) coding conventions used by the D/A Converter (DAC) are shown below.

Straight Binary - OUTPUT (volts DC) = (SPAN/4096 * DAC_INPUT) + MIN_OUT

Where SPAN is MAX_OUT - MIN_OUT

DAC_INPUT ranges from 0 to 4095 decimal ($0 to $FFF), MAX_OUT is the DAC output with $FFF as the input, and MIN_OUT is the DAC output with 000 as the input.

TWO's COMP - OUTPUT (volts DC) = (SPAN/4096 *(DAC_INPUT 0x0800))

where

DAC_INPUT ranges from -2048 to 2047 decimal ($800 to $7FF), MAX_OUT is the DAC output with $7FF as the input, and MIN_OUT is the DAC output with $800 as the input.

Table 3-4 DAC Data Format and Coding

DAC DATA FORMAT							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	D	D	D	D

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
D	D	D	D	D	D	D	D

NOTE: Bits 15 through 12 are don't care.

Table 3-5 DAC Coding

UNIPOLAR RANGES			STRAIGHT BINARY			
OUTPUT	**0 TO +10 V**	**0 TO +5 V**	**D15 - D12**	**D11 - D8**	**D7 - D4**	**D3 - D0**
+FS	+9.9975 V	+4.9988 V	XXXX	1111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	XXXX	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001

BIPOLAR RANGES				OFFSET BINARY			
OUTPUT	**+10 V**	**+5 V**	**+2.5 V**	**D15 - D12**	**D11 - D8**	**D7 - D4**	**D3 - D0**
+FS	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	1111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	1000	0000	0001
-1 / 2 FS	-0.0049 V	-0.0024 V	-0.0012 V	XXXX	0111	1111	1111
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	0000	0000	0000

BIPOLAR RANGES				TWO'S COMPLEMENT			
OUTPUT	**+10 V**	**+5 V**	**+2.5 V**	**D15 - D12**	**D11 - D8**	**D7 - D4**	**D3 - D0**
+FS	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	0111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	0100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	1000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	1000	0000	0000

Off-Line Operation

Setting the V Out Enable bit in the CSR (bit 09) connects and enables all channels configured as voltage outputs. When the V Out Enable bit is low, the voltage outputs are disconnected by way of an analog switch and appears as high impedance.

As mentioned earlier, the SRAM locations assume unknown states upon power up. To keep the outputs from assuming unpredictable levels, it is advisable to load the desired starting output levels into the SRAM prior to enabling the V Out Enable or I Out Enable bits.

Scan Enable

Setting the Scan Enable bit in the CSR (bit 07) high enables the refresh scanning cycles. If Scan Enable is set low with the outputs enabled, the outputs will quickly and unpredictably drift from their last set values. Under normal operation, the SRAM is first loaded with the initial values, then this control bit is set high and left high.

Maintenance

Maintenance

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

1. Software
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components of adjacent boards are disturbed when inserting or removing the board from the PCI board slot
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

VMIC's Customer Service can be reached by any of the following:

Direct: 256-650-8398

Toll-Free Direct: 800-240-SRVC (7782)

FAX: 256-650-7245

Email: customer.service@vmic.com

Maintenance Prints

User-level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.