

# **VMIPCI-2335**

## **PCI bus 16-Channel Optically Coupled Digital Output Board with Built-in-Test**

### **Product Manual**



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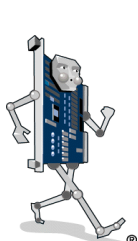
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# Overview

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## Introduction

The VMIPCI-2335 Optically Coupled Digital Output board is designed to provide isolation between the field and PCI bus chassis. There are 16 optically coupled outputs. The outputs provide a sustained 1.5 kV of system isolation to the PCI bus backplane.

The VMIPCI-2335 Optically Coupled Digital Output board has several features as specified below.

- a. 16 optically coupled voltage sourcing or current sinking outputs
- b. Pull-up resistors for the Voltage Sourcing output
- c. External voltage may be applied on byte boundaries to supply power for voltage sourcing mode
- d. On-board Built-In-Test logic for fault detection and isolation
- e. Front panel with standard 37-pin female connector
- f. 8-, 16-, or 32-bit data transfers
- g. Output ranges to a maximum of 50 V
- h. Output range to a maximum 300 mA
- i. Fail LED
- j. 1/2 card length
- k. Compliance with PCI Specification; Revision 2.1

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## Functional Description

The output circuitry of the VMIPCI-2335 has two configurations, Voltage Sourcing or Current Sinking. For the voltage sourcing option, pull-up resistors are installed on the optically coupled, open-collector outputs. The user supplies voltage to the VEXT pins on the interface connector, P1. The current sinking option has no pull-up resistors installed. These output functions may be selected on byte boundaries.

This board supports Built-In-Test (BIT) of most of the active components. This allows the host to write data to a register, read it back, and compare the two to determine the health of the board. After the integrity of the board has been determined, the board may be changed from off-line to on-line mode.

A Control and Status Register (CSR) is used to control and monitor the state of the board. This register allows independent control of the on-line/off-line state of the outputs and provides control for the Fail LED. The purpose of the Fail LED is for status indication under user software control. The default reset condition of the Fail LED is ON. This does not indicate a failure of the board because the board does not contain any self-test capabilities.

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## Reference Material List

Refer to the *PCI Local Bus Specification Revision 2.1* for a detailed explanation of the PCI bus. The *PCI Local Bus Specification Revision 2.1* is available from the following source:

*PCI Local Bus Specification, Revision 2.1*

PCI Special Interest Group

P.O. Box 14070

Portland, OR 97214

(800) 433-5177 (U.S.A)

(503) 797-4207 (International)

(503) 234-6762 (FAX)

Refer to VMIC product specification description No. 800-852335-000

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## Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

### Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

### Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

### Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

### Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

### Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

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**WARNING** Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

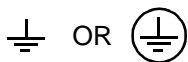
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## Safety Symbols Used in This Manual



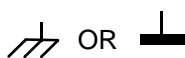
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).



The STOP symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

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**WARNING** Denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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**Caution** Denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

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**Note** Denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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# *Theory of Operation*

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## Introduction

The following sections are designed to describe the functionality of the VMIPCI-2335 board. This discussion includes the VMIPCI-2335's role in the system hardware architecture as well as important individual registers located on the board itself.

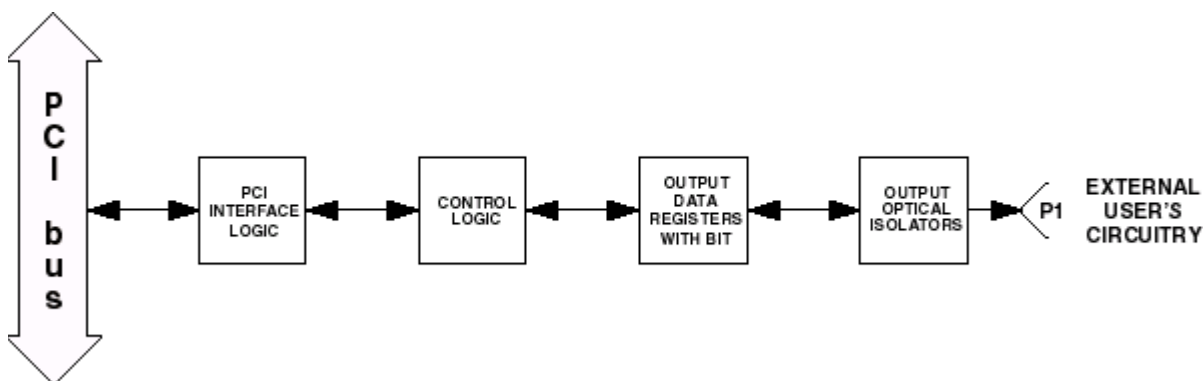
## Operational Overview

The VMIPCI-2335 Optically Coupled Digital Output board is designed to provide isolation between the system hardware and the PCI bus. The output voltage level is determined by the system hardware to which it is connected.

The VMIPCI-2335 board address is assigned by the system BIOS during system powerup per the PCI specification. By executing a write cycle to the data registers, data is steered from the backplane to the Output Data Register (ODR). The data stored in this register is used to drive the open-collector output to the field.

The VMIPCI-2335 has Built-In-Test (BIT) registers. They are used to check the health of the board. In order to prevent interaction with the field during BIT, the host first takes the board off-line to isolate the outputs, then simply writes data to the register to be checked. Then by reading the register and comparing the data read to the data written, the user can determine if the board is functioning correctly. In order to maintain isolation between the field and the PCI bus, the Built-In-Test can only verify the circuitry associated with the PCI bus side of the board.

Figure 1-1 is a block diagram of the basic functions of the VMIPCI-2335. These blocks will be discussed in more detail in the following sections.



**Figure 1-1** VMIPCI-2335 Functional Block Diagram

## PCI Compatibility

The VMIPCI-2335 is a PCI Specification 2.1 compliant add-on slave card. The board occupies 64 bytes of contiguous I/O space and can be mapped onto any PCI I/O space. The board does not utilize interrupts or DMA access and the hardware does not require a "wait state."

## Data Polarity

The VMIPCI-2335 has positive true output data polarity. On the PCI bus, when a 1 is written to an output, the open-collector output transistor will be active (turned on).



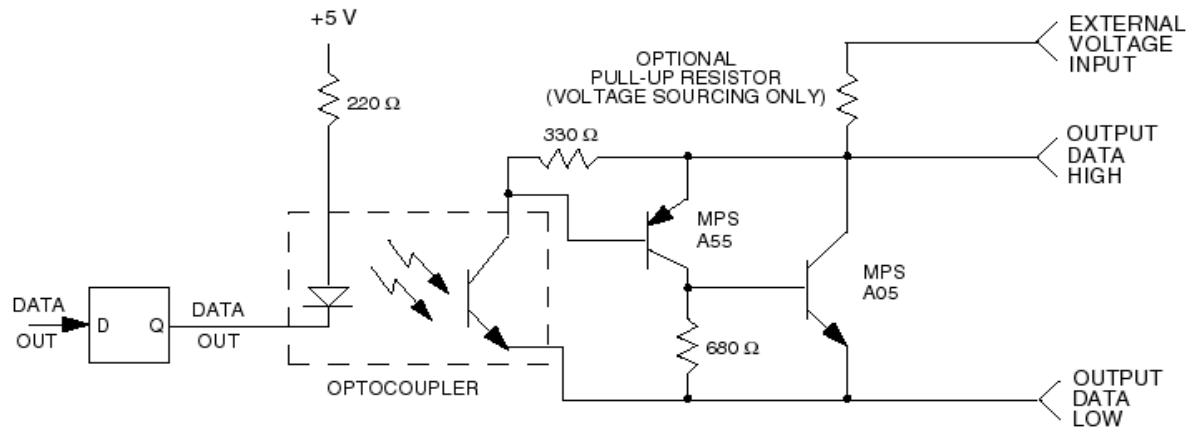
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## **Output Data Registers**

The Output Data registers may be read back to check for proper functioning of the board. This allows the user to simply write to and then read from the port to be checked. Data stored in the Output Data Register will be read back to the PCI bus when read.

## Output Circuitry

Figure 1-2 shows the basic topology of each output. The information stored in the Output Data Register from a PCI bus write is gated to the LED of the optocoupler. The output of the optocoupler biases the output transistors ON or OFF.



**Figure 1-2** Typical Output Configuration

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## Output Types

The open-collector outputs can be configured for one of two types, either voltage sourcing or current sinking. Current sinking outputs do not have pull-up resistors installed. Pull-up resistors are present if the outputs are configured for voltage sourcing. These pull-up resistors may be driven by an external voltage supplied by the user. There are two such external voltage inputs, one for each byte. Output channels 0 through 7 may be pulled up with VEXT0 (pin 36). Output channels 8 through 15 may be pulled up with VEXT1 (pin 17).

## Configuration Space

This portion of the theory of operation defines the programming model and usage rules for the configuration register space in PCI compliant devices. The intent of the PCI configuration space definition is to provide an appropriate set of configuration "hooks" which satisfies the needs of current and anticipated system configuration mechanisms.

### Configuration Space Organization

This section defines the organization of configuration space registers and imposes a specific record structure or template on the 256-byte space. This space is divided into a predefined header region and a device dependent region. Devices implement only the necessary and relevant registers in each region. A device's configuration space must be accessible at all times, not just during system boot. The predefined header region has a size of 64 bytes and every device must support the register layout of this region. This region consists of fields that uniquely identify the device and allow the device to be generically controlled. See Figure 1-3 below.

D31		D16 D15		D0
DEVICE ID 2335		VENDOR ID 114 A		\$00
STATUS 0000		COMMAND 0000		04h
CLASS CODE 08 80 00			REVISION ID 00	08h
BIST 00	HEADER TYPE 00	LATENCY TIMER 00	CACHE LINE SIZE 00	0Ch
BASE ADDR				10h
BASE ADDRESS REGISTERS				14h
				18h
				1Ch
				20h
				24h
RESERVED				28h
RESERVED				2Ch
EXPANSION ROM BASE ADDRESS				30h
RESERVED				34h
RESERVED				38h
MAX_LAT 00	MIN_GNT 00	INTERRUPT PIN 00	INTERRUPT LINE FF	3Ch

**Figure 1-3** Configuration Space Header

All compliant devices must support the Vendor ID, Device ID, Command and Status fields in the header. Implementation of other registers is optional (that is, they can be treated as reserved registers) depending on device functionality. If a device supports the function that the register is concerned with, the device must implement it in the defined location and with the defined functionality.

## Configuration Space Functions

PCI has the potential for greatly increasing the ease with which systems may be configured. To realize this potential, all PCI devices must provide certain functions that system configuration software can utilize. This section also lists the functions that need to be supported by PCI devices by way of registers defined in the predefined header portion of the configuration space. The exact format of these registers (that is, number of bits implemented) is device-specific. However, some general rules must be followed. All registers must be capable of being read back and the data returned must indicate the value that the device is actually using.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions. Its use should be restricted to initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers.

### Device Identification

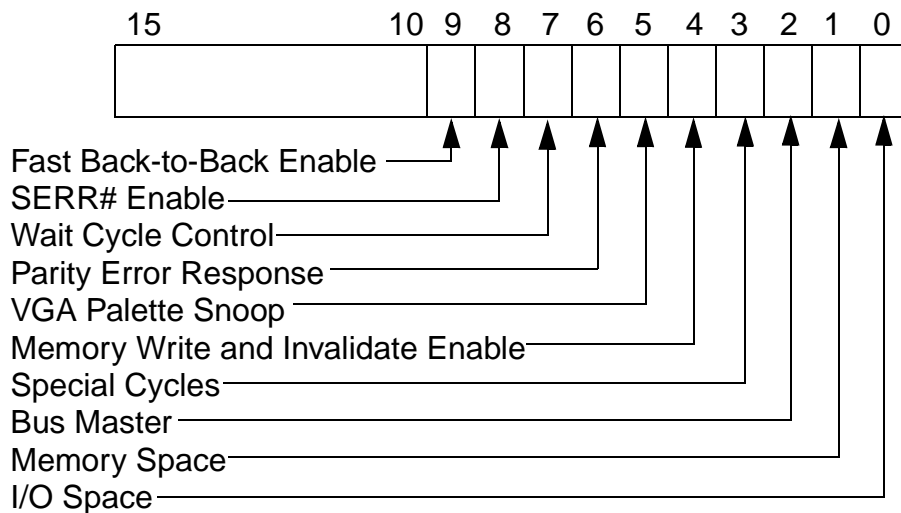
Five fields in the predefined header deal with device identification. All PCI bus devices are required to implement these fields. Generic configuration software will be able to easily determine what devices are available on the system's PCI bus(es). All of these registers are read-only.

<b>Vendor ID</b>	This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. \$114A is VMIC's vendor ID.
<b>Device ID</b>	This field identifies the particular device. This identifier is allocated by the vendor. The Device ID for the VMIPCI-2335 is \$2335.
<b>Revision ID</b>	This register specifies a device-specific revision identifier. The value is chosen by the vendor. \$C0 is the default value. This field should be viewed as a vendor-defined extension to the Device ID.
<b>Header Type</b>	This byte identifies the layout of location \$10 through \$3F in configuration space and also whether or not the device contains multiple functions. Bit 7 in this register is used to identify a multifunction device. If the bit is 0, then the device has multiple functions. Bits 6 through 0 specify the layout of locations \$10 through \$3F. One encoding, \$00, is defined and specifies the layout shown in Figure 1-3 on page 20. All other encodings are reserved.

**Class Code** The Class Code Register is used to identify the generic function of the device. The register is broken into three byte-size fields. The upper byte (at offset \$0B) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset \$0A) is a subclass code which identifies more specifically the function of the device. The lower byte (at offset \$09) identifies a specific register-level programming interface (if any) so that device-independent software can interact with the device.

## Device Control

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality. For instance, devices that do not implement an I/O space probably will not implement a writable element at bit location zero of the Command register. Devices typically come up with all zeros in this register. Figure 1-4 shows the layout of the register and Table 1-1 on page 23 explains the definitions of the different bits in the Command register.



**Figure 1-4** Command Register Layout

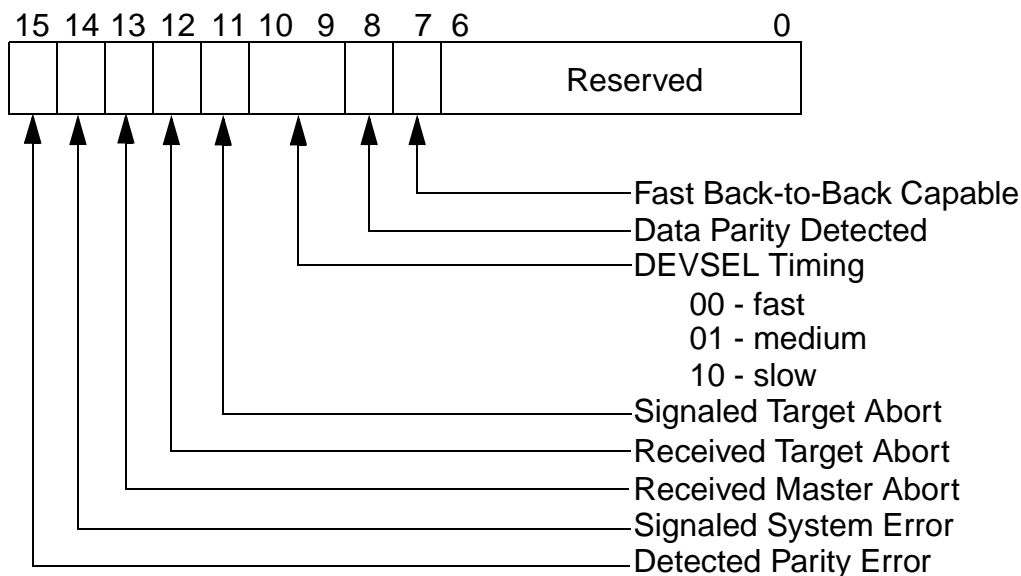
**Table 1-1** Command Register Bits

Bit Location	Bit Definitions
0	Controls a device's response to I/O space accesses. A value of zero disables the device response. A value of 1 allows the device to respond to I/O space accesses. State after RST# is 0.
1	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to memory space accesses. State after RST# is 0.
2	Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. State after RST# is 0.
3	Controls a device's action on Special Cycle Operations. A value of 0 causes the device to ignore all Special Cycle Operations. A value of 1 allows the device to monitor Special Cycle Operations. State after RST# is 0.
4	This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When this bit is 0, Memory Write must be used instead. State after RST# is 0. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
5	This bit controls how VGA-compatible devices handle accesses to VGA palette registers. When this bit is 1, special palette snooping behavior is enabled (i.e., device must not respond). When the bit is 0, the device should treat palette accesses like all other accesses. VGA-compatible devices should implement this bit.
6	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device must ignore any parity errors that it detects and continue normal operation. This bit's state after RST# is 0. Devices that check parity must implement this bit. Devices are still required to generate parity even if parity checking is disabled.
7	This bit is used to control whether or not a device does address/data stepping. Devices that never do stepping must have this bit hardwired to 0. Devices that always do stepping must have this bit hardwired to 1. Devices that can do either should make this bit read/write and have it initialize to 1 after RST#.
8	This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. This bit's state after reset is 0. All devices that have an SERR# pin must implement this bit. This bit (and bit 6) must be ON to report address parity errors.
9	This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transactions to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent.
10-15	Reserved

## Device Status

The Status register is used to record status information for PCI bus related events. The definition of each of the bits is given in Table 1-2 on page 24, and the layout of the register is shown in Figure 1-5 below. Devices would not need to implement all bits, depending on device functionality. For instance, a device that acts as a target but will never signal target-abort, would not implement bit 11.

Reads to this register behave normally. Writes are slightly different in that the bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one (1). For instance, to clear bit 14 and not affect any other bits, write the value 0100\_0000\_0000\_0000b to the register.



**Figure 1-5** Status Register Layout

**Table 1-2** Status Register Bits

Bit Location	Descriptions
0 through 6	Reserved
7	This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions, and must be set to 0 otherwise.
8	This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.



**Table 1-2** Status Register Bits (Continued)

9 and 10	These bits encode the timing of DEVSEL#. The bits are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.
11	This bit must be set by a target device whenever the target terminates a transaction with a Target-Abort. All master devices must implement this bit.
12	This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
13	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
14	This bit must be set whenever the device asserts SERR#. Devices which will never assert SERR# do not need to implement this bit.
15	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled as controlled by bit 6 in the Command register.

## Interrupt Line

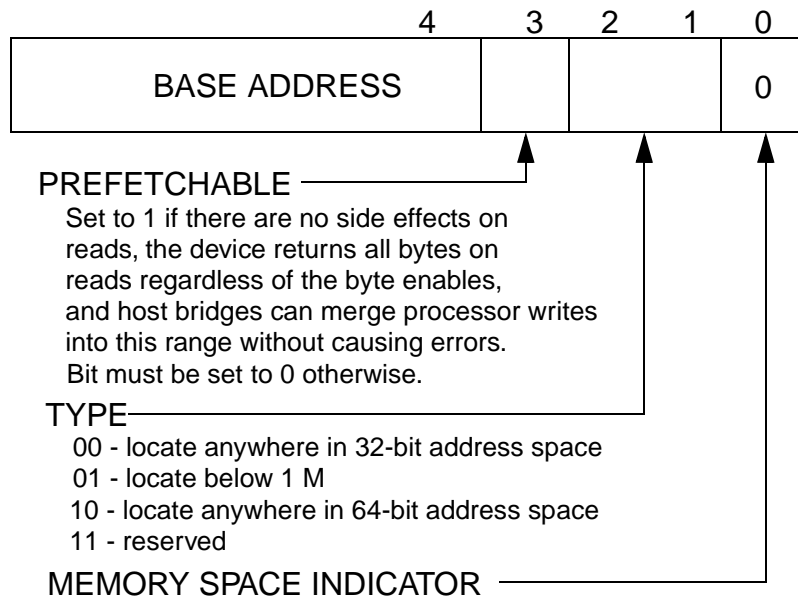
The VMIPCI-2335 does not utilize interrupts.

## Base Addresses

One of the most important functions for enabling superior configurability and ease-of-use is the ability to relocate PCI devices in the address spaces. At system powerup, device independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM. Each of these areas is covered in the following sections.

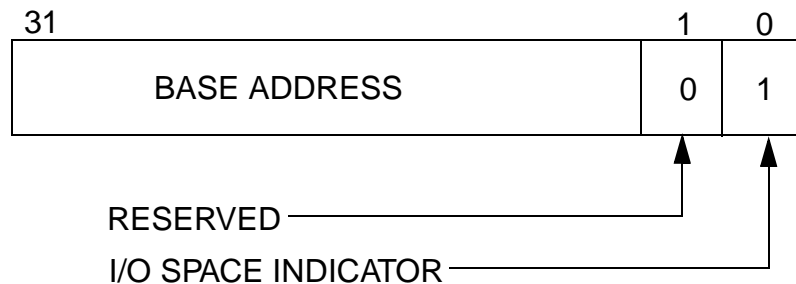
## Address Maps

Powerup software needs to build a consistent address map before booting the machine to an operating system. This means it must determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, powerup software can map the I/O controllers into reasonable locations and proceed with system boot. In order to do this mapping in a device independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space.



**Figure 1-6** Base Address Register for Memory

Bit 0 in all base registers is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a zero in bit 0. Base registers that map to I/O space must return a one in bit 0.



**Figure 1-7** Base Address Register for I/O

Base registers that map into I/O space are always 32 bits with bit 0 hardwired to a one, bit 1 is reserved and must return zero on reads, and the other bits are used to map the device into I/O space.

Base registers that map into memory space (Figure 1-6 can be 32 bits wide to support mapping into a 64-bit address space) have bit 0 hardwired to a zero. For memory base registers, bits 2 and 1 have an encoded meaning as shown in Table 1-3 below. Bit 3 should be set to one if the data is prefetchable, and reset to zero otherwise. A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bits 0 through 3 are read-only.

**Table 1-3** Bits 2/1 Encoding

Bits 2/1	Definition
00	Base register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
01	Base register is 32 bits wide but must be mapped below 1 Mbyte in memory space.
10	Base register is 64 bits wide and can be mapped anywhere in the 64-bit address space.
11	Reserved

The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. A device that wants a 1 Mbyte memory address space (using a 32-bit base address register) would build the top 12 bits of the address register hardwiring the other bits to zero.

Powerup software can determine how much address space the device requires by writing a value of all ones to the register and then reading the value back. The device will return zeros in all "don't care" address bits, effectively specifying the address space required.

This design implies that all address spaces used are a power of two in size, and are naturally aligned. Devices are free to consume more address space than required, but decoding down to a 4 Kbyte space for memory and 256 bytes for I/O is suggested for devices that need less than those amounts. Devices that do consume more address space than they use are not required to respond to the unused portion of that address space.

Six DWORD locations are allocated for Base Address registers starting at offset \$10 in configuration space. The first Base Address register is always located at offset \$10. The second register may be at offset \$14 or \$18 depending on the size of the first. The offsets of subsequent Base Address registers are determined by the size of previous Base Address registers.

A typical device will require one memory range for its control functions. Some graphics devices may use two ranges, one for control functions and another for a frame buffer. A device that wants to map control functions into both memory and I/O space at the same time must implement two base registers (one Memory, one I/O). The driver for that device might only use one space in which case the other space will be unused. Devices should always allow control functions to be mapped into memory space.

---

**Note** Any device that has a range that behaves like normal memory, but doesn't participate in PCI's caching protocol, should mark the range as prefetchable. a linear frame buffer in a graphics device is an example of a range that should be marked prefetchable.

---

Refer to the *PCI Local Bus Specification Revision 2.1* for detailed information about the PCI bus. The contact information to order the *PCI Local Bus Specification Revision 2.1* is given on page 11 of this manual.

# *Configuration and Installation*

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---

## Introduction

The VMIPCI-2335 16-Channel Digital Output Board with Built-in-Test is designed to provide isolation between the system hardware and the PCI bus. The board can be either current sinking or voltage sourcing, depending on the option ordered.

---

## Unpacking Procedures

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**Caution** Some of the components assembled on vmic's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes in which they were shipped. When the board is to be placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

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Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

## Physical Installation

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**Caution** Do not install or remove boards while power is applied.

---

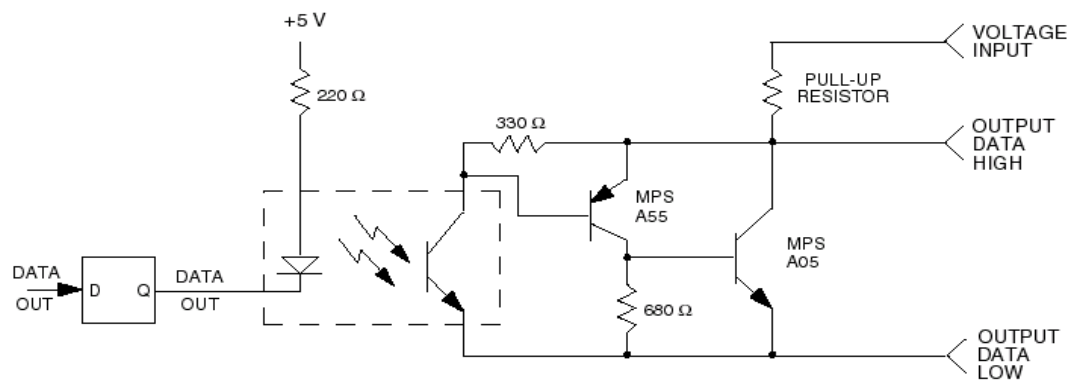
De-energize the equipment and locate the appropriate PCI bus expansion slot. While ensuring that the card bracket is properly aligned with the alignment screw hole, press the board smoothly into the mating connector until firmly seated.

## Board Configuration

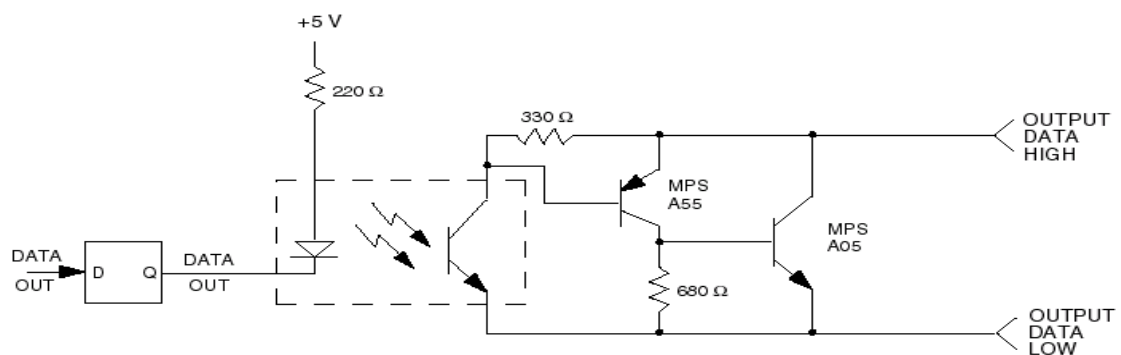
The VMIPCI-2335 can be factory configured for current sinking or voltage sourcing outputs. The pull-up resistors for the outputs are installed if the voltage sourcing configuration is ordered. The outputs for voltage sourcing are configured with one external voltage pin for every eight channels.

### Output Topology

Figure 2-1 shows the circuit topology for voltage sourcing outputs. Figure 2-2 shows the circuit topology for the current sinking configuration. Table 2-1 on page 32 shows the two external voltage inputs and the output channels affected by each.



**Figure 2-1** Typical Voltage Sourcing Output Configuration



**Figure 2-2** Typical Current Sinking Output Configuration

**Table 2-1** External Voltage

External Voltage	Channels Affected	P1 Pin
VEXT 0	Output Channels 0 through 7	36
VEXT 1	Output Channels 8 through 15	17



---

## Address Selection

The VMIPCI-2335 occupies 64 bytes (16 longwords) of I/O space. The choice of 64 bytes is dictated by some PCI hosts which do not properly recognize less. In fact, only the first four bytes (1 longword) are of interest, the remaining 15 longwords are just copies of the first. The actual absolute I/O address space is assigned at configuration time (along with all other PCI devices) as per PCI requirements.

---

## Before Applying Power: Checklist

1. Before installing the board in a PCI bus system, check the following items to ensure that the board is ready for the intended application.
2. Verify that the sections pertaining to theory and programming, Sections 3 and 4, have been reviewed and applied to system requirements.
3. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to "Connector Configuration" section for connector descriptions.
4. After the checklist above has been completed, the board can be installed in a PCI bus system.

---

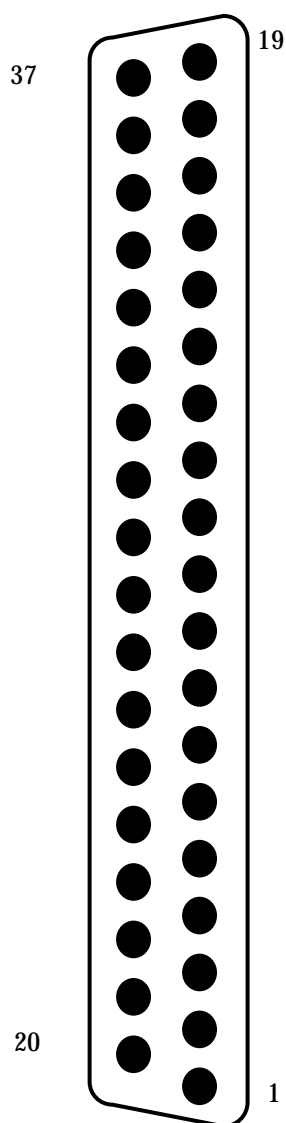
**Caution** Do not install or remove the boards while power is applied.

---

## Connector Configuration

The front panel input connector (P1) on the VMIPCI-2335 is a standard subminiature 37-pin female D-Shell. The card edge connector on the VMIPCI-2335 is a standard 32-bit, 5 V PCI bus connector.

Front View  
(Cable Side) of P1  
Connector



**Table 2-2** P1 Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
37	N/C	19	N/C
36	VEXT 0	18	N/C
35	LOW OUT 15	17	VEXT 1
34	LOW OUT 14	16	HIGH OUT 15
33	LOW OUT 13	15	HIGH OUT 14
32	LOW OUT 12	14	HIGH OUT 13
31	LOW OUT 11	13	HIGH OUT 12
30	LOW OUT 10	12	HIGH OUT 11
29	LOW OUT 9	11	HIGH OUT 10
28	LOW OUT 8	10	HIGH OUT 9
27	LOW OUT 7	9	HIGH OUT 8
26	LOW OUT 6	8	HIGH OUT 7
25	LOW OUT 5	7	HIGH OUT 6
24	LOW OUT 4	6	HIGH OUT 5
23	LOW OUT 3	5	HIGH OUT 4
22	LOW OUT 2	4	HIGH OUT 3
21	LOW OUT 1	3	HIGH OUT 2
20	LOW OUT 0	2	HIGH OUT 1
		1	HIGH OUT 0

**Figure 2-3** P1 Connector Pin Layout



# Programming

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## Introduction

The VMIPCI-2335 requires very little software. After performing any initialization or off-line testing, the user enters on-line mode by writing to the Control and Status Register (CSR). The user may then perform a write operation to the appropriate output register to modify the state of the field.

Where appropriate, information on programming these registers is provided. All values are in hexadecimal unless otherwise indicated.

The programming model for these register definitions includes a table with five lines. Line one is the base address offset of the register and the number of bits defined in the table. Line two shows the bits defined by this table. Line three defines the name of the register or the name of the bits in the register. Line four defines the operations possible on the register bits as follows:

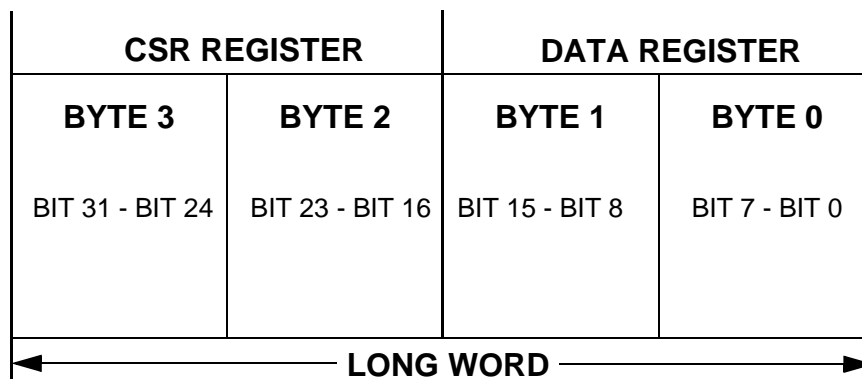
<b>R</b>	This bit is a read-only status bit.
<b>R/W</b>	This bit is readable and writable.
<b>W</b>	This bit is a write-only control bit.
<b>WC</b>	This bit is a write-to-clear control bit.

Line five defines the state of the bit following a reset as defined below:

<b>P</b>	The bit is set to the default state by a powerup reset.
<b>S</b>	The bit is set to the default state by a SYSRESET.
<b>L</b>	The bit is set to the default state by a local reset.
<b>X</b>	The bit is <i>not</i> affected by reset.

## I/O and Memory Mapped Space Definition

The VMIPCI-2335 reserves 64 bytes of both I/O and memory space. Of each of these 64 bytes, only 4 bytes (1 longword) are of interest. Figure 3-1 shows the definition for this longword.



**Figure 3-1** I/O and/or Memory Space Definition

## Control and Status Register (CSR)

Bytes 3 and 2 of the I/O address space comprise the Control and Status Register (CSR). The CSR is a 16-bit register that is used to control the board's Fail LED and on-line/off-line status. Table 3-1 shows the position of the bits used to perform these functions.

All control bits (31 through 16) will be low on powerup or after a PCI bus reset. This ensures that the board is in the off-line mode and prevents the board from interacting with the field until commanded by the host. This will also cause the Fail LED to illuminate.

**Table 3-1** Control and Status Register Bit Map

Control/Status Register, BYTE 3, (READ/WRITE)							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved			Data 0-7 Enable/Disable	Reserved		Data 8-15 Enable/Disable	Fail LED

Control/Status Register, BYTE 2, (READ/WRITE)							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved							

### **Control and Status Register Bit Definitions**

- Bits 31 to 29:** **Reserved.** These bits are reserved and will always read back as zero (0). Data written to these locations will be lost and has no effect on the board.
- Bit 28:** **EN\_LB** **Enable/Disable Lower Byte (Data 0-7).** Controls the ON/OFF status of data lines 0 through 7. Writing a zero (0) to this bit places these lines in the on-line mode and enables PCI bus writes to control the state of output lines 0 through 7. Writing a one (1) to this bit places these lines in the off-line mode and disables output lines 0 through 7 from being controlled from the PCI bus. At powerup or reset, this bit is set low.
- Bits 27 to 26:** **Reserved.** These bits are reserved and will always read back as zero (0). Data written to these locations will be lost and has no effect on the board.
- Bit 25:** **EN\_UB** **Enable/Disable Upper Byte (Data 8-15).** Controls the ON/OFF status of data lines 8 through 15. Writing a 0 to this bit places these lines in the on-line mode and enables PCI bus writes to control the state of output lines 8 through 15. Writing a 1 to this bit places these lines in the off-line mode and disables output lines 8 through 15 from being controlled from the PCI bus. At powerup or reset, this bit is set low.
- Bit 24:** **FAIL\_LED** **Fail LED Bit.** Controls the Fail LED. Writing a one (1) to this bit will turn the Fail LED OFF. At powerup or reset, this bit is set low causing the LED to be ON.

## Output Data Register Bit Definitions

Table 3-2 lists the input channels and their associated register bit locations. The Output Data Register can be read as a Byte or Word.

**Table 3-2** Output Data Register Bit Map

Output Data Register BYTE 1 (READ/WRITE)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08

Output Data Register BYTE 0 (READ/WRITE)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

**EXAMPLE:**

```
-> f 114a 2335 0

Bus# = 0                      Device_function# = 68
Dev ID = 2335                 Vendor ID = 114a
Status = 0                    Command = 107
Class Code = ff0000           Rev ID = 80
Base Addr Reg 0 = fe81
Base Addr Reg 1 = fd81
Base Addr Reg 2 = ffafff40
Base Addr Reg 3 = 0
Base Addr Reg 4 = 0
Base Addr Reg 5 = 0
Exp ROM Base = 0
Int pin = 0                    Int line = 0
->
```

**Figure 3-2** Typical I/O (Regs 0 and 1) and Memory (Reg 2) Mapped Base Address Registers



# Maintenance

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## Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

1. Software
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If the product must be returned, contact VMIC for a Return Material Authorization (RMA) Number. *This RMA Number must be obtained prior to any return.*

VMIC's Customer Service can be reached by any of the following:

Direct: 256-650-8398

Toll-Free Direct: 800-240-SRVC (7782)

FAX: 256-650-7245

Email: [Customer.Service@vmic.com](mailto:Customer.Service@vmic.com)

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## **Maintenance Prints**

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.