VMIPCI-3322
24-Channel, 16-bit PCI Analog-to-Digital Converter (ADC) Board

Product Manual

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

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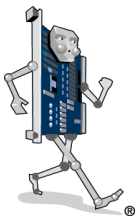

(I/O man figure)

(Instant OPC wizard logo)

(IOWorks man figure)

VMIC

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Introduction

The VMIPCI-3322 board is a 24-channel PCI bus analog input board with 16-bit digitizing resolution. The VMIPCI-3322 is jumper-selectable, supporting several input ranges. Also through factory-installed options, differential or single-ended modes and optional low pass inputs filters can be accommodated.

The VMIPCI-3322 automatically scans and digitizes (autoscans) up to 24 inputs at a rate of 10.05 msec per channel and stores the results in consecutive SRAM locations. The host PC may then read the results from the SRAM through the PCI bus at an independent rate. In addition to the 24 SRAM locations, the VMIPCI-3322 contains a single Control and Status Register (CSR) which is used to enable the basic functions and report status.

The following is a brief overview of the VMIPCI-3322 board:

- 24 differential or single-ended analog inputs
- 16-bit ADC autoscanning conversion
- 10.05 msec per channel conversion time
- Programmable 24, 16, or 8 channels per scan cycle
- ADC ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, and 0 to +10 V
- Optional low pass input filters

Functional Description

A functional block diagram of the VMIPCI-3322 is shown in Figure 1 on page 15. The major sections of the circuitry include 24 pairs of input buffers, a 24-channel differential multilplexer, an instrumentation amplifier, a 16-bit Analog-to-Digital Converter, 32 SRAM registers, timing and control circuitry, and a PCI local bus interface. The PCI interface is incorporated in a single PCI-compliant device. In addition, all timing and control circuitry, including the CSR, is located in one EPLD device.

Through the CSR you can:

- Select the output data format
- Toggle the Fail LED off and on
- Select the number of inputs (24, 16, or 8) to scan/convert
- Enable autoscan
- Issue a software reset

Upon powerup, system reset, or software reset the ADC performs a self-calibration which takes approximately 41 milliseconds. Also upon reset, the CSR is cleared and the autoscan cycle is disabled. The autoscan cycle remains disabled until an enable bit in the CSR is set. While the autoscan cycle is disabled, the SRAM can be verified through a series of PCI bus reads and writes.

Normally the CSR is written at least once to select the number of inputs to scan, select the output data format, and to enable the autoscan cycle. Once the autoscan is enabled, the VMIPCI-3322 sequentially samples the selected number inputs, converts each conditioned sample to a 16-bit digital value, and stores the result in a corresponding SRAM location. Arbitration circuitry permits the host PC to read any of the SRAM locations at any time without affecting the autoscan and digitization timing.

To achieve the sample rate of 10.05 microseconds per channel, the sample and conversion process is pipelined. Prior to converting each sample, an integral sample-and-hold within the ADC device switches to hold. Then while the ADC is converting one channel, the Analog Mux and Instrumentation Amplifier are switched to the next input to slew and settle. Likewise, the SRAM write of each conversion result is written while the ADC is converting the next channel.

Reference Material List

For a detailed explanation of the PCI Local bus and its characteristics, refer to the *PCI Local Bus Specification* from:

PCI Local Bus Specification, Revision 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
PH: (800) 433-5177 (U.S.)
(503) 797-4207 (International)

Intended Audience

Knowledge of PCI Local bus protocol is assumed. Additionally, you should be familiar with standard network protocol and configuration of the PCI device interface.

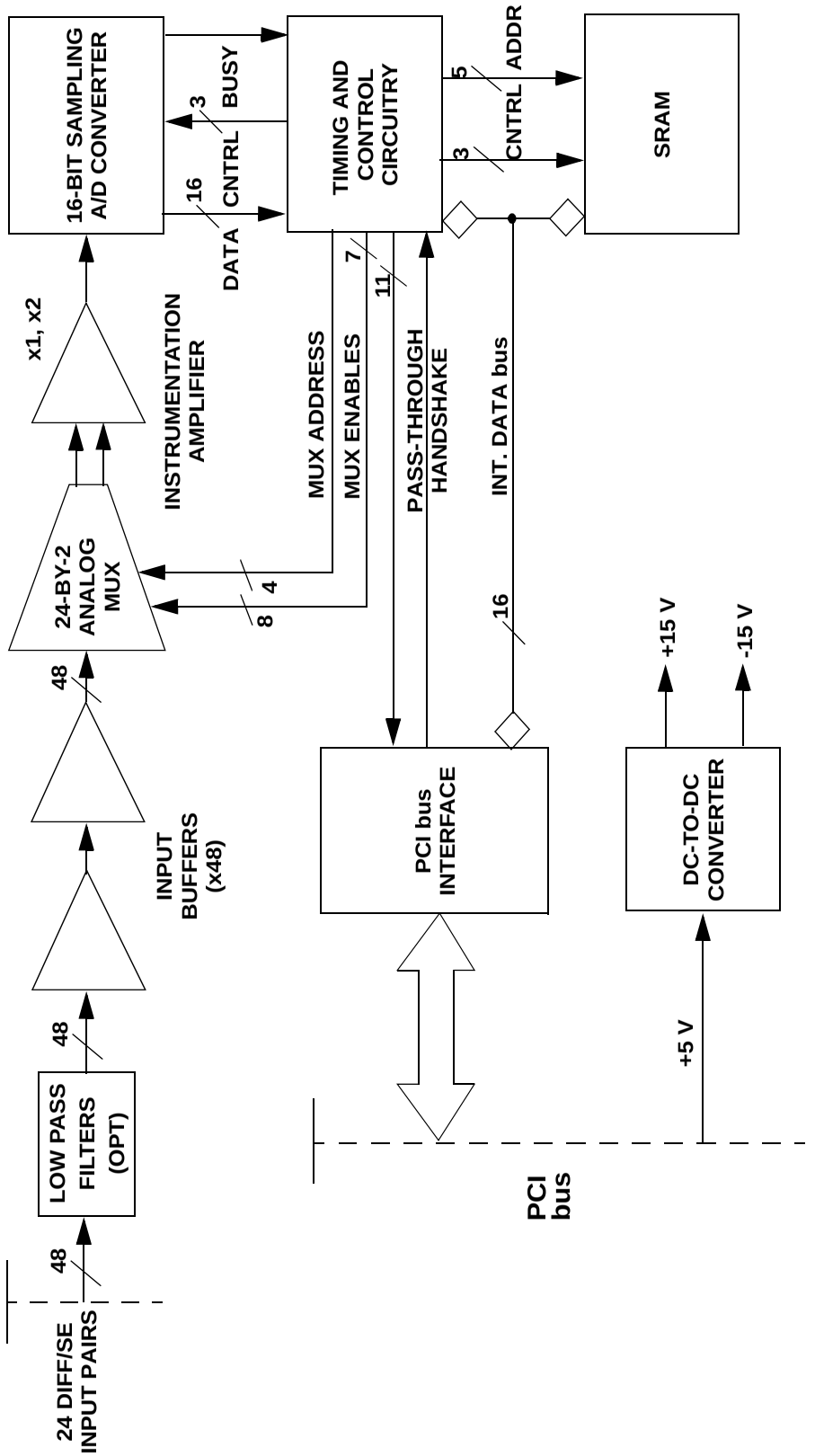


Figure 1 VMIPCI-3322 Functional Block Diagram

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

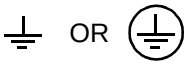
Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

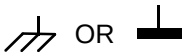
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



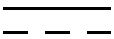
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

The STOP symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING Denotes a hazard. It calls attention to a procedure, a practice, or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution Denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

Note Denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER 1

Theory of Operation

Contents

Introduction

This section describes the internal operation of the VMIPCI-3322 board, and reviews the general principles of operation. The PCI bus Interface section summarizes the major board functions, and the remainder of this chapter addresses each function individually. The information in this section is supplemented by programming details in the chapter titled “Programming” on page 55.

Internal Function Organization

The VMIPCI-3322 board contains the following principal hardware functions, as shown in Figure 1 on page14:

1. PCI bus Interface
2. SRAM
3. Power Converter
4. Optional Low Pass Input Filters
5. Analog Input Buffers
6. Analog Multiplexer
7. Instrumentation Amplifier
8. Analog-to-Digital Converter (ADC)
9. Timing and Control Circuitry

The above topics are discussed in greater detail in the following subsections.

PCI bus Interface

The VMIPCI-3322 is implemented with a PCI bus compliant interface device. The VMIPCI-3322 operates as a PCI bus I/O “target” and supports simple “plug-and-play” capability. On one side, the PCI bus device contains the proper signals and timing to operate on the PCI local bus. On the other side, the PCI device provides an “add-on” interface to which the desired function specific circuitry is connected. In addition, the PCI bus interface device contains the full complement of pre defined configuration registers.

PCI bus Configuration Registers

Any PCI bus interface, which is compliant with the PCI bus specification contains a pre-defined group of configuration registers. This group of registers implements the primary PCI bus functions of identification, PCI bus Command and Status, and board configuration. Several of the standard registers, though present in the PCI bus interface device, do not apply to the VMIPCI-3322 board. However, registers that do apply are listed in the Table 1-1 below.

For a detailed explanation of the PCI local bus and its characteristics refer to the *PCI Local Bus Specification, Revision 2.1*.

Table 1-1 PCI Configuration Registers

Offset Address (Hex)	Register	Mnemonics	VMIPCI-3322 Value (Hex)	Access
00 through 01	Vendor Identification	VID	114A	Read Only
02 through 03	Device Identification	DID	3322	Read Only
04 through 05	PCI Command Register	PCICMD	0001	Read / Write
06 through 07	PCI Status Register	PCISTS	Varies	Read / Write
08	Revision ID Register	RID	0	Read Only
09 through 0B	Class Code Register	CLCD	FF	Read Only
10 through 13	Base Address Register 0	BADR0	Varies	Read / Write
14 through 17	Base Address Register 1	BADR1	Varies	Read / Write
18 through 21	Base Address Register 2	BADR2	Varies	Read / Write

Note Any write to the PCISTS register clears the register.

SRAM

The VMIPCI-3322 contains 32 16-bit wide SRAM locations accessible by the user. While the autoscan cycle is operating, the lower 24 locations of the SRAM store the conversion results of the corresponding input channels. The upper 8 SRAM locations, though accessible, have no specific function. The SRAM is PCI bus accessible via the even relative addresses $10 through $4E (the relative addresses are with respects to the contents of the Base Address Register 1.) All the SRAM locations may be written and read by way of the PCI bus. However, while the autoscan cycle is operating, the first 24 locations are also periodically written with conversion results. Therefore, while performing a memory test on the SRAM, the autoscan should be disabled.

Power Converter

The ±15 V power for the analog circuitry is supplied by an on-board DC-to-DC Converter, which is sourced by +5 V from the PCI bus.

Low Pass Filters

The VMIPCI-3322 inputs utilitize a single-pole passive low pass filters (optional) to minimize the effects of system noise and eliminate high-frequency signals, which would otherwise cause accuracy problems. The input filters also limit the upper frequency of the signal that can accurately be converted. Therefore, the filter options should be chosen with both the signal characteristics and system requirements in mind.

The VMIPCI-3322 offers four low pass filter options based on the -3 dB or corner frequency.

Those options are:

1. No filter
2. -3 dB at 50 Hz
3. -3 dB at 100 Hz
4. -3 dB at 500 Hz

The above cutoff frequencies apply to differential inputs. When the inputs are single-ended, the corner frequencies double.

Input Buffers

Each of the 24 differential inputs has a dedicated pair of input buffers. The input buffers eliminate errors resulting from high or varying source impedance. In addition, the buffers maintain high input impedance and minimize channel interaction while also permitting high sample rates.

Analog Multiplexer (MUX)

The Analog Multiplexer is a 24-channel differential structure, configured in two tiers. The first tier is composed of six multiplexers. Each of the multiplexers in the first tier can select one of four differential buffered pairs. The second tier then selects one of the six first tier outputs and gates the resulting selected pair to the input of the Instrumentation Amplifier. The MUX address and enables, which come from the timing and control circuits, are tailored to ensure break-before-make switching and minimal channel interaction.

Instrumentation Amplifier

The Instrumentation Amplifier converts the selected differential signal pair to a single-ended signal referenced to the ADC analog ground (AGND). It provides the high common-mode rejection required to achieve the rated accuracy. The Instrumentation Amplifier has a nominal gain of one, but can be jumpered for a gain of two, which is necessary for the ±2.5 V and 0 to 5.0 V ranges.

Analog-to-Digital Converter (ADC)

The ADC is a 16-bit successive approximation device with integral sample-and-hold and a output data latch. Each conversion takes 10.05 µsec. A conversion is initiated by 2.0 µsec sample command, during which the sample-and-hold is in the sample mode and the converter clock is inactive. In the remaining 8.05 µsec following the end of the sample command, the sample-and-hold switches to hold, and the converter digitizes the analog sample with 17 toggles of the converter clock. Following the rising edge of the 17th clock, a 16-bit output data latch is updated to the digital representation of the sampled analog signal. The output latch will then maintain this digital word until the completion of the next conversion. Figure 1-1 on page 30 shows the VMIPCI-3322 autoscan timing, which focuses on the ADC timing.

The combination of the sample-and-hold and the output data latch permits pipelining of the conversion cycle. Once the sample-and-hold has switched to hold and the ADC begins the conversion process, the input Multiplexer and Instrumentation Amplifier are switched to the next channel to slew and settle. Likewise, the result of each conversion is not written into the SRAM until the ADC is digitizing the next sample.

The ADC contains a self-calibration feature to achieve and maintain the 16-bit accuracy. Upon system reset or a software issued reset, a calibration signal is asserted to the ADC. Then for the next 85,530 converter clock cycles (approximately 41 milliseconds), the ADC performs a self-calibration. The ADC Calibration Busy Flag is available in the Status Register if needed.

Timing and Control Circuitry

All timing and control circuitry is located in a single EPLD device. This includes the Control / Status Register (CSR), the state machine, the signal lines that controls PCI bus accesses, the state machine signal lines that controls the analog MUX switching, ADC conversion, and the circuitry involved with ADC calibration timing. Figure 1-1 on page 30 shows the VMIPCI-3322 autoscan timing.

Control and Status Register (CSR)

The Control and Status Register is accessible through any even relative addresses $0 through $E. The control register has only 7 of the possible 16 bits used. Three of four bits control the Fail LED, the software reset, and the autoscan enable. A fourth control bit selects the data format between two's complement or straight / offset binary. The fifth control bit is a self-test flag, which only echoes back into the Status Register. The last two active control bits select the number of channels to autoscan. The remaining 9 bits in the control word are reserved and should be written as "zero". Any PCI bus read of relative addresses $0 through $E yields a status word. The status word echoes back the corresponding control register bits and also contains a calibration busy bit. The unused status word bits are reserved and read as zero.

SRAM Arbitration

The possibility of both the autoscan state machine and the PCI bus attempting to access the SRAM at the same time does exist. The timing and control circuitry includes arbitration logic to prevent such access collisions from causing erroneous operation. Either of the two that the start second access is delayed until the first access is complete. If the PCI bus access is the latter, the delay might cause access to exceed a 16 PCI bus clock limit. In that event, the PCI bus interface device issues a PCI bus "retry" request and the PCI bus controller repeats the access. The retry process is, for the most part, transparent to the user. Also, regardless of the arbitration, the overall autoscan timing is unaffected.

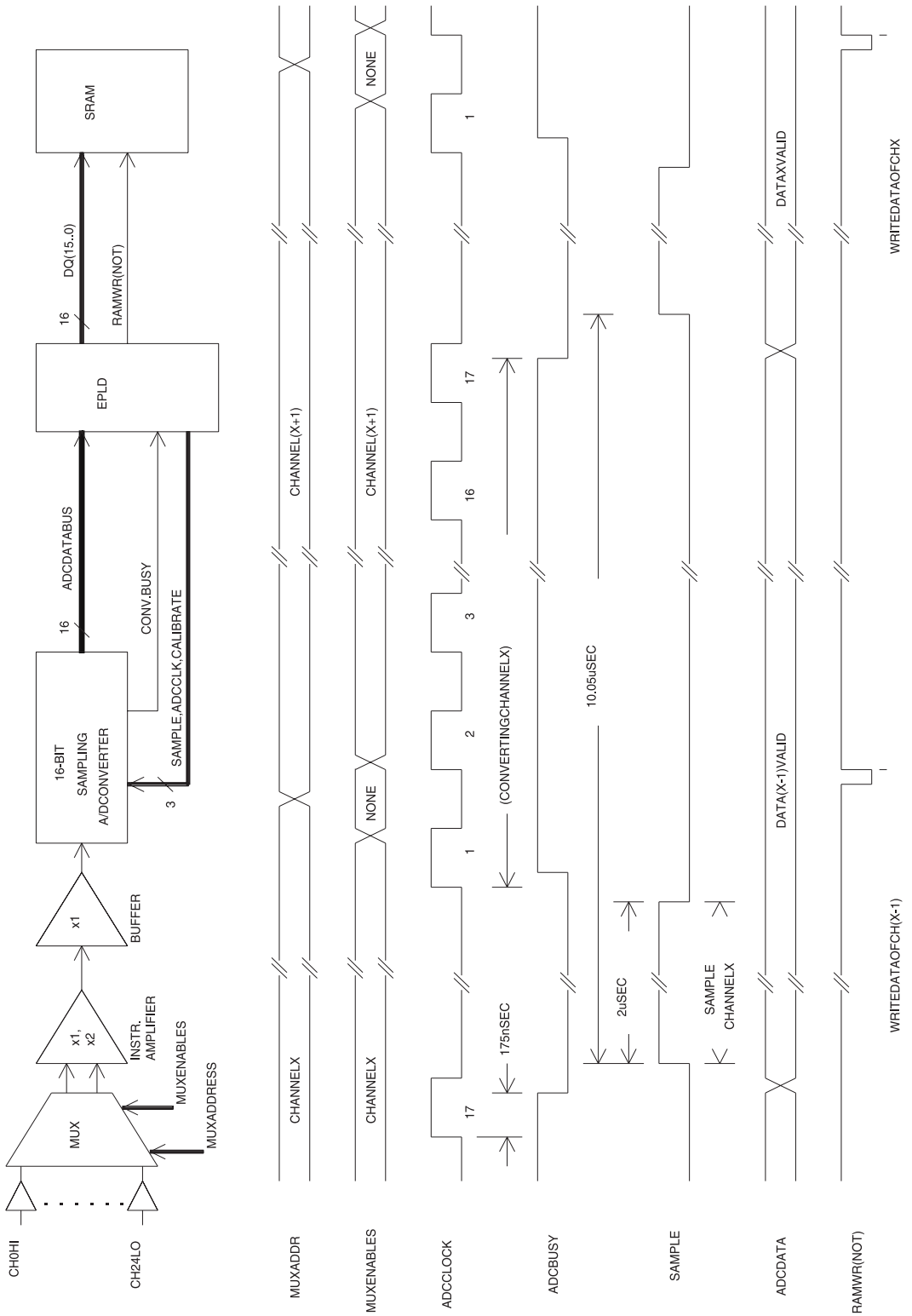


Figure 1-1 VMIPCI-3322 Timing Diagram

CHAPTER
2

Configuration and Installation

Contents

Introduction

The VMIPCI-3322 is designed to operate on the industrial standard 5 V PCI local bus, and supports up to 24 channels of differential or single-ended inputs within the full-scale range of ±2.5 to ±10 V. The board continuously scans the selected inputs, converts each sample to a digital value, and stores the results in dual-ported data registers. The data format of channels scanned is program-selectable between straight / offset binary and two's complement.

The VMIPCI-3322 converts at an aggregate rate of 99.5 kHz. The individual channel sample rate is 99.5 kHz divided by the number of channels scanned.

Unpacking Procedures

Caution Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that may have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. This board can be installed in any slot position with a circle above the handle and also on the backplane, the slot with a triangle above the handle is reserved for the system controller.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides.

Caution Do not install or remove the board while power is applied.

WARNING Prior to installing the board, verify that the jumpers are configured as described in the "Operational Configuration" section on page 35.

1. Remove the PC housing cover. Refer to your PC manual(s) for details. PCI bus systems can conform to one of several standards based on either 5 or 3.3 V operation and based on a 32-or a 64-bit PCI bus. The PCI bus motherboard receptacles are keyed and the PCI bus card edge connectors are slotted to ensure compatibility. The VMIPCI-3322 was designed for a 5 V, 32-bit PCI bus system. However, it is also compatible with a 5 V, 64-bit PCI bus system. Refer to your host computer's manual(s) for information on compatible PCI bus card types. In addition, examine the PCI bus receptacle into which the VMIPCI-3322 is to be installed. Verify that the location of the key in the PCI bus receptacle corresponds to the slot in the card edge connector.
2. Remove the blank back panel mounting bracket corresponding to the PCI bus slot into which the VMIPCI-3322 is to be installed.
3. Insert the VMIPCI-3322 card edge connector into the desired PCI bus receptacle and install the retaining screw in the rear support bracket.

Before Applying Power: Checklist

1. Have the chapters pertaining to "Theory of Operation" and "Programming", Chapters 1 and 3, been reviewed and applied?
2. Have the jumpers as described in the section titled "Factory-Installed Jumpers" been installed correctly?
3. Has the I/O cable with the proper mating connector been installed in I/O port P1? Refer to the section titled "Connector Descriptions" for a description of compatible mating connectors.
4. Calibration has been performed at the factory. If recalibration should be required, refer to the section titled "Calibration".

Operational Configuration

As with other PCI bus cards, the I/O and Memory address space, through which the VMIPCI-3322 operates, is assigned dynamically by the PC system BIOS and is not predefined by jumpers. The VMIPCI-3322 does contain four jumpers that define the input range and type. Location and function of the VMIPCI-3322 jumpers are shown in Figure 2-1 on page 36 and listed in Table 2-1 below.

Table 2-1 Programmable Jumper Functions

Jumper	Function When Installed	Factory Conf.
J1: pins 1,2	±2.5 V, 0 to 5 V, ±5 V, 0 to +10 V Ranges	Omitted
J1: pins 2,3	±10 Range	Installed
J2: pins 1,2	Bipolar Operation	Installed
J2: pins 2,3	Unipolar Operation	Omitted
J3: pins 1,2	Instrumentation Amp. (x2) multiplier (paired with J4)	Omitted
J4: pins 1,2	Instrumentation Amp. (x2) multiplier (paired with J3)	Omitted

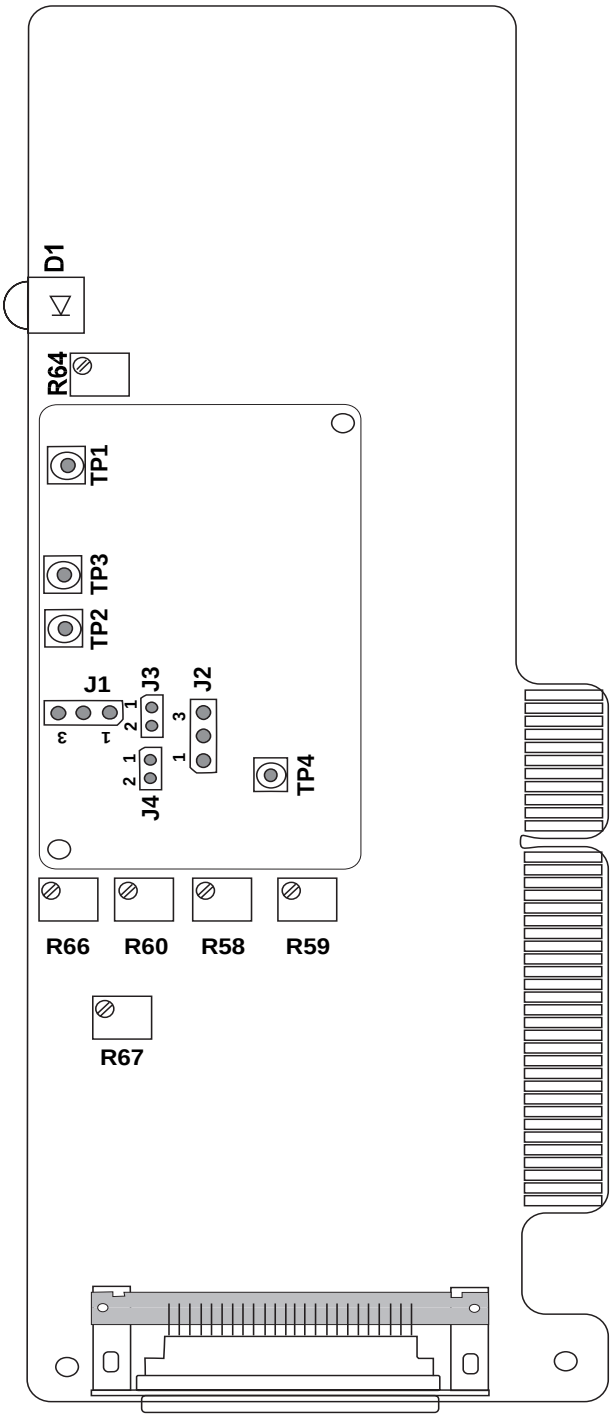


Figure 2-1 Location of Test Points, Potentiometers, and Jumpers

Factory-Installed Jumpers

Each VMIPCI-3322 board is configured at the factory with a specific jumper arrangement as shown in Table 2-1 on page 35. The factory configuration establishes the following functional baseline for the VMIPCI-3322 board, and ensures that all essential jumpers are installed.

- ±10 V input range
- Differential inputs

The VMIPCI-3322 has an RF Shield covering the jumpers and test points. The shield must be removed before configuration of the jumpers is possible. Figure 2-2 illustrates the removal and installation of the RF Shield:

Caution Do not install or remove the RF Shield while power is applied.

1. Using a #1 Phillips Screwdriver, remove the two Phillips Head Screws holding the RF Shield to the PC board.
2. Carefully remove the shield from the PC board. To install the shield, reverse the order that the shield was removed.

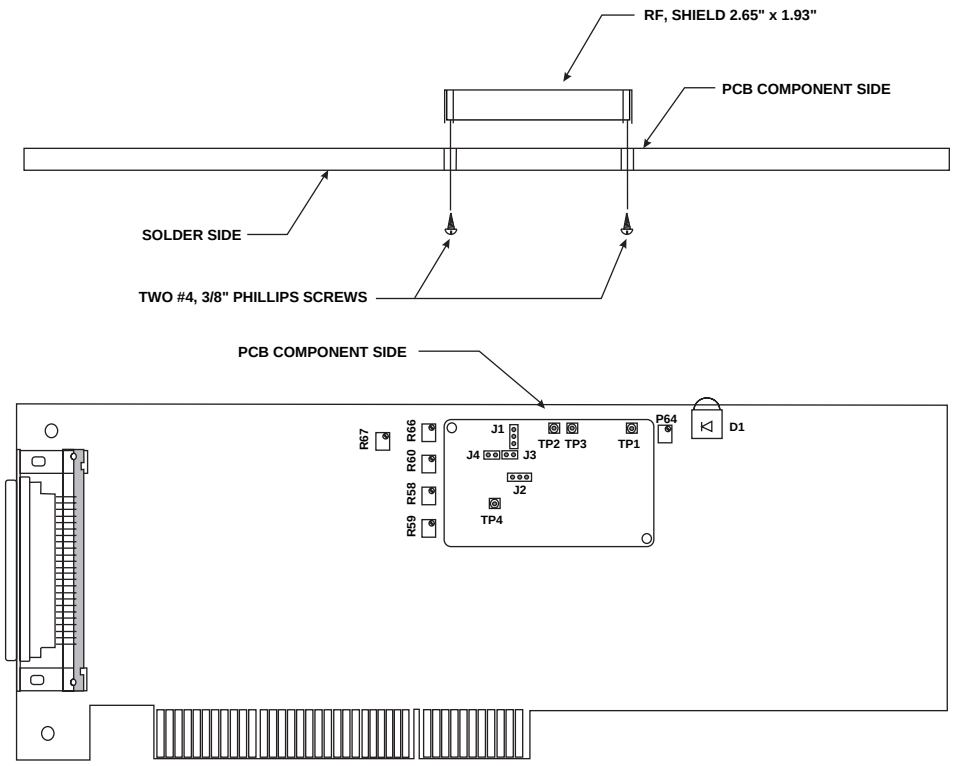


Figure 2-2 RF Shield Installation and Removal

Conversion Range Selection

The conversion range of the VMIPCI-3322 is set through the jumper combinations shown in Table 2-2. See Figure 2-1 on page 36 for jumper locations.

Table 2-2 Conversion Range Selection

Jumper	Input Voltage Range				
	±10 V	±5 V	±2.5 V	0 to +10 V	0 to +5 V
J1	2,3	1,2	1,2	1,2	1,2
J2	1,2	1,2	1,2	2,3	2,3
J3	Removed	Removed	Installed	Removed	Installed
J4	Removed	Removed	Installed	Removed	Installed

Input Configuration

The analog inputs are configured as single-ended or differential by the factory installation of resistor networks. Each active input, both HIGH and LOW, are referenced to the on-board analog ground through a 22 MΩ resistor. The 22 MΩ resistors provide floating input protection while still maintaining high input impedance. In addition, each active input has a 3.9 kΩ series resistor to limit current in overvoltage conditions and to partially implement the input low pass filter. When the inputs are configured as single-ended, the 3.9 kΩ series resistor in the LOW input paths are omitted and, instead, the LOW paths are tied to analog ground through separate resistor networks. When the board is configured in the single-ended mode, the P1 connector pins corresponding to LOW inputs are not connected to any board circuitry.

Calibration

Before delivery from the factory, the VMIPCI-3322 board is fully calibrated and conforms to all factory specifications. However, should recalibration be required perform the appropriate procedures on the following pages, using the test equipment listed below. The locations of all adjustments and test points are shown in Figure 2-1 on page 36. Adjustment potentiometers and their functions are listed in Table 2-3 below.

Table 2-3 Adjustment Potentiometers

Potentiometers	Function
R58	Gain Adjustment
R59	Instrumentation Amp: Input common-mode trim
R60	Instrumentation Amp: Output common-mode trim
R64	Offset Adjustment
R66	+10.0 VDC Reference Adjustment
R67	+5.0 VDC Reference Adjustment

Equipment Required

1. **Digital Multimeter (DMM):** ±1.00000 and ±10.0000 VDC ranges; 6 or more digits; ±0.003 percent of reading voltage measurement accuracy; 10 MΩ minimum input impedance.
2. **Digital Voltage Source:** 10.0000 VDC ±0.0001 VDC voltage source, 7-digit setting resolution and ±0.003 percent accuracy, 10 Ω maximum source resistance.
3. **PCI bus Host System:** The PCI bus Host System requires a minimum of one open PCI bus slot, capable of accommodating a full-sized PCI bus board, one 3.5-inch floppy diskette drive and interface, a monitor, a keyboard, and the associated power supply.
4. **PCI bus Extender Board:** Depending on the configuration of the PCI bus host system, it may be necessary to use a PCI bus extender board to assure access to the adjustment potentiometers.
5. **Test Cables:** Test leads for the equipment listed above. Three short (not longer than 6 inches) test leads with mini-clips or alligator clips on both ends.
6. **Test Adapter:** A 50-pin D-shell male connector with the high inputs of all 24 channels tied together and the low inputs of all 24 channels tied together and the two AGND inputs tied together. The group of high inputs tied together will be called the “high side” and the group of low inputs tied together will be called the “low side”. An illustration of the test adapter is shown in Figure 2-3 on page 40.
7. **Test Software:** A test routine which repeatedly reads the Adds results of 96 or more conversions, displays an average, and deviation spread is the preferred means of calibration. As shown in Table 3-1 on page 58, the ADCs results are located in the SRAM at relative addresses $12 through $3E. Lacking a software routine of this caliber, a software routine which repeatedly displays the results of all 24 input conversions at a rate of 1 or 2 times per second is suggested. The user must then estimate the average.

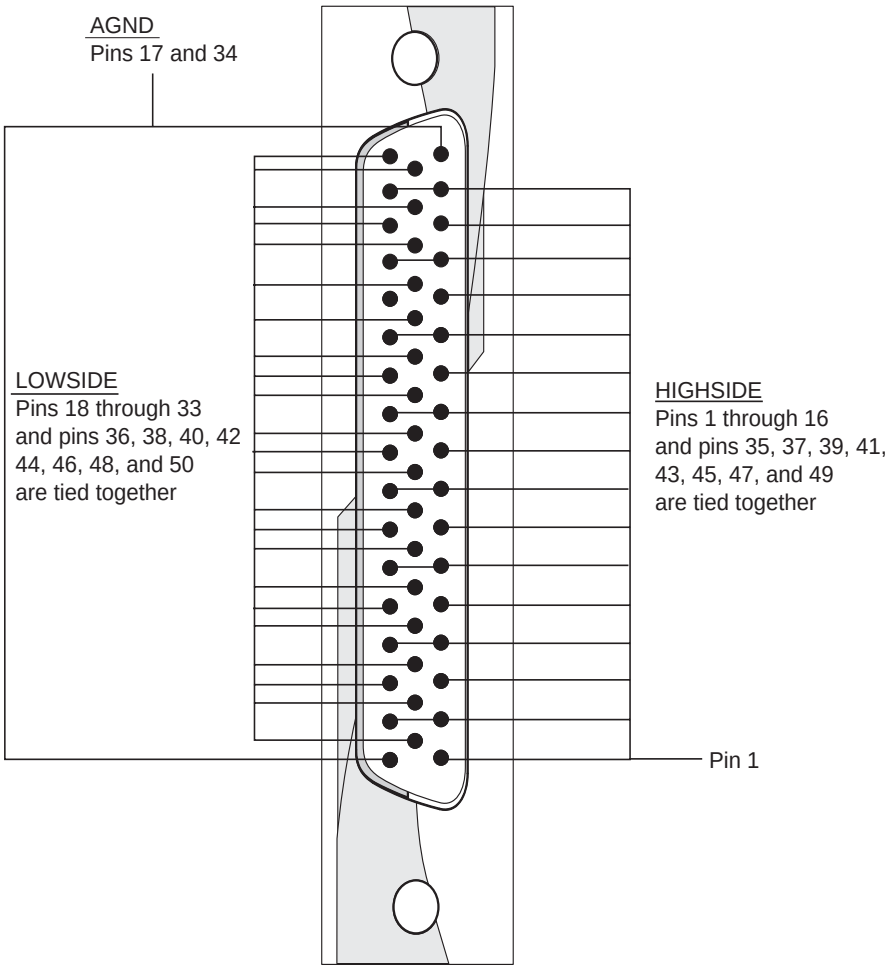


Figure 2-3 Test Adapter

Note This Test Adapter, for use when calibration of the VMIPCI-3322 is required. This adapter is not supplied by VMIC and must be built by the user.

Base Address Determination

With the VMIPCI-3322 installed in the PCI bus Host System, using a protected-mode debugger or equivalent software for calibration, “find” where in the short I/O or Memory space the system BIOS has located the VMIPCI-3322 Base Address Register 1 or 2. The three parameters required to find the base addresses are the VENDOR ID ($114A), the DEVICE ID ($3322), and the REV ID, which is C0h. Base Address Register 1 (if I/O mapped) or Base Address Register 2 (if Memory mapping is used) and the information in Table 3-1 on page 56 establishes the location of the CSR and SRAM locations which are necessary to operate this board. All addresses stated in the following sections are relative addresses in relation to the base address in the Base Address Register 1 or 2.

Calibration Procedures

The following sections provide calibration procedures for all the input voltage ranges of the VMIPCI-3322. In the following procedures, the Fail LED Off bit is set to a logical “1” and the TWOCOMP bit is set to a logical “0”, so the output format is offset or straight binary.

Refer to the following sections for the specific calibration procedure:

±10 V Input Range	Refer to "Calibration Procedure for ± 10 V Input Range" section on page 41.
±5 V Input Range	Refer to "Calibration Procedure for ± 5 V Input Range" section on page 43.
±2.5 V Input Range	Refer to "Calibration Procedure for ± 2.5 V Input Range" section on page 44.
0 to 10 V Input Range	Refer to "Calibration Procedure for 0 to +10 V Input Range" section on page 46.
0 to 5 V Input Range	Refer to "Calibration Procedure for 0 to +5 V Input Range" section on page 48.

Note Calibration of the board to a specific range does not ensure the board shall remain calibrated if the jumpers are then reconfigured.

Calibration Procedure for ± 10 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the ±10 V input range as shown in Table 2-2 on page 38.
2. Install the board in a PCI bus host system, using the PCI bus extender board if necessary.
3. Install the test adapter on the P1 input connector (see Figure 2-3 on page 40).
4. Apply power to the PCI bus host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted-up and the test software routines may be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input channel 0 remains selected and enabled, through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP3(+) and TP1(-). (See Figure 2-1 on page 36.)
2. Adjust potentiometer R66 for a DMM reading of +10.0000 ±0.00015 VDC.

Common Mode-Adjustments:

Perform the following steps to adjust the Common-Mode Voltage:

1. Program the voltage source for 0.00000 VDC.
2. Connect both the high side and the low side of the test adapter to the (+) lead of the voltage source. Connect the (-) lead of the voltage source to the AGND inputs of the test adapter.
3. Connect the DMM (+) lead to jumper J3 pin 1 and connect the DMM (-) lead to jumper J4 pin 2.
4. Record the DMM reading while the voltage source remains at 0.00000 VDC.
5. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R59 to obtain the minimum variation in the DMM reading of ±0.00005 VDC. Disconnect the DMM when finished.
6. Write $A000 to the CSR at relative address 0. (This sets the Fail LED off and sets SCANENA high.) Then start the software routine which repeatedly displays the average or the results of all 24 input conversions.
7. Set the voltage source to 0.00000 VDC, and record the average of the readings. The average should be a value close to $8000.
8. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R60 to obtain the minimum variation in the average of readings. Less than 1 LSB variation in the average reading should be attainable.

Offset Adjustment:

Perform the following steps to adjust the Offset:

1. Disconnect the voltage source from the test adapter. Tie all three of the input sides together. The high side, the low side, and the AGND test adapter inputs should be tied together using test clips.
2. Start the software routine, which repeatedly displays the average or results from all 24 inputs.
3. Adjust potentiometer R64 so that the average reading is $8000.
4. Remove the test clips that tie the test adapter inputs together.

Gain Adjustment:

Perform the following steps to adjust the Gain:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side input and the AGND inputs of the test adapter.
2. Set the voltage source to -9.99512 VDC.
3. Adjust potentiometer R58 so that the average reading is $000F.
4. Set the voltage source to +9.99511 VDC, and verify that the average reading is $FFF0 ±1.
5. Repeat the previous three steps until both averages are within the tolerance.

6. Remove the voltage source and the test adapter.
7. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for ± 5 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the ±5 V input range as shown in Table 2-2 on page 38.
2. Install the board in a PCI bus host system, using the PCI bus extender board if necessary.
3. Install the test adapter onto the P1 input connector.
4. Apply power to the PCI bus host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted-up and the test software routine can be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, Input channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP3(+) and TP1(-). (See Figure 2-1 on page 36.)
2. Install jumper J1 between pins 2 and 3.
3. Adjust potentiometer R66 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper J1 between pins 1 and 2.
5. Adjust potentiometer R66 for a DMM reading of +4.99950 ±0.00005 VDC.

Common-Mode Adjustments:

Perform the following steps to adjust the Common-Mode Voltage:

1. Program the voltage source for 0.00000 VDC.
2. Connect the voltage source (+) lead to both the high and low sides of the test adapter. Connect the (-) lead of the voltage source to the AGND input of the test adapter.
3. Connect the DMM (+) lead to jumper J3 pin 1 and connect the DMM (-) lead to jumper J4 pin 2.
4. Record the DMM reading while the voltage source remains at 0.00000 VDC.
5. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R59 to obtain the minimum variation in the DMM readings of ±0.00005 VDC. Disconnect the DMM when finished.
6. Write $A000 to the CSR at relative address 0. This sets the Fail LED off and sets SCANENA high. Then start the routine which repeatedly displays the average or the results of all 24 input conversions.
7. Set the voltage source to 0.00000 VDC, and record the average of the reading which results. The average should be a value close to $8000.

8. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R60 to obtain the minimum variation in the average readings. A variation in the average of ±1 LSB or less should be attainable.

Offset Adjustment:

Perform the following steps to adjust the Offset:

1. Disconnect the voltage source from the test adapter. Tie all three inputs together. The high side, the low side, and the AGND test adapter inputs should be tied together using test clips.
2. Start the software routine, which repeatedly displays the average or results from all 24 inputs.
3. Adjust potentiometer R64 so that the average reading is $8000.
4. Remove the test clips that ties the test adapter inputs together.

Gain Adjustment:

Perform the following steps to adjust the Gain:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side input and the AGND inputs of the test adapter.
2. Set the voltage source to -4.99756 VDC.
3. Adjust potentiometer R58 so that the average reading is $000F.
4. Set the voltage source to +4.99756 VDC and verify that the average reading is $FFF0 ±1.
5. Repeat the previous three steps until both averages are within tolerance.
6. Remove the voltage source and the test adapter.
7. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for ± 2.5 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the ±2.5 V input range as shown in Table 2-2 on page 38.
2. Install the board in a PCI bus host system, using the PCI bus extender board if necessary.
3. Install the test adapter onto the P1 input connector.
4. Apply power to the PCI bus host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted up and the test software routine can be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP3(+) and TP1(-). (See Figure 2-1 on page 36.)
2. Install jumper on J1, between pins 2 and 3.
3. Adjust potentiometer R66 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper on J1, between pins 1 and 2.
5. Adjust potentiometer R66 for a DMM reading of +4.99950 ±0.00005 VDC.

Common Mode Adjustments:

Perform the following steps to adjust the Common-Mode Voltage:

1. Program the voltage source for 0.00000 VDC.
2. Temporarily remove jumpers J3 and J4.
3. Connect the (+) lead of the voltage source to both the high and low sides of the test adapter. Connect the (-) lead of the voltage source to the AGND input of the test adapter.
4. Connect the DMM (+) lead to the jumper J3 pin 1 and connect the DMM (-) lead to jumper J4 pin 2.
5. Record the DMM reading while the voltage source remains at 0.00000 VDC.
6. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R59 to obtain the minimum variation in the DMM reading of ±0.00005 VDC. Disconnect the DMM when finished.
7. Re-install jumpers J3 and J4.
8. Write $A000 to the CSR at relative address 0. This sets the Fail LED off and sets SCANENA high. Start the software routine which repeatedly displays the average or the results of all 24 input conversions.
9. Set the voltage source to 0.00000 VDC and record the average results. The average should be a value close to $8000.
10. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R60 to obtain the minimum variation in the average readings. A variation in the average of ±1 LSB or less should be attainable.

Offset Adjustment:

Perform the following steps to adjust the Offset:

1. Disconnect the voltage source from the test adapter. On the test adapter, tie all three inputs together. The high side, the low side, and the AGND test adapter inputs should be tied together using test clips.
2. Start the software routine, which repeatedly displays the average or results from all 24 inputs.
3. Adjust potentiometer R64 so that the average reading is $8000.
4. Remove the test clips that tie the test adapter inputs together.

Gain Adjustment:

Perform the following steps to adjust the Gain:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side input and the AGND inputs of the test adapter.
2. Set the voltage source to -2.49878 VDC.
3. Adjust potentiometer R58 so that the average reading is $000F.
4. Set the voltage source to +2.49878 VDC and verify that the average reading is $FFF0 ±3.
5. Repeat the previous three steps until both averages are within the tolerance.
6. Remove the voltage source and the test adapter.
7. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for 0 to +10 V Input Range

Setup:

Perform the following steps to initialize the setup:

1. Configure the jumpers for the 0 to +10 V input range as shown in Table 2-2 on page 38.
2. Install the board in a PCI bus host system, using the PCI bus extender board if necessary.
3. Connect the test adapter onto the P1 input connector.
4. Apply power to the PCI bus host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system may be to booted up and the test software routine can be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

Perform the following steps to adjust the ADC Reference Voltage:

1. Connect the DMM between TP3(+) and TP1(-). (See Figure 2-1 on page 36.)
2. Install jumper J1, between pins 2 and 3.
3. Adjust potentiometer R66 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper J1, between pins 1 and 2.
5. Adjust potentiometer R66 for a DMM reading of +4.99950 ±0.00005 VDC.

Common Mode Adjustments:

1. Program the voltage source for 0.00000 VDC.
2. Connect the (+) lead of the voltage source to both the high and the low sides of the test adapter. Connect the (-) lead of the voltage source to the AGND input of the test adapter.
3. Connect the DMM (+) lead to jumper J3 pin 1 and connect the DMM (-) lead to jumper J4 pin 2.
4. Record the DMM reading while the voltage source remains at 0.00000 VDC.
5. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R59 to obtain the minimum variation in the DMM reading of ±0.00005 VDC. Disconnect the DMM when finished.
6. Write $A000 to the CSR at relative address 0. This sets the Fail LED off and sets SCANENA high. Then start the software routine which repeatedly displays the average or the results of all 24 input conversions.
7. Set the voltage source to 0.00000 VDC and adjust R64 for an average reading of $10.
8. Alternate the voltage source from +10.000 to -10.000 VDC by adjusting potentiometer R60 to obtain the minimum variation in the average readings between the two common-mode extremes. A variation in the average of ±1 LSB or less should be attainable.
9. Set the voltage source to 0.0000 VDC and disconnect it from the test adapter.

Offset Adjustment:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side and the AGND inputs of the test adapter.
2. Set the voltage source for +5.0000 VDC.
3. Start the software routine, which repeatedly displays the average or results from all 24 inputs.
4. Adjust potentiometer R64 so that the average reading is $8000.

Gain Adjustment:

1. Set the voltage source to 0.002441 VDC.
2. Adjust potentiometer R58 so that the average reading is $000F.
3. Set the voltage source to +9.99756 VDC and verify that the average readings is $FFF0 ±1.
4. Repeat the previous three steps until both averages are within tolerance.
5. Remove the voltage source and the test adapter.
6. Calibration is complete. Turn power OFF before removing the board.

Calibration Procedure for 0 to +5 V Input Range

Setup:

1. Configure the jumpers for the 0 to +5 V input range as shown in Table 2-2 on page 38.
2. Install the board in a PCI bus host system, using the PCI bus extender board if necessary.
3. Connect the test adapter to the P1 input connector.
4. Apply power to the PCI bus host system. Allow a minimum warm-up interval of ten minutes before proceeding. During the warm-up interval, the system can be booted up, and the test software routine can be loaded.
5. Write $4000 to the CSR at relative address 0. This issues a software reset to the board. After a software reset and until SCANENA is enabled, input channel 0 remains selected and enabled through to the ADC input.

ADC Reference Adjustment:

1. Connect the DMM between TP3(+) and TP1(-). (See Figure 2-1 on page 36)
2. Install jumper J1, pins 2 and 3.
3. Adjust potentiometer R66 for a DMM reading of +10.0000 ±0.00015 VDC.
4. Install jumper J1, pins 1 and 2.
5. Adjust potentiometer R66 for a DMM reading of +4.99950 ±0.00005 VDC.

Common-Mode Adjustments:

1. Program the voltage source for 0.00000 VDC.
2. Temporarily remove jumpers J3 and J4.
3. Connect the (+) lead of the voltage source to both the high and low sides of the test adapter. Connect the (-) lead of the voltage source to the AGND input of the test adapter.
4. Connect the DMM (+) lead to the jumper J3 pin 1 and connect the DMM (-) lead to jumper J4 pin 2.
5. Record the DMM reading while the voltage source remains at 0.00000 VDC.
6. Alternate the voltage source from +10.000, 0.0000, and -10.000 VDC by adjusting potentiometer R59 to obtain the minimum variation in the DMM reading of ±0.00005 VDC. Disconnect the DMM when finish.
7. Re-install jumpers J3 and J4.
8. Write $A000 to the CSR at relative address 0. This sets the Fail LED off and sets SCANENA high. Then start the software routine, which repeatedly displays the average or the results of all 24 input conversions.
9. Set the voltage source to 0.00000 VDC and adjust R64 for an average reading of $10.

10. Alternate the voltage source from +10.000 to -10.000 VDC by adjusting potentiometer R60 to obtain the minimum variation in the average readings between the two common-mode extremes. A variation in the average of ±1 LSB or less should be attainable.
11. Set the voltage source to 0.0000 VDC and disconnect it from the test adapter.

Offset Adjustment:

1. Connect the (+) lead of the voltage source to the high side input of the test adapter. Connect the (-) lead of the voltage source to both the low side and the AGND inputs of the test adapter.
2. Set the voltage source for +2.5000 VDC.
3. Start the software routine, which repeatedly displays the average or results from all 24 inputs.
4. Adjust potentiometer R64 so that the average reading is $8000.

Gain Adjustment:

1. Set the voltage source to 0.001221 VDC.
2. Adjust potentiometer R58 so that the average reading is $000F.
3. Set the voltage source to +4.99878 VDC and verify that the average readings is $FFF0 ±1.
4. Repeat the previous three steps until both averages are within the tolerance.
5. Remove the voltage source and the test adapter.

Calibration is complete. Turn power OFF before removing the board.

Connector Descriptions

The VMIPCI-3322 has two connectors, P1 and P2. P1 is the external I/O connector and is located on the rear mounting bracket. P2 is the PCI bus card edge connector.

PCI Bus Connector (P2)

PCI bus motherboard receptacles are keyed and the PCI bus card edge connectors are slotted to ensure compatibility. The VMIPCI-3322 was designed for a 5 V, 32-bit PCI bus system. However, it is also compatible with a 5 V, 64-bit PCI bus system. Refer to your host computer's manual(s) for information on compatible PCI bus card types. The pin with a reference designation "B1" is located on the component side of the board and is the pin closest to the rear mounting bracket. Likewise, the pin "A1" is located on the back side of the board and is the pin closest to the rear mounting bracket.

I/O Connector (P1)

The P1 connector is a 50-pin D-shell subminiature receptacle. Table 2-4 on page 51 details the signal/pin assignment, and Figure 2-4 on page 51 provides a view of the connector.

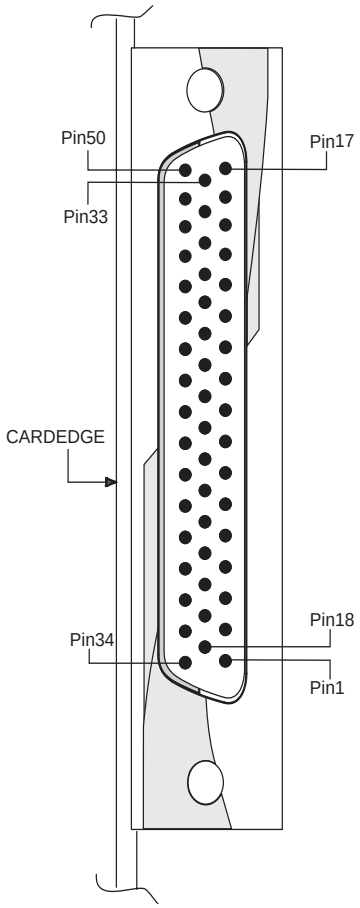


Figure 2-4 P1 I/O Connector

Table 2-4 P1 Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	CHH0	CH0 High	31	CHL19	CH19 Low
2	CHH1	CH1 High	32	CHL21	CH21 Low
3	CHH3	CH3 High	33	CHL22	CH22 Low
4	CHH4	CH4 High	34	AGND	Analog GND
5	CHH6	CH6 High	35	CHH2	CH2 High
6	CHH7	CH7 High	36	CHL2	CH2 Low
7	CHH9	CH9 High	37	CHH5	CH5 High
8	CHH10	CH10 High	38	CHL5	CH5 Low
9	CHH12	CH12 High	39	CHH8	CH8 High
10	CHH13	CH13 High	40	CHL8	CH8 Low
11	CHH15	CH15 High	41	CHH11	CH11 High
12	CHH16	CH16 High	42	CHL11	CH11 Low
13	CHH18	CH18 High	43	CHH14	CH14 High
14	CHH19	CH19 High	44	CHL14	CH14 Low
15	CHH21	CH21 High	45	CHH17	CH17 High
16	CHH22	CH22 High	46	CHL17	CH17 Low
17	AGND	Analog GND	47	CHH20	CH20 High
18	CHL0	CH0 Low	48	CHL20	CH20 Low
19	CHL1	CH1 Low	49	CHH23	CH23 High
20	CHL3	CH3 Low	50	CHL23	CH23 Low
21	CHL4	CH4 Low			
22	CHL6	CH6 Low			
23	CHL7	CH7 Low			
24	CHL9	CH9 Low			
25	CHL10	CH10 Low			
26	CHL12	CH12 Low			
27	CHL13	CH13 Low			
28	CHL15	CH15 Low			
29	CHL16	CH16 Low			
30	CHL18	CH18 Low			

System Considerations

Input Filter Selection

The VMIPCI-3322 offers four factory installed Low Pass Filter options, which are no filter, 50, 100, and 500 Hz. Selection of the proper filter should be based on knowledge of the input signal characteristics and expected system noise. Selection of a lower frequency filter will increase the attenuation of high-frequency noise, but should also lower the maximum frequency of the signal that can be accurately converted.

Input Cables

Optimum performance is usually obtained if the input cables consist of individually twisted and shielded pairs. Short of individual shielded pairs, twisted pairs with a group or bundle shield is recommended. P1 pins 17 and 34, serve to tie cable shields to the board AGND as well as providing a ground reference for the external signal sources.

General Guidelines

The grounding scheme used can have a major affect on system performance. Each system has its own unique interface considerations, but the following general guidelines will apply in most cases.

Long Input Lines:

Long input lines (greater than 10 feet), or inputs from grounded sources (sources which are not floating), should be connected to differential inputs. The overall shields should be extended from the input source to as close to the board as possible. Single-ended inputs are susceptible to ground loop errors, and should be used only with high-level floating sources.

Source Impedance:

Use a signal source with the lowest available impedance. Susceptibility to crosstalk and induced interference increases as the source impedance increases.

Floating Signal Sources:

The shield from a floating signal source (RTD, strain gage, etc.,) should be connected to the LOW (negative) terminal at the source. For low-impedance sources (less than 10), or for sources which are protected from interference fields, connect the board end of the shield to analog return (AGND) at the board. For high-impedance sources, connect all shielded terminals of the source together, and leave the board ends of the shields open.

Grounded Signal Sources:

Outputs of grounded sources (sources which are not floating) must be referenced to a common ground, which ensures that the input voltage will not exceed the input range (±10 V) of the board. Shields from grounded sources should be connected to LOW terminal of the sources, and left open at the board.

Unused Inputs:

Unused inputs within each group of eight channels (0 through 7, 8 through 15, etc.,) should be connected to a common ground to avoid interference with active channels. Grounding of unused groups of 8 channels is not essential, but will assist in minimizing susceptibility to system noise.

CHAPTER

3

Programming

Contents

Introduction

As described in the "Theory of Operation", the Base Address Register 1 and 2 contain the starting I/O and memory mapped address at which the VMIPCI-3322 registers are located. This address is assigned by the system BIOS during the boot process (See . Starting at the base address, the VMIPCI-3322 reserves the next 128 consecutive byte addresses. Of these addresses, only the even addresses are used due to 16-bit configuration of the VMIPCI-3322. The first 8 even addresses, $0 through $E, access the CSR. The next 32 even addresses, $10 through $4E, access the SRAM. The remaining addresses, $50 through $7F, are reserved. Table 3-1 on page 56 details the VMIPCI-3322 memory map.

Note Writing to Base Address Register 1 automatically updates Base Address Register 2 and vice versa.

PCI bus Operation Registers

Base Address Register 0 contains a 32-bit address, which points to a group of 16 DWORD (32-bit) registers. These registers are called the PCI Bus Operation Registers and they are not involved in the basic VMIPCI-3322 operation.

Table 3-1 VMIPCI-3322 Memory Map

Relative Address (Hex)	Function	Access
00 through 0E	Control and Status (CSR)	Read / Write
10	SRAM Location 0 (Analog Input Channel 0 Data)	Read / Write
12	SRAM Location 1 (Analog Input Channel 1 Data)	Read / Write
14	SRAM Location 2 (Analog Input Channel 2 Data)	Read / Write
16	SRAM Location 3 (Analog Input Channel 3 Data)	Read / Write
18	SRAM Location 4 (Analog Input Channel 4 Data)	Read / Write
1A	SRAM Location 5 (Analog Input Channel 5 Data)	Read / Write
1C	SRAM Location 6 (Analog Input Channel 6 Data)	Read / Write
1E	SRAM Location 7 (Analog Input Channel 7 Data)	Read / Write
20	SRAM Location 8 (Analog Input Channel 8 Data)	Read / Write
22	SRAM Location 9 (Analog Input Channel 9 Data)	Read / Write
24	SRAM Location 10 (Analog Input Channel 10 Data)	Read / Write
26	SRAM Location 11 (Analog Input Channel 11 Data)	Read / Write
28	SRAM Location 12 (Analog Input Channel 12 Data)	Read / Write
2A	SRAM Location 13 (Analog Input Channel 13 Data)	Read / Write
2C	SRAM Location 14 (Analog Input Channel 14 Data)	Read / Write
2E	SRAM Location 15 (Analog Input Channel 15 Data)	Read / Write
30	SRAM Location 16 (Analog Input Channel 16 Data)	Read / Write
32	SRAM Location 17 (Analog Input Channel 17 Data)	Read / Write
34	SRAM Location 18 (Analog Input Channel 18 Data)	Read / Write
36	SRAM Location 19 (Analog Input Channel 19 Data)	Read / Write
38	SRAM Location 20 (Analog Input Channel 20 Data)	Read / Write
3A	SRAM Location 21 (Analog Input Channel 21 Data)	Read / Write
3C	SRAM Location 22 (Analog Input Channel 22 Data)	Read / Write
3E	SRAM Location 23 (Analog Input Channel 23 Data)	Read / Write
40 through 4E	SRAM Locations 24 through 31 (Spare)	Read / Write
50 through 7E	Reserved	Read / Write

Control and Status Register Description

Control Register Bit Assignments

Only 7 of the 16 possible data bits in the Control register have assigned functions. Those functions are detailed in Table 3-2 below:

Table 3-2 Control Register Bit Map

Control Register (Offset 00 through 0E) Write Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED_OFF	SOFT_RST	SCANENA	TWOCOMP	Reserved	SCANSIZ1	SCANSIZ0	Reserved

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved							

Control Register Bit Definitions

Bit 15, LED_OFF: The Fail LED is mounted along the top edge of the board and is only visible when the host computer's chassis cover is removed. Therefore, the LED may only be useful during initial installation and verification. The LED is turned ON by writing a logical "0", the user can extinguish the LED by writing a logical "1" to this bit.

Bit 14, SOFT_RST: The Software Reset, resets all sections of the timing and control EPLD, including the CSR itself. The Software Reset is immediate and will interrupt any current autoscan cycle. The reset duration lasts 60 nsec and an ADC calibration cycle occurs following the reset. After the Software Reset, the ADC performs a self-calibration which takes approximately 41 milliseconds. Set this bit to a "1" to initiate a software reset. The SRAM is not affected by a software reset, and is initialized, if necessary, by PCI write cycles.

Bit 13, SCANENA: Upon any reset the SCANENA bit is low and the autoscan cycle is disabled. Once the SCANENA bit is set, the board autoscans sequentially and repeatedly through the selected number of channels starting with channel 0. If the autoscan is in process and the SCANENA bit is set low, the board completes the current ADC conversion and then stops.

Bit 12, TWOCOMP: The TWOCOMP control bit affects the state of the most significant data bit, D15, as it being copied from the ADC data output into the SRAM. The output of the ADC itself assumes a two's complement convention. If the TWOCOMP bit is set high, the D15 bit is written unchanged into the SRAM, otherwise, D15 is inverted and the data is considered straight or offset binary.

Bit 11, Reserved: This bit is reserved for future expansion, write to zero.

Bits 10 and 9, SCANSIZ[1..0] : The SCANSIZ1 and SCANSIZ0 bits select the number of inputs to scan and digitize. The selections are 24, 16, or 8 channels. With any selection, the scan starts with channel 0, sequences up the channels until the selected number is reached, and then repeats starting at channel 0. It is recommended that the SCANSIZx bits be changed only while the scan cycle is disabled.

The definition of the SCANSIZx bits are detailed in Table 3-3 below:

Table 3-3 SCANSIZx Bit Definitions

SCANSIZ1	SCANSIZ0	Channels Scanned
0	0	0 through 23
0	1	0 through 15
1	0	0 through 7
1	1	0 through 7

Bits 8 through 0, Reserved: These bits are reserved for future expansion, write to zero.

Status Bit Assignments

All 16 data bits of the status word are defined as either true status or a fixed state. The bit descriptions are detailed below:

Table 3-4 Status Register Bit Map

Status Register (Offset 00 through 0E) Write Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED_OFF	SOFT_RST	SCANENA	TWOCOMP	TEST1	SCANSIZ1	SCANSIZ0	CALBUSY

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved							

Status Register Bit Definitions

Bits 15 through 9, Status Bits: These bits indicates the status of their respective control register bits.

Bit 8, CALBUSY: This bit is high while the ADC is in calibration mode.

Bits 7 through 0, Reserved: These bits are reserved for future expansion, write to zero.

ADC Data Formats

The convention for the ADC data represents the most significant bit as D15 and the least significant bit as D0. If the TWOCOMP bit in the CSR is a one, the coding is termed two's complement. If the TWOCOMP bit is zero, the coding is termed straight binary for unipolar ranges and offset binary for bipolar ranges. Table 3-5 details the relationship of the input voltage to ADC output format for 0 to +10 V and ±10 V ranges. The other ranges have a similar relationship.

Table 3-5 ADC Data Formats

Range: Unipolar, 0 to +10 V Output: Straight Binary		
Fraction of Scale	**Equivalent Input Voltage**	**D15.....D0**
Full Scale	+9.99985 V	1111 1111 1111 1111
Half Scale	+5.00000 V	1000 0000 0000 0000
Zero Scale	+0.00000 V	0000 0000 0000 0000

Range: Bipolar, -10 to +10 V Output: Offset Binary		
Fraction of Scale	**Equivalent Input Voltage**	**D15.....D0**
+Full Scale	+9.99969 V	1111 1111 1111 1111
+Half Scale	+5.00000 V	1100 0000 0000 0000
Zero Scale	+0.00000 V	1000 0000 0000 0000
-Half Scale	-5.00000 V	0100 0000 0000 0000
-Full Scale	-10.0000 V	1000 0000 0000 0000

Range: Bipolar, -10 to +10 V Output: Two's Complement		
Fraction of Scale	**Equivalent Input Voltage**	**D15.....D0**
+Full Scale	+9.99969 V	0111 1111 1111 1111
+Half Scale	+5.00000 V	0100 0000 0000 0000
Zero Scale	+0.00000 V	0000 0000 0000 0000
-Half Scale	-5.00000 V	1100 0000 0000 0000
-Full Scale	-10.0000 V	1000 0000 0000 0000

LSB Bit Weights and Specific Ranges

When describing the input ranges, they are often rounded off for simplicity. Table 3-6 lists the LSB weights and the specific input range that results.

Table 3-6 LSB Bit Weights and Specific Ranges

Input Range	LSB Weight	+Full Scale (V)	+Half Scale (V)	Zero Scale (V)	-Half Scale (V)	-Full Scale (V)
0 to +5 V	76.2939 µV	+4.99992	+2.50000	0.0	-----	-----
±2.5 V	76.2939 µV	+2.49992	+1.25000	0.0	-1.25000	-2.50000
0 to +10 V	152.588 µV	+9.99985	+5.00000	0.0	-----	-----
±5 V	152.588 µV	+4.99985	+2.50000	0.0	-2.50000	-5.00000
±10	305.176 µV	+9.99969	+5.00000	0.0	-5.00000	-10.00000

Input Frequency Range

If the optional low pass input filters are present, they will dictate the upper frequency limit of the signal that can accurately be converted. Note that the signal's upper frequency limit should be well below the corner frequency of the filters. At the corner frequency, the amplitude of the signal is attenuated to 70.7 percent of its original amplitude. One least significant bit (LSB) of 16-bit conversion is equivalent to approximately 0.001526 percent of full scale.

If no input filters are present, the input frequency range is limited by either the sample rate or the frequency response of the board amplifiers. A basic rule of analog sampling, called the Nyquist limit, states that the frequency of a signal should not exceed one half the sample rate. Although the VMIPCI-3322 converts at an aggregate rate of one channel every 10.05 msec (or 99.5 kHz), the rate at which each channel is repeatedly sampled is actually 99.5 kHz divided by the number of channels sampled.

The primary reason the VMIPCI-3322 offers a selection in the number of channels scanned per cycle is to improve frequency response. The user can sample higher frequency signals by limiting the number of channels used. Table 3-7 details the frequency range for the three groups of channels being scanned.

Table 3-7 Input Frequency Verus Channels Scanned

Channels Used	Channel Sample Rate	Input Frequency Limit	Reason
0 through 23	4.146 kHz	2.073 kHz	Nyquist Limit
0 through 15	6.219 kHz	3.109 kHz	Nyquist Limit
0 through 7	12.438 kHz	6.219 kHz	Nyquist Limit

Example:

```
-> f 114a 3322 0

Bus# = 0                          Device_function# = 68
Dev ID = 3322                     Vendor ID = 114a
Status = 0                        Command = 107
Class Code = ff0000               Rev ID = 80
Base Addr Reg 0 = fe81
Base Addr Reg 1 = fd81
Base Addr Req 2 = ffafff40
Base Addr Reg 3 = 0
Base Addr Reg 4 = 0
Base Addr Reg 5 = 0
Exp ROM Base = 0
Int pin = 0                       Int line = 0
->
```

Figure 3-1 Typical I/O (Regs 0 and 1) and Memory (Reg 2) Mapped Base Address Registers

Maintenance

Maintenance

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

1. Software
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components of adjacent boards are disturbed when inserting or removing the board from the PCI board slot
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. *This RMA Number must be obtained prior to any return.*

Maintenance Prints

User-level repairs are not recommended. The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.