# VMIVME-1183
## 32-bit Change-of-State (COS) Input Board with Sequence-of-Events (SOE)

- 32 bits of high-voltage digital Change-of-State inputs (COS)
- COS is programmable to respond to rising edge only, falling edge only, or any edge on a selectable basis per channel
- Each group of 8 inputs are jumper-selectable to monitor: contact closure, voltage sourcing (including TTL levels), or current sinking
- Contact debounce is jumper-selectable: 10 µs, 1, 5, or 10 ms
- Input voltage range: 0 to 66 V
- User-selectable input voltage thresholds (+0.6 to +38 V)
- 8-, 16-, or 32-bit data transfers
- COS data is stored 512 bytes deep to prevent latency loss
- Double slot Eurocard form factor with P2 inputs and front panel with fail LED
- High reliability DIN-type input connector (P2)
- Change-of-State FIFO identified by a unique programmable interrupt vector
- Optional external quadrature clock input w/ daisy-chain capability
- Sequence-of-Events (SOE) monitoring on channel-by-channel basis

**INTRODUCTION** — The VMIVME-1183 is a 32-channel P2 input board with Change-of-State (COS) interrupt capabilities. The interrupt control logic can be programmed to issue an interrupt upon specific state changes. The user selects the state change to use by programming the Control and Status Register (CSR) for the desired activity. This board will store up to 512 state changes as long as the COS logic is enabled. This will prevent the board from losing a state change during interrupt servicing.

The VMIVME-1183 supports built-in-test (BIT). BIT registers are available to test the active components of the input data paths on the board. The board also supports byte, word, and longword data transfers, during basic input data operations.

## FUNCTIONAL CHARACTERISTICS

**Input Organization:** The inputs are arranged into four input ports, 8 bits wide. The data ports are accessible on 8-, 16-, or 32-bit boundaries.

**Addressing Scheme:** Twenty-one jumpers are used to select the base address of the board. This address may be supervisory or non-privileged. The registers on this board are stacked on top of this base address. For detailed information about these registers and their relationship to the base address of the board, see *"Programming"* in the VMIVME-1183 Product Manual.

**VMEbus Compliance:** Complies with the VMEbus Specification, ANSI/IEEE STD 1014-1987 IEC 821 and 297.

**Board Type:** Slave

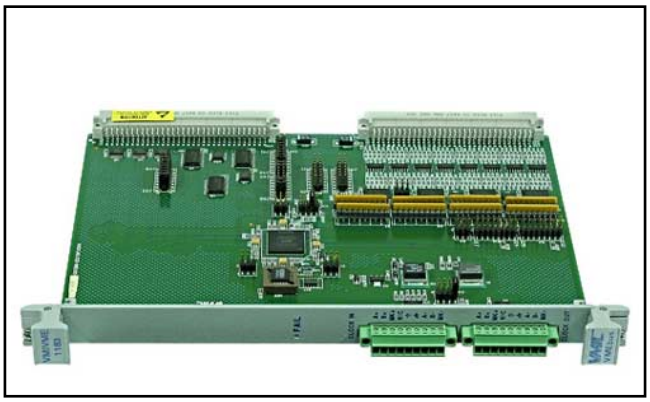
**Board Size:** 6U (166 x 233.4 mm)

**Addressing:**

| Mode | Responding Modifiers |
|---|---|
| A24 | 39, 3D |
| A16 | 29, 2D |

**Data Transfers Available:** D32, D16, D08 (EO)

**COS Data Transfers:** D32



**Bus Interrupter:**

| | |
|---|---|
| Interrupt Levels: | I (1) to I (7) |
| Interrupt Release: | ROAK, ROFE* |
| Interrupt Vector: | D08 (O) |

NOTE: *Release-On-FIFO-Empty

## INPUT CHARACTERISTICS

**Input Signal Conditioning:** The input buffers provide a high input impedance (15 kΩ) with a threshold accuracy of 10 percent over the entire 66 V input range (typically). Figure 2 shows the input signal conditioning electronics. This circuit provides for input debounce with a time constant that is user selected through a jumper. The bounce eliminator circuit will remove bounce on both the *make* and the *break* of a contact closure. This debounce circuit can also be used to eliminate input transients caused by ground noise or crosstalk in cables. The debounce times are jumper-selectable for 10 µs, 1, 5, and 10 ms.

**Ordering Options**

| Aug. 5, 2003 800-001183-000 A | | A | B | C | – | D | E | F |
|---|---|---|---|---|---|---|---|---|
| VMIVME-1183 | – | 0 | 0 | 0 | – | | | |

ABC = 000 (Options reserved for future use)

**Connector Data**

| | |
|---|---|
| Compatible Cable Connector | Panduit No. 129-964-435 |
| Strain Relief | Panduit No. 100-000-072 |
| PC Board Header Connector | Panduit No. 100-096-033A |

**Note**

Panduit is also known as ITW/Pancon.

**For Ordering Information, Call:**
**1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859**
**E-mail: info@vmic.com Web Address: www.vmic.com**

**Input Configurations:** Voltage source or logic level

Current sink or contact sense

**Input Voltage Range:** 0 to 66 V

**Input Connector Type:** P2 User Inputs (refer to "*Connector Data*" in the ordering options on page 1 of this specification).

**Built-in-Test:** This board is designed with internal self-test logic that exercises the input data paths. Special output registers are provided to generate data that may be used as a *health test* during real time or offline operation. A special test mode bit disables the change-of-state logic and enables the output test registers which are then used to drive the input comparators. This bit is provided in the board's control register. A front panel Fail LED is illuminated at power up and can be extinguished under program control upon successful completion of diagnostics.

**Type:** VMEbus slave/interrupter

**Levels:** Any of the seven available interrupt levels

**Interrupt Event:** The COS FIFO is assigned an interrupt level and an interrupt vector. Any change-of-state causes an interrupt to be generated at the assigned level.

**Interrupt Enable:** An interrupt enable bit is provided for each channel.

**COS Selection:** Two control bits per input channel are provided in the CSR to control the type of change-of-state interrupts desired. These types are (1) no interrupts (input data only), (2) falling edge only, (3) rising edge only, (4) any transition, and (5) COS clocking - internal or external quadrature (with marker) clocking (single-ended or differential).

**COS Select State**

| SEL B | SEL A | COS Mode |
|---|---|---|
| 0 | 0 | No Interrupts |
| 0 | 1 | Rising Edge Only |
| 1 | 0 | Falling Edge Only |
| 1 | 1 | Any Transition |

**COS Data and SOE:** The COS data is stored in a FIFO 512 bytes deep. This data is available at the addresses listed in the "Programming" Chapter 3 of the VMIVME-1183 Product Manual. Sequence-of-events stores the state of a channel before and after each event for comparison. Time stamping (from an external counter) is available at the front panel connector.

## PHYSICAL/ENVIRONMENTAL

**Temperature:** 0 to 55 °C, operating
-20 to 85 °C, storage

**Humidity:** 20 to 80 percent relative, noncondensing

**Cooling:** Forced air convection

**Dimensions:** 6U double slot Eurocard — 160 x 233.35 mm

**Power Requirements:** 1.0 A at +5 VDC typical. External Voltage Current requirement is 100 mA (maximum).

**MTBF:** <TBD>

## TRADEMARKS



## APPLICATION AND CONFIGURATION GUIDES

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

| Title | Document No. |
|---|---|
| Digital Input Board Application Guide | 825-000000-000 |
| Change-of-State Board Application Guide | 825-000000-002 |
| Digital I/O (with Built-in-Test) Product Line Description | 825-000000-003 |
| Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide | 825-000000-004 |
| Analog I/O Products (with Built-in-Test) Configuration Guide | 825-000000-005 |
| Connector and I/O Cable Application Guide | 825-000000-006 |

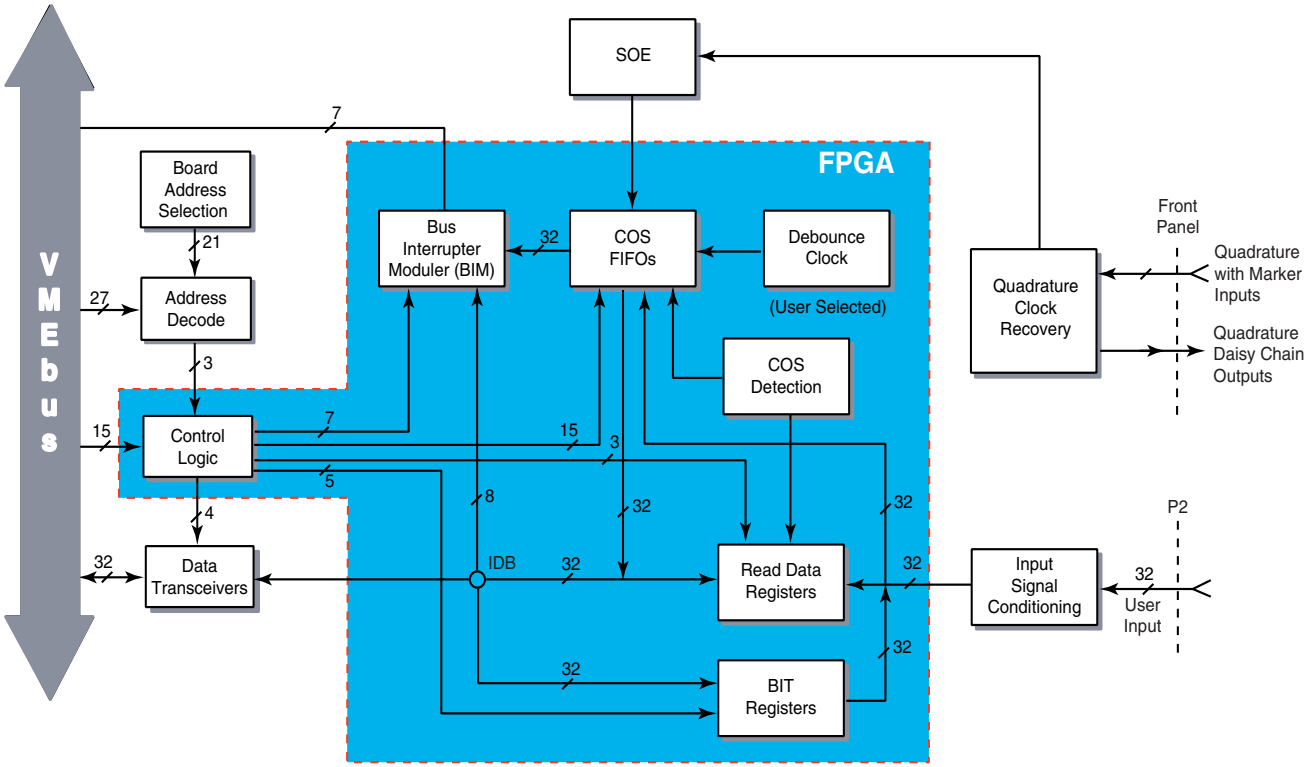
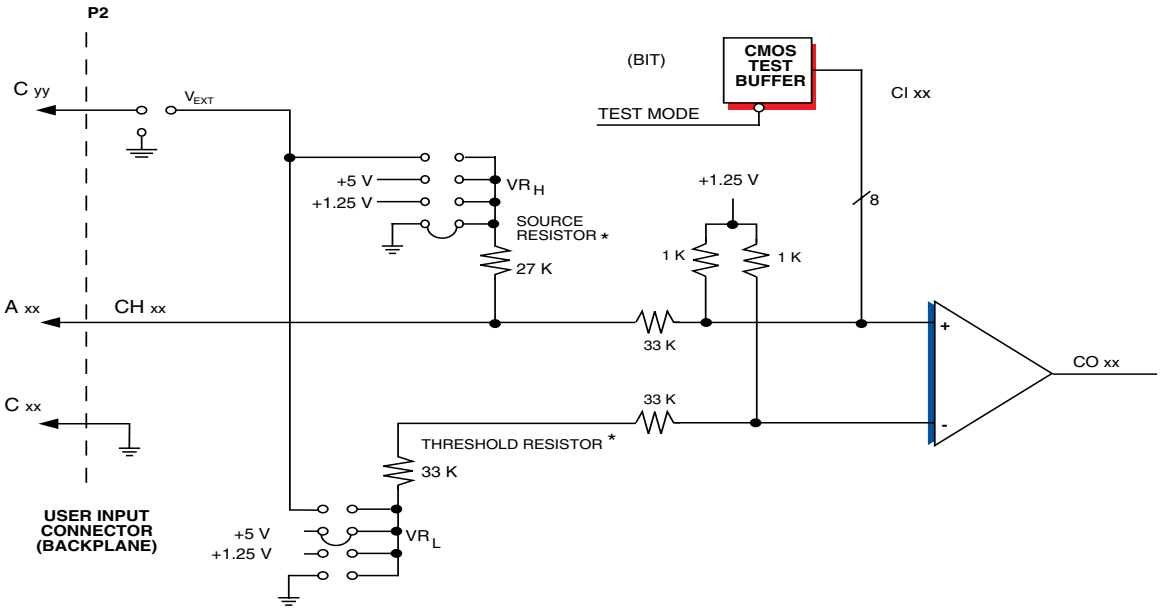



**Figure 1. VMIVME-1183 Functional Block Diagram**




*These SIP resistors are socketed and interchangeable.

**Figure 2. Typical Input Signal Conditioning for Voltage Sourcing Inputs**

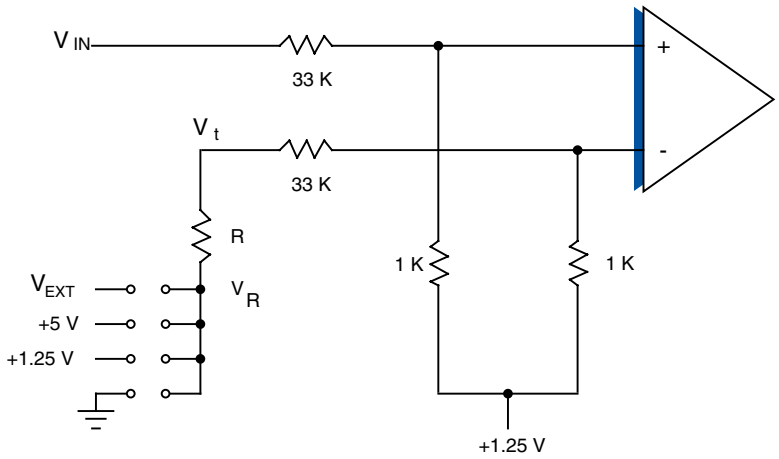



**Figure 3. Threshold Voltage ($V_t$) Diagram**

**Table 1. Threshold Voltages ($V_t$) for R = 27 kΩ**

$V_t = [(V_R - 1.25) (.56)] + 1.25$

| $V_R$ | $V_t$ |
|---|---|
| 0 V | 0.55 V |
| 1.25 V | 1.25 V |
| 5 V | 3.35 V |
| 12 V | 7.27 V |
| 24 V | 14 V |
| 28 V | 16.20 V |
| 48 V | 27.35 V |
| 66 V | 37.52 V |

**Table 2. Threshold Voltages ($V_t$) for R = 33 kΩ**

$V_t = [(V_R - 1.25) (.51)] + 1.25$

| $V_R$ | $V_t$ |
|---|---|
| 0 V | 0.61 V |
| 1.25 V | 1.25 V |
| 5 V | 3.2 V |
| 12 V | 6.7 V |
| 24 V | 12.9 V |
| 28 V | 14.8 V |
| 48 V | 25.1 V |
| 66 V | 34.3 V |