VMIVME-3119

16-bit Scanning Analog Input Board with Programmable Gain, Filter Cutoff, and Autocalibration Per Channel

- 16 differential analog input channels
- Software-programmable gain per channel (x1, x10, x100, x1,000)
- Input signal range from ±10 mV to ±10 V
- Software-programmable fourth-order low pass filter (1 Hz, 10 Hz, 100 Hz, 1 kHz) factory option of Bessel or Butterworth response
- Autocalibration per channel utilizing DSP technology
- 16-bit A/D converter; high accuracy
- Software-programmable sample rate from 305 Hz to 100 kHz aggregate
- Software-programmable scan table
- Large data buffer retains up to 4 million data samples
- Overvoltage input protection
- Flexible triggering: internal, external, or multiboard synchronous
- VMEbus interrupts at mid scan or end scan
- Two-slot configuration
- UIOC® capability
- Self-test
  - — Extensive on-board diagnostic testing capability
  - — Implements precision internal reference voltages
  - — Independent of field connections

APPLICATIONS

- Precision voltage monitoring
- Data acquisition systems
- Laboratory instrumentation
- Process control
- Automatic test equipment

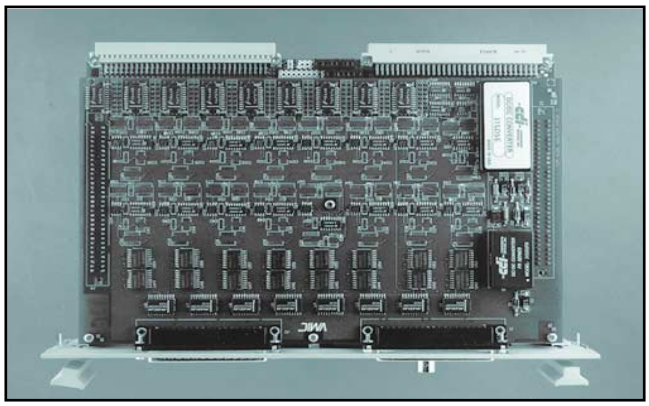
INTRODUCTION — The VMIVME-3119 analog input board provides 16 high accuracy differential analog input channels with high throughput 16-bit analog-to-digital (A/D) conversion. Each input is equipped with a dedicated programmable-gain amplifier (PGA), software selectable, fourth-order low pass filter, and autocalibration.

The on-board autocalibration corrects for offset and gain errors in real-time. Calibration correction values are determined at user-controlled calibration intervals without removing the board from the system. Individual channel correction is accomplished by DSP technology in real-time for every A/D conversion. Calibration can be verified at any time by implementing the self-test feature. Self-test uses internal precision voltages, which are applied to all channels simultaneously to verify signal path integrity.

The VMIVME-3119 can be jumper configured for either standard or extended address space, and can be jumper configured to occupy 16, 8, 4, 2, 1 Mbyte or 512, 256, or 128 Kbyte.

The VMIVME-3119 has a software-configurable sample buffer which begins at the base address of the Data RAM (address P) (see Figure 1). The size of the sample buffer determines the number of samples to be stored per scan. The sample buffer size can be configured in any power-of-2 from 1 sample to 4 M samples.

A functional block diagram is provided in Figure 2.



FUNCTIONAL CHARACTERISTICS

Compliance: This product complies with the VMEbus specification ANSI/IEEE STD 1014-1987 IEC 821 and 297 with the following mnemonics:

Addressing:	A32, A24 supervisory or nonprivileged data access
Data Access:	D32, D16, D8(EO), D32:BLT, D16:BLT, D8(EO):BLT
Interrupts:	I(1 to 7) ROAK, D08(EO) vector
Form Factor:	6U, 2 slot

Ordering Options

Sept. 24, 2001 800-003119-000 C	A	B	C	–	D	E	F
VMIVME-3119 –	0			–			

A = 0 (Option reserved for future use)
B = Filter Type Option
0 = No Filter
1 = Bessel Filter
2 = Butterworth Filter
C = Number of Channels
0 = 16 Channels, 4 M Samples
1 = 16 Channels, 2 M Samples
2 = 8 Channels, 4 M Samples
3 = 8 Channels, 2 M Samples

Example

A part number VMIVME-3119-013 specifies an 8-channel VMIVME-3119 board with a 2 megasample data buffer and Bessel low pass filters.

I/O Connector Data

Compatible Cable Connector	Standard subminiature D 37-pin male connector

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

VME Interrupt: An interrupt can be issued on any level, and a single byte vector will be placed on the bus when acknowledged. There is one ROAK interrupt for the board and it can be generated when the data buffer is 50 percent (mid scan) or 100 percent (end scan) filled.

Data-Ready Flag: A data-ready flag is set when the data buffer is at end scan or mid scan.

Self-Test: Precision internal voltage references are substituted for field inputs on all channels simultaneously. Field cables may be left connected.

System Reset: A reset automatically establishes the following default conditions:

Continuous scan of channels 0 to 15
20 kHz aggregate sample rate
Buffer size = 32 bytes (16 samples)
Channel Gain = x1 (input voltage is ±10 V full scale)
Channel Filter Frequency = 1 kHz (filter option)
Channel Filter Frequency = 10 kHz (no-filter option)

PGA: Channel gains of x1, x10, x100, x1,000 are selected through a programmable-gain amplifier (PGA). The gain of each channel can be independently selected.

Calibration: The VMIVME-3119 uses DSP technology to determine and store gain and offset coefficients for all A/D channels. This feature eliminates the need for gain and offset trim potentiometers and allows user-initiated calibration. The DSP routes a precision voltage to each channel, reads the response from the 16-bit ADC, and then calculates the offset and gain coefficients for the gain setting selected by software. The calibration coefficients are stored in EEPROM. During normal operation, the A/D data for a particular channel is multiplied by the gain coefficient and added to the offset coefficient. This corrected data is then written to the memory. Note: After powerup, the DSP initializes the board by recalling calibration coefficients from EEPROM for each channel at the x1 gain setting (±10 V input).

Front Panel LED: The LED indicates progression/status of certain DSP operations, such as power-on, self-test, and calibration. The LED can also be software controlled.

Board Identification: A Board Identification Register (BIR) contains the VMIVME-3119 identification code.

Data Buffer: 8 Mbyte (4 Megasamples), maximum. (See the Ordering Options.)

Scan Table: 1 to 1,024 byte scan table which, when enabled, defines the scanning sequence of the VMIVME-3119.

Sample Rate: The internal sample clock is software programmable from 305 to 100,000 SPS (samples per second). The sample rate can be controlled from zero to 100,000 SPS by the external triggering sources. This sample rate is defined as the aggregate sample rate for all active channels.

SCAN MODES — The VMIVME-3119 supports the following scan modes:

Continuous Scan: When a scan is triggered, the selected channels are scanned continuously until the scan is aborted.

Single Scan: When a scan is triggered, the selected channels are scanned until the sample buffer is filled.

Advance Scan on Trigger: On each trigger event, the scan is advanced to the next active channel. This scan mode allows a VMIVME-3119 to be synchronized to a master or to be controlled by an external sample command/clock.

TRIGGER MODES — The VMIVME-3119 supports the following trigger modes:

Single-Board, Software: The configured scan is triggered by a software trigger command.

Single-Board, Single-Ended External: The configured scan is triggered by a high-to-low TTL logic-level change on the single-ended external trigger input.

Multiboard Master, Software: The configured scan is triggered by a software trigger command. The differential trigger output can be used to synchronize multiple boards to this software trigger.

Multiboard Master, Single-Ended External: The configured scan is triggered by a high-to-low TTL logic-level change on the single-ended external trigger input. The differential trigger output can be used to synchronize multiple boards to this single-ended external trigger.

Multiboard Slave, Differential External: The configured scan is triggered by a differential external trigger.

ANALOG INPUTS

(Specified at +25 ˚C and rated supplies, unless otherwise noted.)

Input Configuration: Sixteen differential input channels with selectable gain, filter cutoff, and autocalibration. An 8-channel option is available; see the Ordering Options.

A/D Converter: 16-bit A/D converter

Input Voltage Ranges: Software selectable as ±10 mV, ±100 mV, ±1 V, ±10 V

Bias Current: ±5 nA, ±10 pA/˚C

Common-Mode Voltage: $(^{V}CM + \frac{(V_{DIFF} / 2)}{Gain})$, ±10 V, 0 V input signal

Common-Mode Rejection Ratio (CMRR): DC to 60 Hz with 350 W source imbalance. Units in dB.

Gain	Minimum	Typical
1	85	100
10	100	120
100	120	140
1,000	120	140

Input Noise: Typical and maximum input noise is shown in Table 1. In this table, inputs Hi and Lo are shorted to AGND at front panel connector. Noise units are µV RMS.

Table 1. Noise in µV RMS as a Function of Filter Setting and Input Range

Typical				
Range	1 kHz	100 Hz	10 Hz	1 Hz
±10 V	290	275	275	260
±1 V	28	28	28	28
±100 mV	2.9	2.5	2.5	2.5
±10 mV	0.56	0.3	0.25	0.25
Maximum				
±10 V	465	420	400	400
±1 V	40	40	40	40
±100 mV	4.5	4.0	3.8	3.8
±10 mV	0.7	0.6	0.4	0.3

Overvoltage: Protected to ±40 V sustained, ±100 V for one second

Crosstalk: DC to1 kHz, 100 SPS sample rate
Adjacent Channel: -75 dB
Other Channels: -90 dB

TRANSFER CHARACTERISTICS

(Specified at +25 ˚C and rated supplies, unless otherwise noted.)

Gain Accuracy: ±0.005 percent, ±5 PPM/˚C, ±0.005 percent/year after calibration to internal references

Integral Nonlinearity: ±0.0025 percent, maximum from best straight line

Sampling Rate: 100 k SPS (thousand samples per second) maximum aggregate rate. The sample period can be programmed from 10 µs to 3.277 ms with 50 ns resolution.

Full Power Bandwidth(1): 11.1 kHz, typical

Bandwidth: DC to selected filter frequency, or
48 kHz (-3 dB) at G = 10
10 kHz (-3 dB) at G = 100
1 kHz (-3 dB) at G = 1,000

Low Pass Input Filters: Fourth-order low pass filters with software-programmable cutoff frequencies of 1, 10, or 100 Hz, or 1 kHz. Factory options of Bessel or Butterworth filter types available. Also available without these programmable filters. See the Ordering Options on the first sheet of this specification.

PHYSICAL/ENVIRONMENTAL

Dimensions: Standard VME 6U double height board (160 x 233.5 mm); 2 slot

Temperature Range: 0 to +65 ˚C, operating
-25 to +85 ˚C, storage

Relative Humidity: 20 to 80 percent, noncondensing

Cooling: Normal VMEbus chassis forced air circulation

Power Requirements: 4.3 A typical at 5 VDC, 5.0 A maximum

Altitude: Operation to 10,000 ft (3,048 m)

1. Full power calculated from slew rate: FPBW = SR/2p Vp, where Vp = 10, SR = .7 V/ms

TRADEMARKS

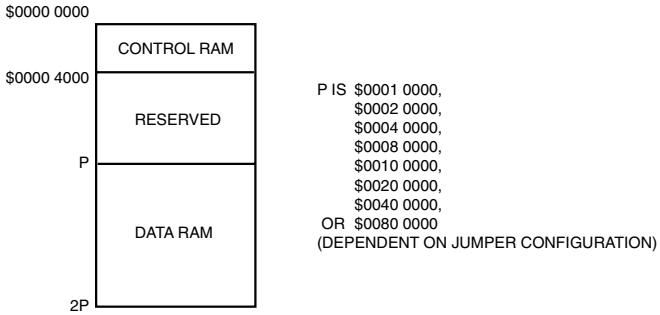


Figure 1. Memory Map

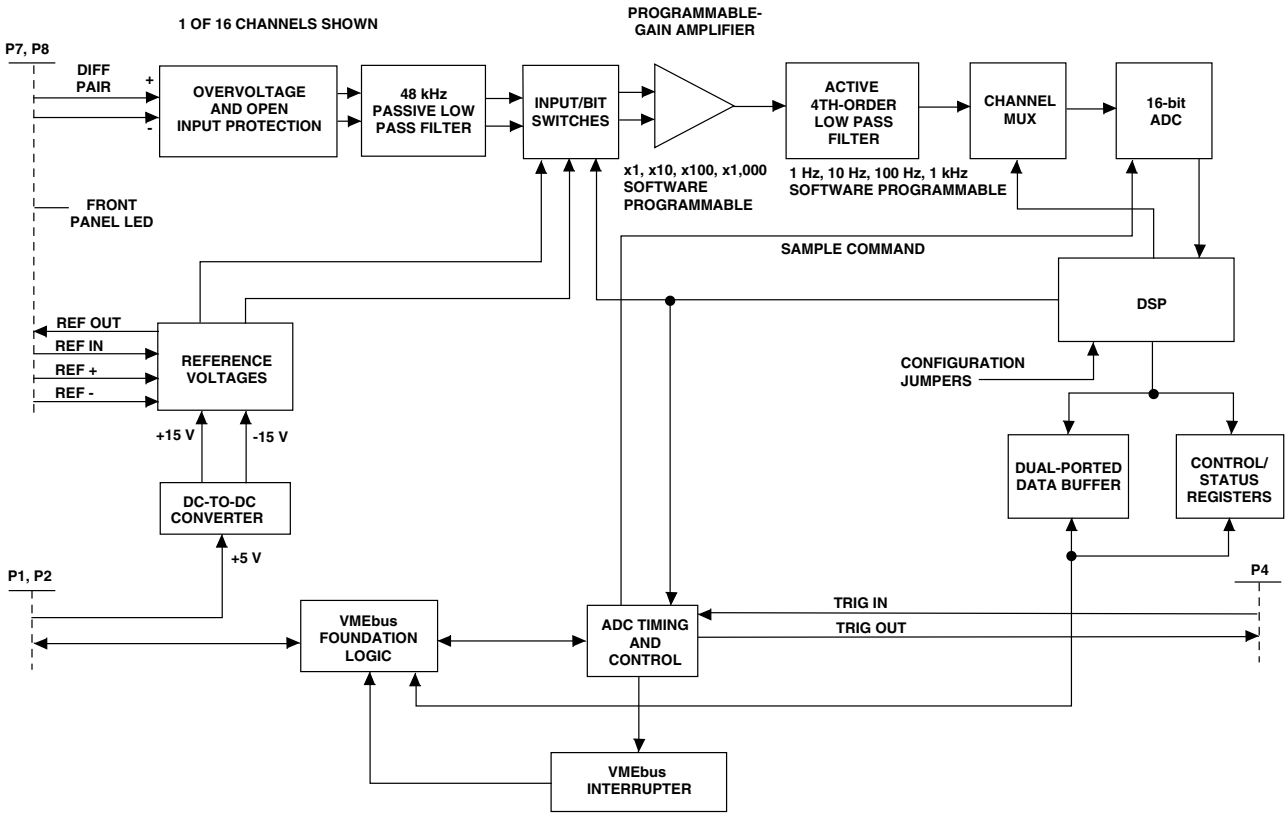


Figure 2. VMIVME-3119 Functional Block Diagram