VMIVME-3123

16-bit High Throughput Analog Input Board
16 Channels with Simultaneous Sample-and-Hold Inputs

- 16 differential analog input channels
  - — Software-selectable as 1, 2, 4, 8, or 16 active channels
- 16-bit A/D converters; one per channel
- Simultaneous sample-and-hold inputs
- High throughput
  - — 1,600 kHz aggregate sample rate
  - — 100 kHz per channel; 200 kHz with channel pairing
- Digital calibration; no channel trimmers
- Built-in-Test; internal references applied to channel inputs; all active devices tested
- Large data buffer; up to 4 million data samples
- Transient capture mode triggering on input signal
- Continuous sampling mode
- Triggering capabilities
  - — Internal, external, VME host triggering, or multiboard synchronous
- ±10 V, ±5 V input ranges with bipolar option and +10 V, +5 V input ranges with true unipolar option
- Selectable delay
- Low pass filters for antialiasing
- Interrupter

APPLICATIONS

- Precision voltage monitoring
- Data acquisition systems
- Control systems
- Automatic test equipment (ATE)
- Trainers and simulators

INTRODUCTION — The VMIVME-3123 analog input board provides 16 high accuracy differential analog input channels with high throughput 16-bit analog-to-digital (A/D) conversion rates to 1.6 million samples per second. Each input is equipped with a dedicated sample-and-hold amplifier, a fourth-order antialiasing filter, and a precision 16-bit A/D converter.

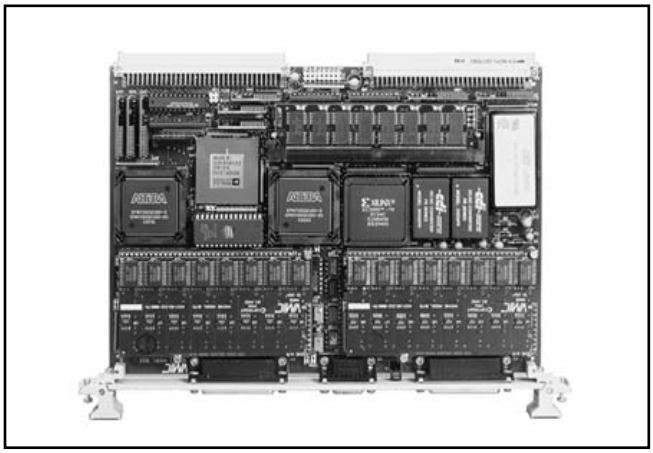
Digitized samples are accumulated in a data buffer until retrieved by the system. Buffer size is software controlled from one sample to 4 million samples.

Accuracy is optimized with the use of correction values for gain and offset that are applied in real-time, and determined during a host-controlled calibration mode. Calibration can be performed at any time without removing the board from the system. Calibration uses internal precision voltages (a built-in-test feature) applied to all input channels to determine the correction values. A test mode as well as the host have access to the voltages for BIT purposes.

FUNCTIONAL CHARACTERISTICS

Compliance: This board complies with the VMEbus specification (ANSI/IEEE 1014-1987 IEC 821 and 297) with the following mnemonics:

Addressing:	A32, A24, A16
Address Modifiers:	0F, 0D, 0B, 09, 3F, 3D, 3B, 39, 2D, 29
Data Transfers:	D32: D16: D08 (EO): D08 (0): BLT
Control Register Transfers:	
Hardware Registers:	D16, D08 (EO)
Firmware Registers:	D16 (WRITE) D16, D08 (EO) (READ)
Interrupts:	I(1) to I(7) ROAK, with D08 (0) vector
Form Factor:	6U



Board Address: The physical base address for the board's data buffer is software selected by on-board registers in short I/O space. The standard and extended windows into the data buffer can be enabled/disabled through registers in short I/O space.

Ordering Options

June 14, 2002 800-003123-000 M	A	B	C	–	D	E	F
VMIVME-3123 –				–			

A = Bipolar Input Option
- 0 = Reserved
- 1 = Bipolar (±10 and ±5 V Input Ranges)
- 2 = Unipolar (+10 and +5 V Input Ranges)

B = Low Pass Filter Type and Frequency
- 0 = No Filter
- 1 = Bessel, 240 Hz
- 2 = Bessel, 2.4 kHz
- 3 = Bessel, 24 kHz
- 4 = Butterworth, 240 Hz
- 5 = Butterworth, 2.4 kHz
- 6 = Butterworth, 24 kHz

C = Input Channels and Data Buffer Size
- 0 = 16 Channels/4 Megasamples
- 1 = 16 Channels/1 Megasample
- 2 = 8 Channels/4 Megasamples
- 3 = 8 Channels/1 Megasample

Example

A part number VMIVME-3123-140 specifies a 16-channel VMIVME-3123 board with 4 megasample data buffer, bipolar input ranges, and 240 Hz Butterworth low pass filter.

I/O Connector Data

Style	Recommended Connecting Component	P3 and P4 I/O Connector
25-pin Discrete Wire	Mating Connector 25-pin D-Subminiature Discrete Wire Using Solder Cups	AMP 747912-2
	Connector Shell Housing	AMP 748042-1
9-pin Discrete Wire	Mating Connector 25-pin D-Subminiature Discrete Wire Using Solder Cups	AMP 747904-2
	Connector Shell Housing	AMP 748038-1

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com
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VMEbus Access: Address modifier bits are enabled in short I/O registers and decoded to support both nonprivileged, supervisory, or both access modes.

Data Transfers: Conversion data is retrieved from the data buffer through the memory-mapped data space, commencing with the first conversion sample and proceeding in sequence through the last sample in the buffer.

Built-in-Test: Precision internal reference voltages can be substituted for the field inputs at all channels simultaneously.

System Reset: After a system reset occurs, the board enters an IDLE operating mode in which the board sample clock is chosen as the sampling source, and the buffer sizes are maximized with all channels enabled. The board does not acquire data in IDLE mode. The front panel LED indicator is turned ON at reset.

Calibration: This board calibrates itself under host control and then uses the gain and offset coefficients during signal acquisition. This eliminates the need for gain and offset trim potentiometers, and provides a software solution to calibrating the board. Calibration is performed when the host changes the operating mode to CAL and consists of routing precision reference voltages to the channel inputs, reading the associated 16-bit analog-to-digital converter (ADC), determining the gain and offset coefficients, and storing them in on-board volatile memory. During data acquisition, the A/D data in a particular channel is multiplied by the gain coefficient and added to the offset coefficient. This corrected data is then written to the data buffer.

Note: Calibration is under host control and does not occur during powerup.

ELECTRICAL CHARACTERISTICS

(Specified at +25 ˚C and rated supplies, unless otherwise noted.)

Analog Inputs:

Input Configuration: Sixteen differential input channels, with dedicated sample-and-hold per channel. Optional 8-channel configuration available; see the Ordering Options.

A/D Converters: 16-bit A/D converter per channel

Voltage Ranges: ±5 and ±10 V full scale, software-selectable

Offset Voltage and Drift: ±2.7 µV, ±5 µV/°C RTI[1]

Bias Current and Drift: ±55 ±1 nA/°C

Common-Mode Voltage (CMV): (VCM + (VDIFF/2)(G)): ±12 V

Common-Mode Rejection Ratio (CMRR): 95 dB typical, 85 dB minimum DC to 60 Hz with 350 Ω source unbalance

Noise: 1,000 µVRMS, RTI at 240 Hz
1,000 µVRMS, RTI at 2,400 Hz
1,000 µVRMS, RTI at 24 kHz
1,300 µVRMS, RTI at No Filter

Overvoltage: Protected to ±40 V sustained, ±100 V for one second

Crosstalk: 96 dB maximum, DC to 1 kHz

TRANSFER CHARACTERISTICS (±10 V FSR)

Resolution: 16-bit (305 µV/LSB)

Gain Accuracy: ±0.005 percent ±21 PPM/˚C ±0.005 percent/year after calibration to internal references. Drift errors can be removed with recalibration.

Integral Nonlinearity: ±0.0053 percent

Differential Nonlinearity: ±0.0053 percent

Sampling Rate: 1,600 KSPS (thousand samples per second) maximum aggregate rate. Per-channel rate software controlled from 381 to 100,000 SPS. The per-channel rate can be doubled to 200,000 SPS by pairing input channels (0 and 8, 1 and 9, etc.) when using a 16-channel board with a net reduction in available channels.

Sampling Delay: Internal clock - 40 ns (typical), External clock - 70 ns (typical), Multiboard - 100 ns (typical)
Board-to-board sample time difference - 50 ns maximum

Sampling Jitter: 0 to 3 ns (0 to 15 ns if channel pairing is used to achieve a 200 KSPS per channel sample rate)

Data Latency: The user should note the data deposited into DRAM from the analog section will correspond to the (n-1) sample. When a sample pulse is generated, the ADC converts the sampled analog input and simultaneously transmits the previously converted sample to the Digital Signal Processor to correct and place in DRAM. The latency from the sample pulse to the availability of the n-1 sample will be less than 20 µs.

Internal Bit References: ±9.9800 VDC, ±4.99 VDC ±0.003 percent ±3PPM/°C ±0.002 percent/year

Bandwidth: DC to specified filter frequency. The *No Filter* option provides a minimum bandwidth of DC to 400 kHz.

Large Signal Bandwidth: 1 kHz (no filter) with 10 V peak

Small Signal Bandwidth: 40 kHz (no filter)
1 V pk-pk

1. RTI = Referred to inputs.

Low Pass Input Filters: Fourth-order low pass filters with corner frequencies of 240 Hz, 2.4 kHz, or 24 kHz, ±25 percent. Available with Bessel or Butterworth response. (See the Ordering Options.)

ACCESS AND CYCLE TIMES

Access Time: Time (DSA* to DTACK*)

Cycle Time: Time (DSA* to DSA*)

Hardware Registers: 250 ns Access Time

Firmware Registers: 3.5 µs Access Time (maximum), 2.5 µs (typical)

Note: Firmware registers are used for nonreal-time operations and are available only during IDLE mode.

Non-BLT DRAM Memory: 380 ns Access Time, 750 ns Cycle Time

BLT DRAM Read Access:
1st Transfer - 360 ns Access Time, 640 ns Cycle Time
2nd - 256th Transfer - 100 ns Access Time, 260 ns Cycle Time

Note: The VMEbus must compete with refresh operations and input data deposits through arbitration for control of the DRAM. Refresh operations occur at 16 µs intervals and hold the DRAM for 300 ns. A 16-channel burst of analog input data will occupy the DRAM for 1.5 µs (two bursts of 750 ns each) and occurs at the host-selected sampling rate during modes when the board is digitizing data. The VMEbus has the lowest priority.

CONTROL

Sample Clock: All active inputs are sampled (that is, enter *Hold* sample mode) simultaneously in response to sampling clock which is controlled by three control bits in a control register.

Sampling Mode	Sampling Clock
Internal	On-board timer generates a periodic clock at software-selectable rates from 381 to 100,000 samples per second (clocks per second); to 200,000 CPS on a 16-channel board with channel pairing*.
I/O Sample Clock	Clock is generated by setting a control register bit.
External Master	A front panel TTL-level input is available as an external clock. It can be software selected to generate a conversion on either the rising or falling edge. Front panel multiboard sample clock signals are used to synchronize multiple boards. Multiple boards will be sampled within 100 ns of the external master clock and within 50 ns of each other.
External Slave	Front panel multiboard sample clock inputs allow the VMIVME-3123 to be set up as a slave and clocked in tandem with a master board. The slave boards will be sampled within 100 ns of the external master clock and within 50 ns of each other. Up to two slave boards may be used as slaves in tandem with a master board.
2x (Channel Pairing)*	Provides alternate clocking of upper and lower 8 channels to support channel pairing (16-channel board only). Available for internal timer and external master clocks.

Operational Modes: The board uses five modes to perform a variety of tasks. They are listed as follows:

Idle: Host initialization

Burst: Used for capturing transient waveforms, uses triggers

Continuous Sample: Continuous data stream that does not use triggers

Calibration: Determines correction coefficients

Test: Performs self-test on analog input section and DRAMs

Trigger: Two bits in a control register determine the starting point for the data in the buffer when using burst mode. The buffer is continuously filled and the trigger marks the starting address for the desired position in the data buffer. The position of the trigger is user selected to be at the beginning, end, or middle of the buffer. The trigger is not to be used in continuous sample mode.

Built-in-Test: Three control bits are used to select one of the following inputs to all channels:
Normal field inputs
+9.9800 VDC
-9.9800 VDC
+4.9900 VDC
-4.9900 VDC
Zero

* Channel pairing is implemented by (a.) wiring input channels together in groups of two and (b.) by selecting the 2x mode, which effectively doubles the per-channel sample rate. The channel pairing option is only available on the 16-channel board.

Calibration: A board calibration sequence is performed upon host command. The calibration constants are accessible by the VMEbus. Calibration elapsed time is approximately 8 s.

Front Panel Indicator: A single control bit turns the front panel LED indicator ON or OFF. The indicator is turned ON automatically after any RESET operation.

CSR Reset: The board uses two bits in a hardware control register to perform hardware reset and Halt functions.

Active Channels: The active channels are selected by setting the corresponding bit in a 16-bit channel enable register. The host may enable channels in groups of 1, 2, 4, 8, or 16 active channels. The channels may be selected in any combination as long as the aforementioned groupings are adhered to. (An active channel is one which is digitized and stored in the data buffer.)

Buffer Size: Five control bits configure the data buffer size from one data sample to 4 million samples

Sampling Rate: In the *Internal Sample Clock Mode*, fourteen bits control the sampling rate from 381 to 100,000 SPS (200,000 SPS available with channel pairing on the 16-channel board only).

In all sample clock modes other than the internal mode, the sampling rate is controlled from zero to 200,000 SPS by external clock sources.

Buffer Flag Control: Two interrupt control bits (A and B) can be used by the host to determine when the data buffer is 50 or 100 percent filled. The interrupt request can be enabled for interrupt operation or disabled, and the A and B status bits polled by the host.

PHYSICAL/ENVIRONMENTAL

Dimensions: Standard VME double height board (160 x 233.5 mm)

Weight (Mass): 0.7 kgm maximum

Temperature: 0 to 65 ˚C, operating, -25 to +85 ˚C, storage

Relative Humidity: 20 to 80 percent, noncondensing

Cooling: Normal VMEbus chassis forced air circulation

Power Requirements: +5 VDC (+5/-2.5 percent) at 5.0 A maximum

Altitude: Operation to 3,000 m

MTBF: >63,000 hours (217F)

TRADEMARKS

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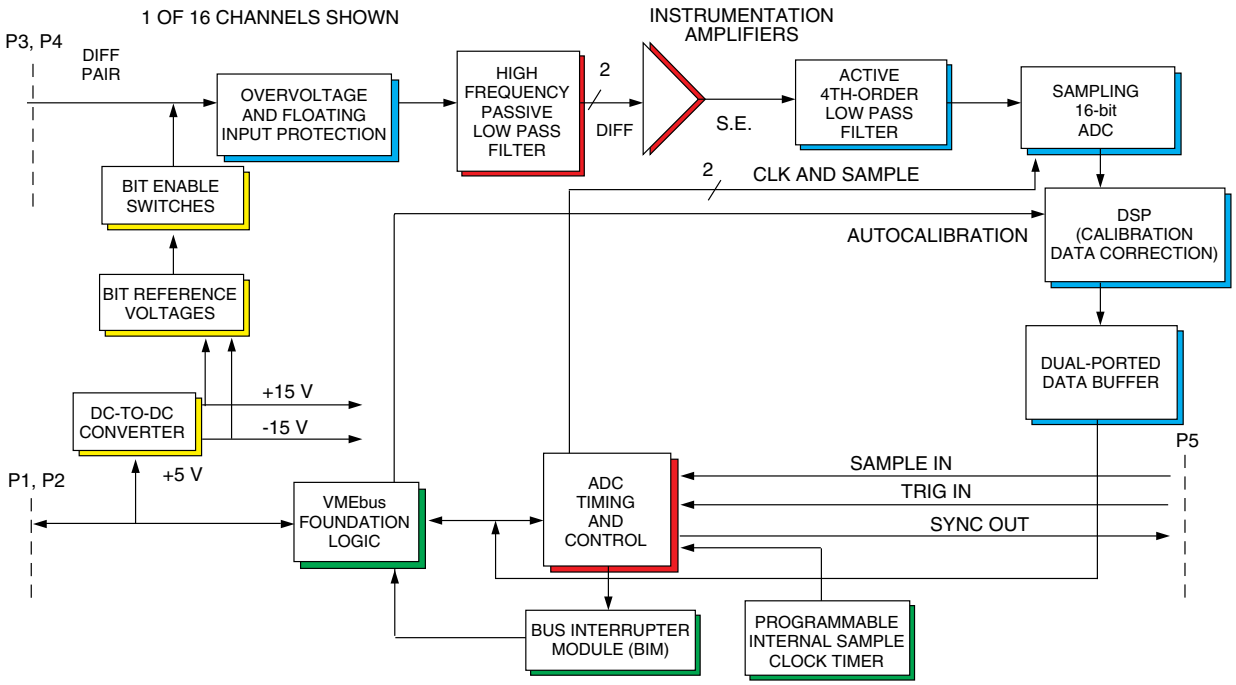

Figure 1. VMIVME-3123 Functional Block Diagram