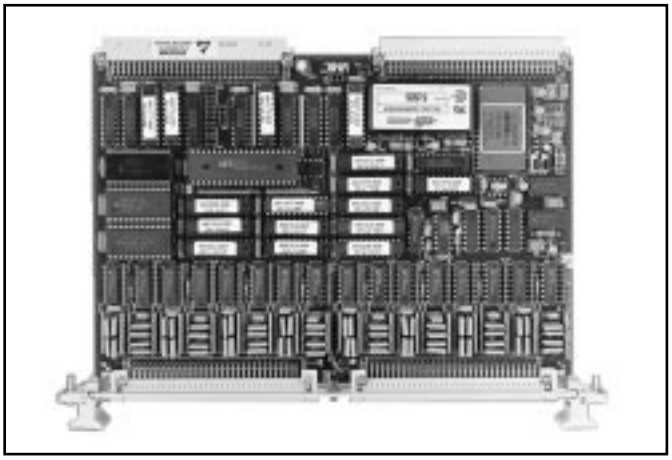
VMIVME-3128
Scanning 14-bit Analog-to-Digital Converter Board with Programmable Gain Memory

- 64 differential or single-ended inputs
- 14-bit A/D conversion
- 58 kHz conversion rate
- Program-selectable scanning of 16, 32, 48, or 64 channels
- Continually digitizes all input channels and stores the results
- Six operating modes
  - — Autoscanning mode
  - — Single channel random polling mode
  - — Timed burst mode
  - — Locally triggered burst mode
  - — Remotely triggered burst mode
  - — Gain loading mode
- Programmed VMEbus interrupts
- User-programmable interval timer
- Software-programmable gain 1, 10, 100
- External trigger to synchronize multiple boards simultaneously
- Jumper-selectable A/D ranges of 0 to +5, 0 to +10, ± 2.5, ±5, and ±10 V
- Optional low pass filter
- Overvoltage protected inputs
- 1,024-word data buffer (16-word deep buffer x 64 channels)
- Selectable output coding
- Powers up in autoscanning mode with gain of 1



APPLICATIONS

- Factory automation and instrumentation
- Process control and monitoring
- Laboratory instrumentation
- Machine monitoring
- Data acquisition and control

INTRODUCTION — This product is designed to support 64 channels of differential or single-ended wide range (±25 mV to ±10 V) analog inputs.

The board supports the following operating modes which are described below:

Autoscanning
Single Channel Random Polling
Timed Burst
Locally Triggered Burst
Remotely Triggered Burst
Gain Loading

One thousand and twenty-four dual-port Data Registers provide storage for continuous scanning of all channels. The scanning modes are executed automatically at powerup, system reset, or are entered under program control. The dual-port registers allow VMEbus access at any time to read the latest stored data.

Channel gain can be jumper selected as x1, x10, or x100, or can be software programmed individually for each channel. Scan rate is programmable up to 58 kCPS (thousand channels/s. Low pass input filters are available.

A functional block diagram is provided in Figure 1, and the Ordering Options are provided on the first page of this specification.

Ordering Options

April 14, 1998 800-003128-000 E	A	B	C	–	D	E	F
VMIVME-3128*	–		0		–			

A = Input Filter Options
0 = No Filter
1 = 10 Hz ±24% (-3 dB)
2 = 50 Hz ±24% (-3 dB)
3 = 100 Hz ±24% (-3 dB)
4 = 500 Hz ±24% (-3 dB)
9 = 1.6 kHz ±24% (-3 dB)
B = 0 (Option reserved for future use)
C = Input Option
0 = 64 Diff/SE Analog Input Channels
1 = 64 SE Analog Inputs with Improved High Frequency Rejection

Connector Data

Style	Recommended Connecting Component	P3 and P4 I/O Connectors
64-pin IDC	Mating Connector (64-pin) Strain Relief (for 64-pin Connectors)	Panduit 120-964-435E Panduit 100-000-032
96-pin Discrete Wire	Mating Connector (96-pin Discrete) Female Crimp Contacts (96-pin Discrete)	AMP 925486-1 AMP 530151-6 **
	Connector Housing (for 96-pin Connectors)	Harting 09 03 096 0501
96-pin IDC	Mating Connector (96-pin Mass Terminated)	ERNI 913.031
	0.033-inch Ribbon Cable (96-pin Mass Terminated)	ERNI 913.049
	Strain Relief Insert (0.033-inch Ribbon Cable)	Harting 09 02 000 9912
	Connector Housing (for 96-pin Connectors)	Harting 09 03 096 0501
	PC Board I/O Connector Part Number	Panduit 101-096-033A

Notes

* -9BC must be ordered when VMIC signal conditioning products are coupled with the VMIVME-3128.
** AMP crimp tool part number 90301-2.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com
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The VMIVME-3128 employs an unbuffered 64-channel input multiplexer. Systems Integrators must consider source impedances and cable length when using this board unless the VMIVME-3413, VMIVME-3417A, VMIVME-3418, or other signal conditioning is used. If these signal conditioning products are used with the VMIVME-3128, then the VMIVME-3128-9BC must be ordered. In those applications where no signal conditioning board is used or where extremely low noise is required, VMIC recommends the VMIVME-3122.

FUNCTIONAL CHARACTERISTICS

(Typical at +25 °C and rated power supplies, unless otherwise stated.)

Operating Modes:

Autoscanning Mode: This default operating mode is selected by a reset operation, or by clearing both CSR Mode control bits. All active channels are scanned continuously in this mode, and any channel value can be read at any time.

Single Channel Random Polling Mode: Each input channel is accessed individually, and the digitized channel value is read from the Converter Data Register (CDR).

Timed Burst Mode: A single data burst (scan of all buffer locations) is acquired at the end of a programmed interval, or the process can be repetitive.

Locally Triggered Burst: A single burst is initiated through the Control and Status Register (CSR).

Remotely Triggered Burst: A single data burst (scan of all enabled channels) is initiated through the P2 connector by an external TTL trigger source.

Gain Loading Mode: If the board is jumper configured for automatic gain control, gain loading is performed by first selecting the gain loading mode, and by then loading the gain code for each channel into a 64-location gain buffer. The gain codes (0 for x1, 1 for x10, 2 for x100) for all channels are initialized to *zero* (gain = x1) automatically after a reset operation.

Channel Autogain: The unique gain code for each channel is loaded from the VMEbus into a gain buffer (see Gain Loading Mode). The assigned code is retrieved from the buffer in real-time for each channel acquisition.

Synchronization: A single scan or burst, can be initiated by an external TTL trigger through the P2 connector (Remotely Triggered Burst), or locally through the CSR (Locally Triggered Burst). Either event generates a P2 *trigger* output, which can be used to synchronize up to 15 boards.

Board Address: Jumper located on word boundary anywhere in the short I/O A16 space, or the standard A24 space. Required word boundary is 1000h in either space.

VMEbus Access: Response to address modifiers is jumper-selectable as:

Short I/O A16 or standard A24 address space
Supervisory or user privilege, or both
Data or program access

VMEbus Compliance: This product complies with VMEbus Specification ANSI/IEEE STD 1014-1987 IEC 821 and 297 with the following mnemonics:

A24/A16:D16/D8 (EO) DTB Slave
Interrupter I(1 to 7) ROAK (DYN)
Interrupter Vector: D08 (O) (DYN)
6U form factor

VMEbus Interrupt: An interrupt request can be generated at the end of a buffer scan in all modes except autoscanning mode. Response vectors are controlled through Interrupt Vector Registers.

Data Ready Flag: A data ready flag in the CSR is set when the data buffer is filled (endscan) or half-filled (midscan).

Interval Timer: Bursts intervals of up to 536 s are provided by a programmable interval timer.

Reset Operations: Board reset occurs in response to a system reset or by setting a *reset* bit in the CSR. For programming-free initial operation, a reset operation automatically establishes the following default conditions:

Autoscanning mode
64-channel block size
64-channel data buffer
Channel Gain = x1

PGA: Channel gains of x1, x10, and x100 are selected through a Programmable Gain Amplifier (PGA). PGA gain can be jumper configured with a single gain for all channels, or it can be controlled in real-time with unique gains assigned for each channel. See *Channel Autogain*.

Panel Indicator: Program-controlled front panel LED is energized during reset, and is extinguished through the CSR.

Board Identification: A Board Identification Register (BIR) contains the VMIVME-3128 identification code.

INPUT CHARACTERISTICS

Number of Input Channels: 64 differential or single-ended channels

Full-Scale Input Ranges: ±2.5, ±5, ±10, 0 to +5, 0 to +10 V; jumper-selectable

Channel Gain: Program selected or jumper selected as x1, x10, or x100. See *Channel Autogain*.

Full-Scale Input Range: ±25 mV to ±10 V

Input Offset Voltage:
(0.3 + 6/G + 0.6 k) mV;
where: G = PGA gain
K = Sample rate per channel, KSPS
e.g.: The maximum input offset voltage with a PGA gain of x10 and a sample rate of 0.5 KSPS per channel would be 1.2 mV (0.3 + 0.6 + 0.3)

Input Bias Current: 50 nA maximum at zero input

Input Impedance: 5 MΩ in parallel with 50 pF

Input Noise: 0.3 mV RMS, DC to 100 Hz

Input Filters: Optional low pass single-pole filters:

-3 dB at 10 Hz ±24%
-3 dB at 50 Hz ±24%
-3 dB at 100 Hz ±24%
-3 dB at 500 Hz ±24%
-3 dB at 1.6 kHz ±24%

Overvoltage Protection:

	Sustained Overvoltage Maximum	
Option	Power On	Power Off
-000	±16 V	±4 V
-100	±31 V	±23 V
-200	±21 V	±10 V
-300	±21 V	±10 V
-400	±21 V	±10 V
-900	±16 V	±4 V
-001	±24 V	±16 V
-101	±40 V	±33 V
-201	±24 V	±16 V
-301	±24 V	±16 V
-401	±24 V	±16 V
-901	±17 V	±5 V

TRANSFER CHARACTERISTICS

Resolution: 14 bit

Input Sampling: Sequential, starting at channel 00

Integral Nonlinearity: ±0.005 percent maximum; from best straight line

Differential Nonlinearity: ±0.0015 percent; typical at MSB transition

Quantization Error: ±1/2 LSB

Missing Codes: None

Conversion Cycle Time*: 17 µs, total time for acquisition, A/D conversion, and storage

A/D Conversion Rate: 58 KSPS (thousand samples per second)

Channel Sample Rate (Maximum): 3.625 KSPS (58 KSPS ÷ number of channels in scanning block, 16 channels minimum)

Timed Burst Interval: 305 µs to 536 s

Interchannel Crosstalk:

Filter Option	Cross Talk (Maximum) (Adjacent Channels)	Cross Talk (Maximum) (Alt. Channels)
None	-80 dB	-110 dB
10 Hz	-70 dB	-110 dB
50 Hz	-70 dB	-110 dB
100 Hz	-70 dB	-110 dB
500 Hz	-70 dB	-110 dB
1.6 kHz	-77 dB	-110 dB

Common-Mode Voltage: CMV = ±9 V; maximum input voltage = ±11 V on either input line for linear operation.

Common-Mode Rejection: CMRR = 82 dB, DC to 100 Hz, 64-channel block size.

Data Coding: Program selectable as two's complement, or straight/offset binary. 14-bit data is left-justified in a 16-bit data word.

ACCURACY

PGA Nonlinearity, DC:
G=1: ±0.005 percent FSR (Full-Scale Range)
G=10: ±0.005 percent FSR
G=100: ±0.01 percent FSR

* Each channel is sampled during the A/D conversion of the preceding channel.

Gain Accuracy (Including Nonlinearity):
G=1: ±0.008 percent FSR
G=10: ±0.06 percent FSR
G=100: ±0.06 percent FSR

STABILITY (Over Temperature Range)

PGA Offset Voltage Drift: ±(3 + 15/G) µV/°C

System Accuracy Drift:
G=1: ±20 PPM/°C
G=10: ±50 PPM/°C
G=100: ±90 PPM/°C

Total Noise: 4,500 µV maximum at GAIN = 1 and FS = ±10 V

DATA BUFFER MEMORY

Buffer Size: 16 to 1,024 contiguous 16-bit data words, in six equal ratios of 2:1; program controlled.

Block Size: 16, 32, 48, or 64 channels; program controlled.

VMEbus Access: D8 or D16

Availability: Accessible at any time from the VMEbus. Buffer and block sizes are controlled through a Buffer Control Register (BCR).

PHYSICAL/ENVIRONMENTAL

Temperature:
0 to +55 °C, operating (standard VME slot)
-40 to +85 °C, storage

Humidity: 10 to 80 percent relative, noncondensing

Altitude: Operation to 10,000 ft (3,048 m)

Cooling: Forced air convection (standard VMEbus slot)

Dimensions: Double height Eurocard (6U) board, 160 x 233.35 mm

Input Connectors (P3, P4): 96-pin DIN connector, center row grounded (accepts 64- and 96-pin mating connectors).

Power Requirements: 4.0 A (maximum) at +5 VDC

MTBF: 131,900 hours (217F)

TRADEMARKS

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APPLICATION AND CONFIGURATION GUIDES — The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Board Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006
Integration of the VMIVME-5588 with GE Fanuc PLC	825-000000-025
Data Acquisition Noise Reduction Application Guide	825-000000-026
IOWorks Base Package Application Guide	825-000000-027
IOWorks Systems Application Guide	825-000000-028

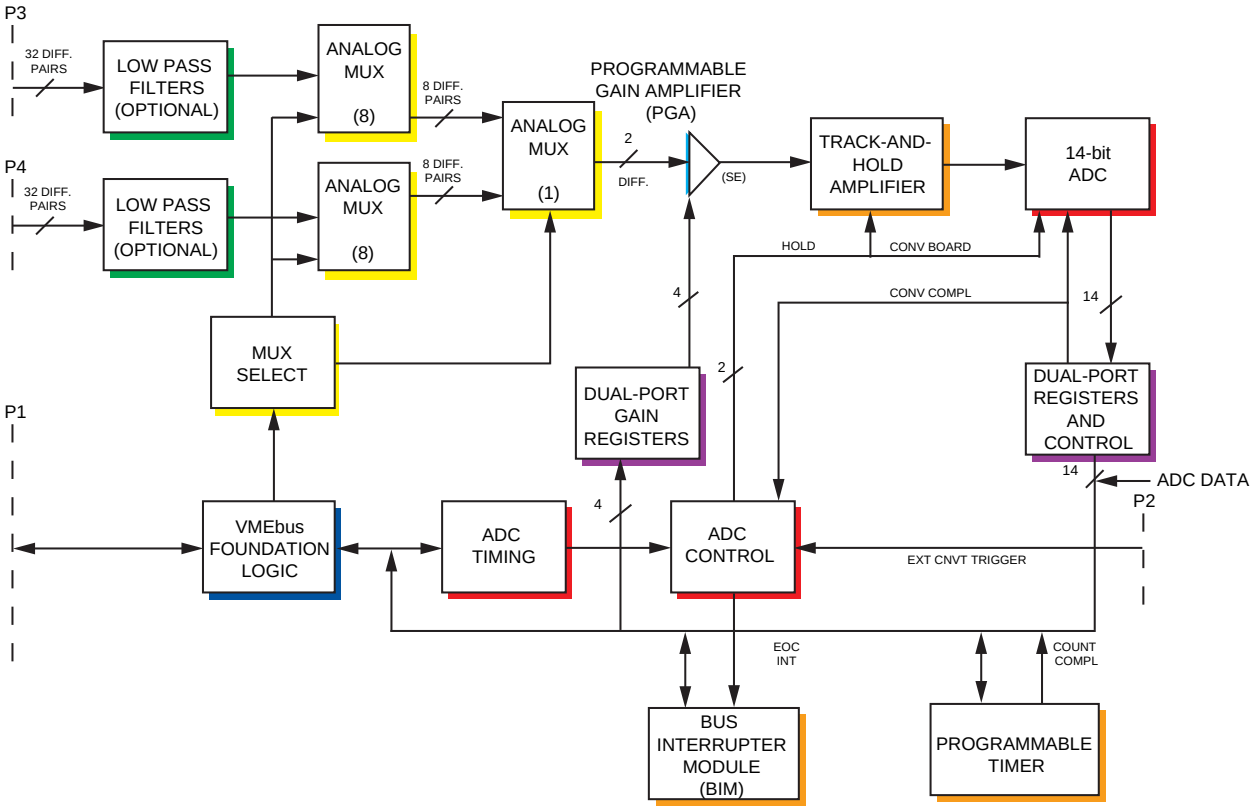

Figure 1. VMIVME-3128 Functional Block Diagram

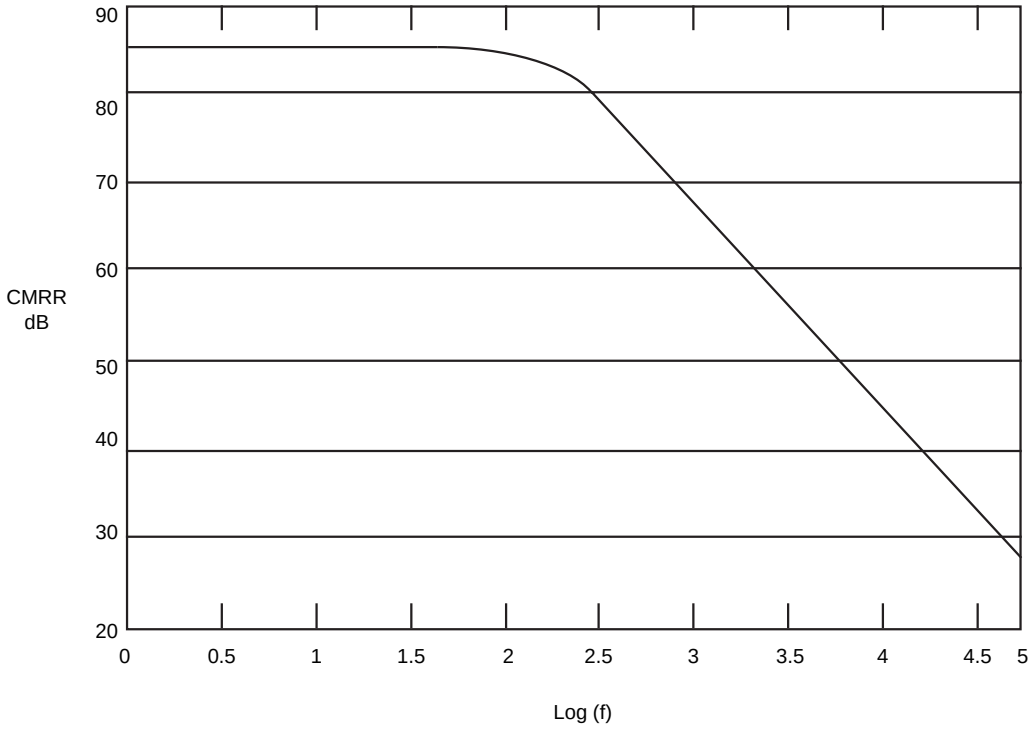

Figure 2. VMIVME-3128 Common-Mode Rejection Ratio Versus Frequency