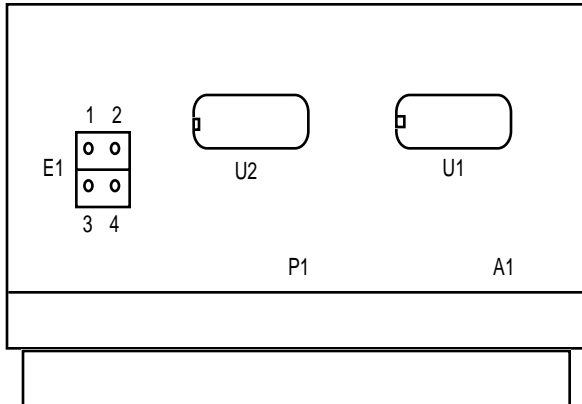- BERRs any data cycle that lasts longer than time limit
- Time limit jumper selectable: nominally 5, 50, or 500 μs
- VMEbus compatible (ANSI/IEEE Std 1014-1987 IEC 821 and 297)
- Uses no VMEbus slot space. Plugs directly onto the rear of the P1 backplane. Requires P1 backplane with extended pin on the rear of P1.

Component side view:

INSTRUCTIONS FOR USE:

You must have a backplane that has wirewrap pins on the back of J1 at slot 1.

Set the jumpers on the VMIACC-0300 for the nominal timeout desired. Refer to the component side view above.

E1-1 to E1-2	E1-3 to E1-4	NOMINAL TIMEOUT
INSTALLED	REMOVED	5 μs
INSTALLED	INSTALLED	50 μs
REMOVED	REMOVED	50 μs
REMOVED	INSTALLED	500 μs

The module is shipped with both jumpers installed, for 50 μs nominal delay.

Be sure the backplane power is OFF.

Hold the module so the end of the connector marked A1 is aligned with the wirewrap pin at J1-A1. Slant the module slightly, so the A1 end can be carefully worked onto J1-A1, and the other end is slightly away from J1-A32. Rock the
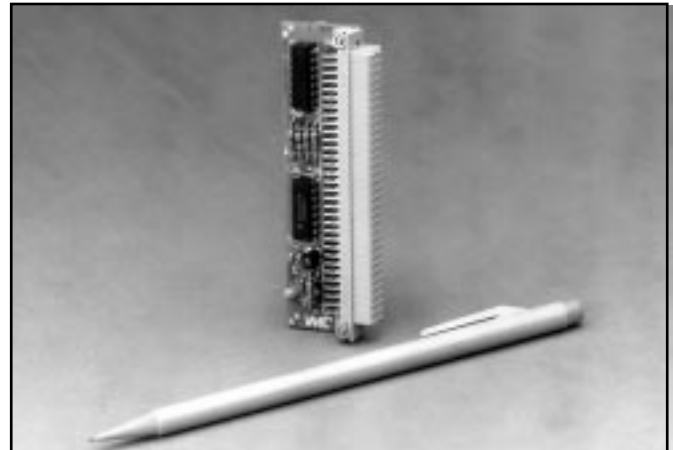
module from side-to-side slightly as you mate the module with the pins, row-by-row, until all are started correctly into the VMIACC-0300 connector. Then push the module onto the pins as far as it will easily go (about 6 mm).

This completes the VMIACC-0300 installation. The VMIACC-0300 will terminate any bus data cycle that exceeds the nominal timeout period with a BERR* signal.

TRADEMARKS

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Ordering Options
Sept. 3, 1993 800-800300-000 A
VMIACC-0300
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