VMIVME-2510B
64-bit TTL Digital I/O with Built-in-Test

- The Direction of Each 8-bit Port is Individually Programmable
- 64 mA Sink Capability
- Separate Board Address Decoding for Control and Data Registers
- Built-in-Test Logic for Fault Detection and Isolation
- Fail LED
- Compatible with VMIC's Intelligent I/O Controller Product Line
- High Reliability DIN Type I/O Connections
- 8-, 16-, 32-bit Transfers
- Optional Open-Collector Outputs

FUNCTIONAL CHARACTERISTICS

Compatibility: VMEbus specification compatible double-height form factor

I/O Connector Type: Dual 64-pin connector, DIN 41612

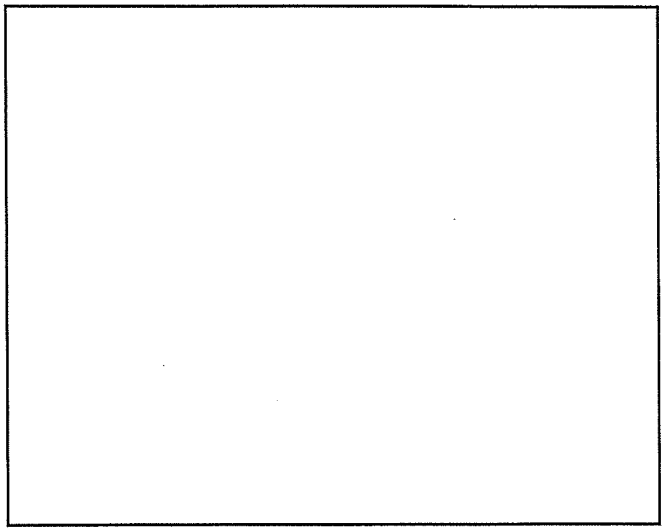
I/O Organization: Eight I/O ports; eight bits wide. Addressable to any address within short supervisory or short nonprivileged I/O map.

Addressing Scheme: Eight ports individually addressable on 8- or 16-bit boundaries. Address DIP switches provide unlimited short data I/O address map selection.

Built-in-Test: Output data may be read back in real-time or in an off-line mode. The off-line mode is enabled by executing a write to the Control and Status Register (CSR) to set the TEST MODE bits. With the TEST MODE enabled, all outputs are in TRI-STATE. Two TEST MODE bits are provided so that each connector I/O (32 bits) can be tested independently if necessary.

Fail LED: A Fail LED is provided that is illuminated at power up and system reset. It may be extinguished under program control upon a successful diagnostic execution.

I/O Circuit: Transceivers support high current sink (64 mA) outputs. These octal bus transceivers are SN74AS645 for the logic level TTL I/O option. The open-collector option uses SN74AS641 type transceivers. If the open-collector option is ordered, all 64 bits are output only.



Variations: This product may be purchased in the following variations:

Model No.	Description
2510	Original Design - one test mode bit
2510A	Two test mode bits (one per connector)
2510B	Recommended for new designs (two test mode bits)

ORDERING INFORMATION

October 28, 1994 800-000103-000 C	A	B	C	-	D	E	F
VMIVME-2510B -			**0**	-			

A = Input/Output Type and Data Polarity
1 = TTL Logic Level Inputs and Outputs, Positive True
2 = TTL Logic Level Inputs and Outputs, Negative True
3 = Open-Collector Outputs (No Inputs), Positive True *
4 = Open-Collector Outputs (No Inputs), Negative True *

B = Output Resistor
0 = No Resistors Installed
1 = 2.2 kΩ**

C =
0 = Not Used

NOTES

* 10-pin SIP sockets are provided for user-installed pull-up resistors. Inputs are active once pull-up resistors are installed.

** Must select open-collector Input/Output.

CONNECTOR DATA

Compatible Cable Connector	Panduit No. 120-964-435E
Strain Relief	Panduit No. 100-000-032
PC Board Header Connector	Panduit No. 120-964-033A

For Ordering Information, Call:
1-800-322-3616 or 1-205-880-0444 • FAX (205) 882-0859

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to 55 °C, operating -20 to 85 °C, storage

Relative Humidity Range: 20 to 80 percent, noncondensing

Cooling: Convection

Power Requirements: +5 V at 3.786 A (maximum)

POSITIVE/NEGATIVE TRUE ORDERING INFORMATION TTL I/O — This board may be ordered with positive or negative true I/O options. A positive true input option presents a high-level input voltage on each data line whose corresponding bit on the VMEbus is a logic "one". A positive true output option presents a logic "one" to the Output Data Register (ODR) which presents a high-level output voltage on each data line. A negative true input option presents a high-level input voltage on each data line whose corresponding bit on the VMEbus is a logic "zero". A negative true output option presents a logic "zero" to the Output Data Register which presents a high-level output voltage on each data line.

OPEN-COLLECTOR OUTPUT OPTION — A positive true output option presents a logic "one" to the ODR whose corresponding bit on the VMEbus is a logic "one", which turns the output open-collector transistor ON, thereby supplying a ground to the load.

A negative true output option presents a logic "zero" to the ODR whose corresponding bit on the VMEbus is a logic "one", which turns the open-collector output transistor OFF.

IIOC COMPATIBILITY — This product is compatible with VMIC's family of Intelligent I/O Controllers (IIOCs) which have applications in the data acquisition, process control, factory automation, and simulation and training markets. IIOC software support for this product is designed to support I/O as shown below:

CONNECTOR	
P3	P4
I	I
O	I
I	O
O	O

This concept allows the user to downline load the direction of I/O on each connector; therefore, individual port control is not supported by the IIOC. IIOC support is limited to the VMIVME-2510A or -2510B models. The IIOC is a multiprocessor controller that includes CPU(s), global memory(s), a wide variety of optional host computer interfaces and firmware that provides a total "turnkey" I/O solution. More information concerning this product may be obtained by requesting the Intelligent I/O Controller Instruction Manual, Document No. 500-009016-000.

TRADEMARKS

APPLICATION AND CONFIGURATION GUIDES — The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Board Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

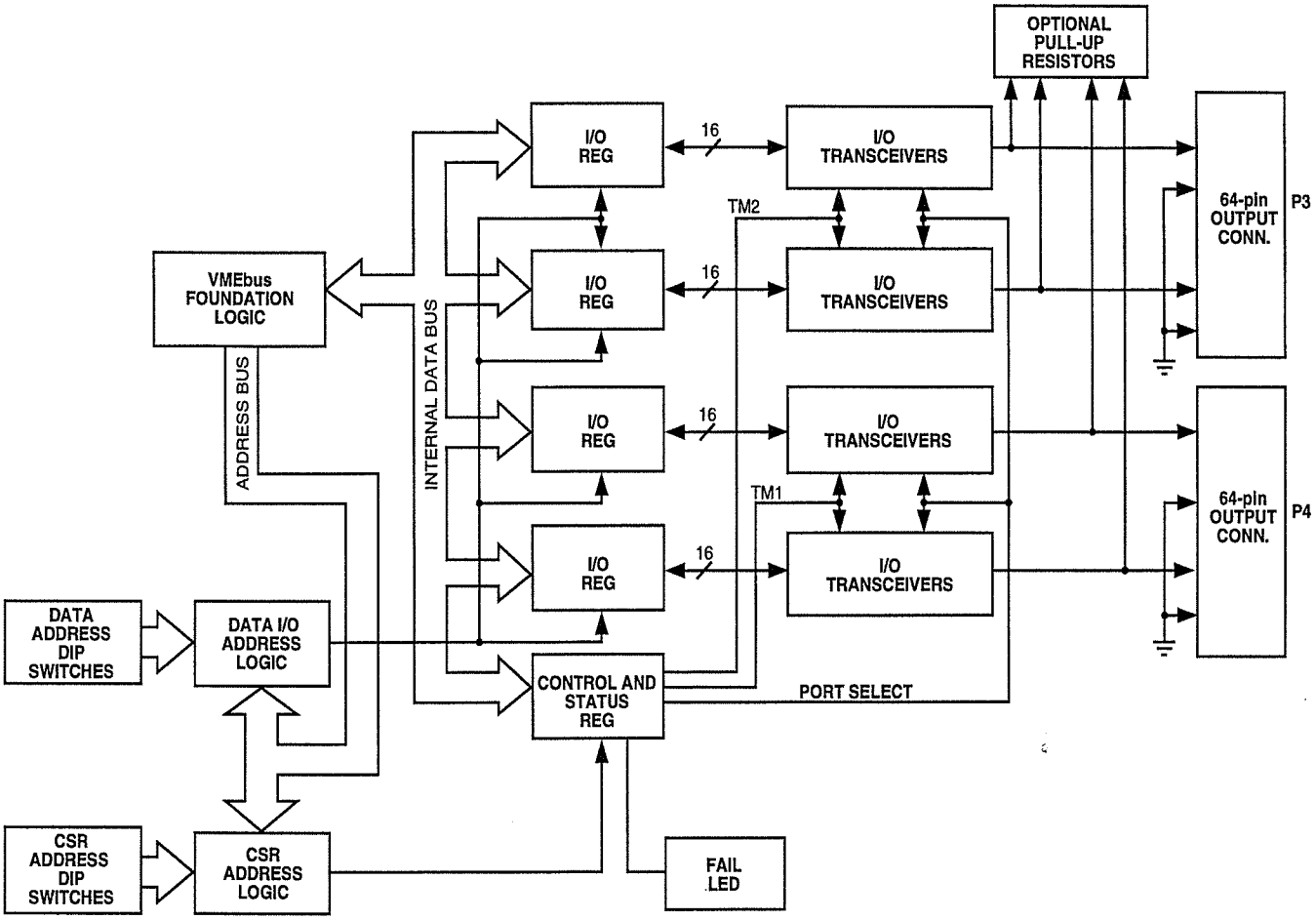


Figure 1. VMIVME-2510B Functional Block Diagram

VMIVME-2510B

64-BIT TTL I/O MEGAMODULE™

INSTRUCTION MANUAL

DOCUMENT NO. 500-000103-000 L

Revised March 5, 1997

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, AL 35803-3308
(205) 880-0444
1-800-322-3616
FAX NO.: (205) 882-0859

COPYRIGHT AND TRADEMARKS

(I/O man figure)

(IOWorks man figure)

(VMIC logo)

UIOC® *WinUIOC*®

VME Microsystems International Corporation

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	05/02/89	Release Manula	89-0003
B	05/02/89	Appendix A	89-0004
C	08/14/89	Cover, Page ii, Section 6, and Appendix A	89-0104
D	07/12/90	Cover, Page ii, and Appendix A	89-0194
E	12/18/90	Cover, Page ii, TOC, 2-1, 2-3, 2-5, Section 6, Appendix A, Renumber Tables and Figures	90-0180
F	03/27/91	Cover, Pages ii, vii, and Section 5	91-0095
G	08/13/91	Cover, Pages ii, 1-2, and Appendix A	91-0215
H	04/22/92	Cover Page ii, Sesctions 2, 6, and Appendix A	92-0099
J	02/16/94	Entire Manual Updated	94-0222
K	10/09/95	Cover, Pages ii, vi, 5-4, 5-5, and Section 6	95-0587
L	03/05/97	Cover, Pages ii and 4-5	97-0239

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

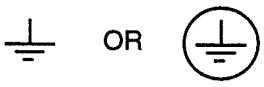
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

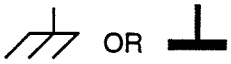
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



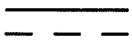
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

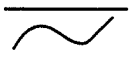


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

VMIVME-2510B
64-BIT TTL I/O MEGAMODULE™

TABLE OF CONTENTS

TABLE OF CONTENTS (Concluded)

LIST OF FIGURES

LIST OF TABLES

APPENDIX

SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-2510B is a VMEbus compatible 64-Bit TTL Input/Output Board. Its features include:

a. The direction of each 8-bit port is individually programmable
b. 64 mA sink capability (15 mA source)
c. Separate board address decoding for control and data registers
d. Built-in-test logic for fault detection and isolation
e. Fail LED
f. Compatible with VMIVME-9016 intelligent I/O controller
g. High reliability DIN type I/O connectors
h. 8-, 16-, 32-bit transfers
i. Optional open collector outputs

1.2 FUNCTIONAL DESCRIPTION

The 2510B is a member of VMIC's Megamodule™ family, which is designed with common programming features. Subsystems may be configured with contiguous I/O addresses to conserve memory. Each of these products (1110, 2120, 2130, and 2510B) are designed with two sets of board address switches to provide an efficient memory address map for CSR and I/O addresses. CSR address switches may be set such that all CSR's among a variety of boards in a system may be mapped into contiguous memory locations.

The Megamodule™ product is also designed to support 8-, 16-, and 32-bit data transfers. Specific hardware has been designed into the 2510B to support built-in-test functions. The 2510B supports both off-line and on-line fault detection and isolation. A front panel Fail LED is used to indicate when a fault exists on this board. Upon power-up or reset, the LED is illuminated. After successfully completing board-level diagnostics, the LED can be extinguished.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-In-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-000103-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW

As shown in the functional block diagram in Figure 3.1-1, the VMIVME-2510B provides for the control/monitoring of 64 output/input lines via eight 8-bit data registers. These 64 bits of I/O are addressable as two 32-bit long words, four 16-bit words, or as eight 8-bit bytes. These eight registers are selected by address bits A2, A1, DS0 and DS1.

Direction control of I/O is on a byte basis. Eight direction control bits in the CSR select whether an octal port is to be input or output. In addition, the CSR contains a Fail LED bit, two test mode bits, and five storage bits that can be used for message passing between VMEbus masters.

3.1.1 Built-in-Test

The built-in-test feature of the VMIVME-2510B is enabled by asserting the Test Mode (TM) bits in the CSR. Test Mode P3 controls the transceivers for connector P3, while Test Mode P4 controls the P4 transceivers. While in the Test Mode, the I/O transceivers are disabled, allowing data to be looped back through the I/O Data Registers for test purposes without disturbing the device being controlled. A port must be configured for output before loopback testing can be done. This requires a logic "one" to be written to the appropriate control bit of the CSR. The Test Mode and the Fail LED (FL) bits are initialized active (logic "zero") by system reset. The design of the Built-in-Test hardware supports off-line and on-line fault detection and isolation and on-line fault isolation.

3.2 BOARD ADDRESSING

The VMIVME-2510B is designed to support data transfers in supervisory or non-privileged short I/O memory space. A jumper is provided as shown in Figure 3.2-1 (Address Selection Block Diagram) to allow user selection of either I/O access type. The jumper (J1) is shown on the logic diagram in Appendix A. The VMIVME-2510B is factory configured (Jumper J1 is not installed) to respond to short-supervisory I/O access.

The VMIVME-2510B is designed with two sets of board select switches and decode logic, as shown in Figure 3.2-1, to provide an efficient memory address map for CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into contiguous memory locations when configuring subsystems that require more than one board.

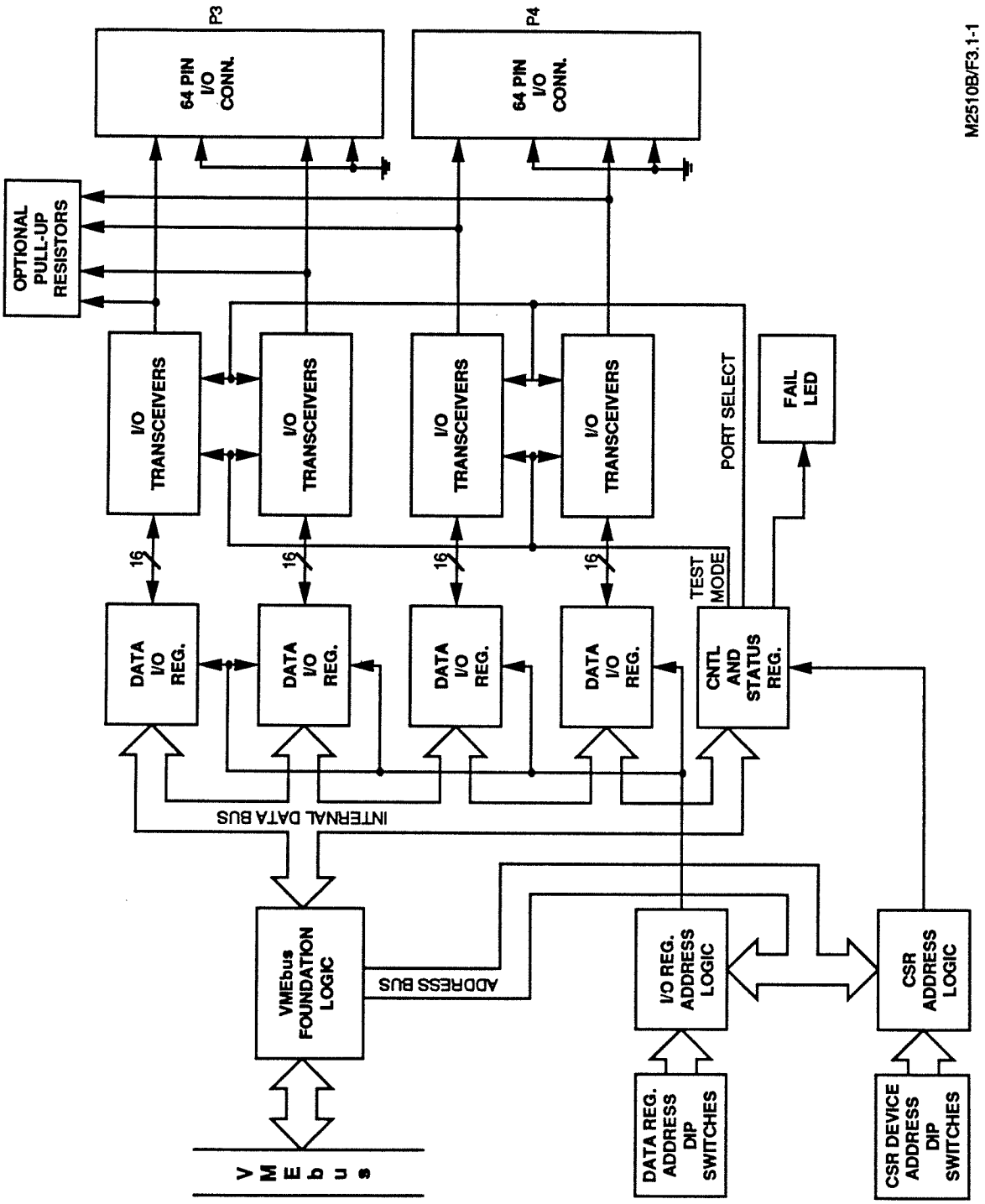


Figure 3.1-1. Functional Block Diagram

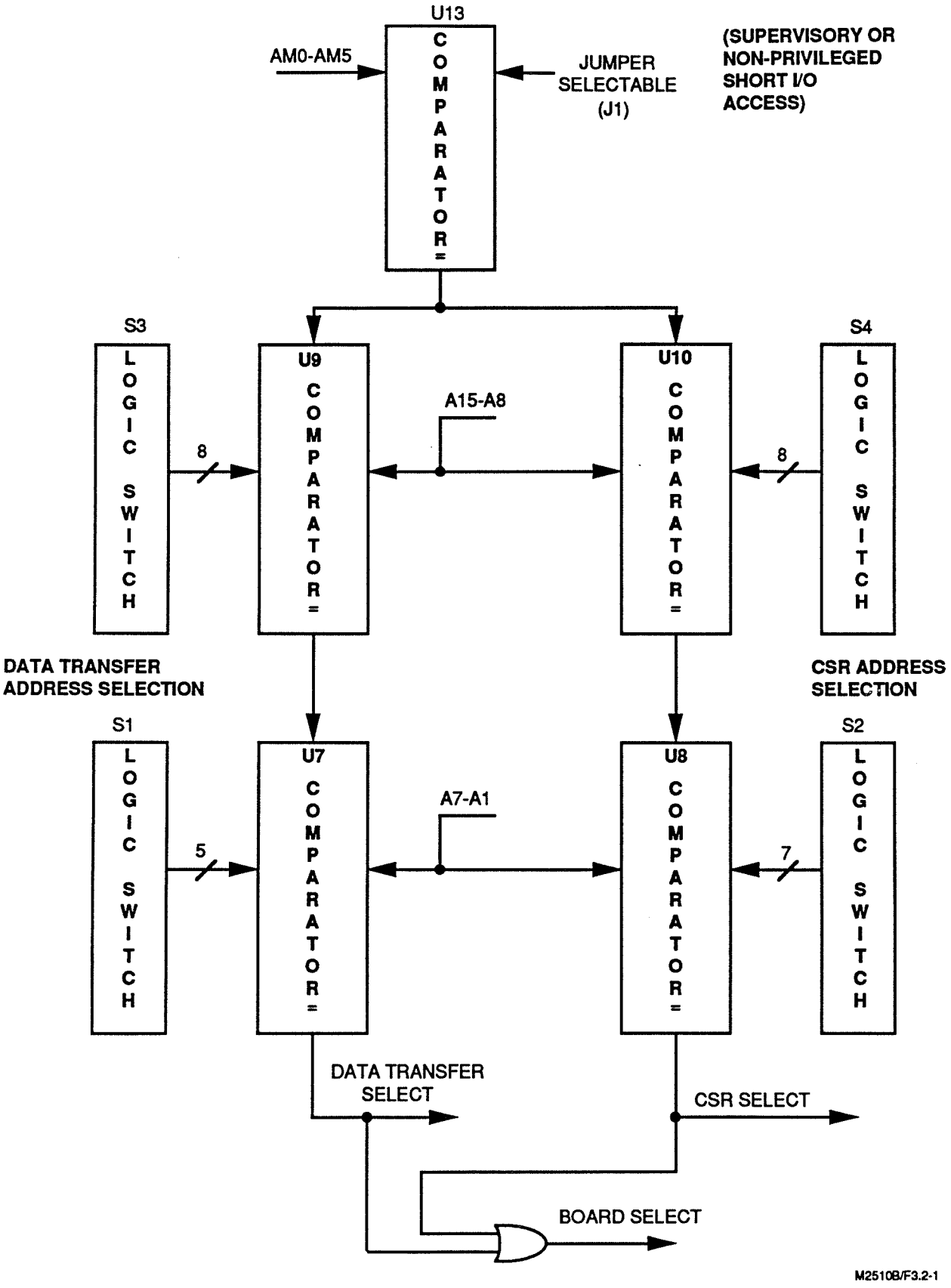


Figure 3.2-1. Address Decoder Block Diagram

3.3 VMEbus COMPATIBILITY LOGIC

Typical VMEbus drivers, receivers and control logic are shown in Figures 3.3-1, 3.3-2, and 3.3-3.

3.4 DATA TRANSFERS

Data transfer transceivers are shown in Figure 3.3-3. The data transceivers are designed to support write and read operations on 8-, 16-, and 32-bit boundaries.

3.5 I/O REGISTERS CONTROL LOGIC

The VMIVME-2510B is designed utilizing the AMD2952 dual-rank octal bi-directional bus latch. The control logic shown in Figure 3.5-1 is designed to support I/O transfers to eight 8-bit registers. To simplify the control logic design, the read and write control logic is separated to take advantage of the 2952's control lines. As shown in Figure 3.5-1, U6 separates the control signals into write and read register strobes, and U22 provides additional control logic to allow 8-, 16-, and 32-bit data transfers.

3.6 CONTROL AND STATUS REGISTER (CSR)

The CSR is a 16-bit read/write data register that is independently selectable as described in Section 3.2. The CSR controls the direction of data transfers on each 8-bit I/O port, the Built-in-Test operations, and the front panel Fail LED. Bits 0 through 4 are not used for on-board operations; therefore, the user may program these bits as system resource flags, or semaphores, if required. The CSR is initialized active (outputs are logic "zeros") by a system reset. This enables both Test Mode bits, which places the transceivers in the TRI-STATE mode, and lights the front panel Fail LED. CSR control logic is shown in Figure 3.6-1.

3.7 I/O DATA REGISTERS AND TRANSCEIVERS

The VMIVME-2510B is designed utilizing eight octal bi-directional registers (AMD 2952), as shown in Figures 3.7-1 through 3.7-4. The I/O data port of each register is connected to an I/O transceiver as shown in Figures 3.7-2 and 3.7-4. These transceivers provide the I/O buffering for the data received from, or transmitted to, the user device connected to the P3 and P4 front panel connectors. The VMIVME-2510B may be ordered with open collector outputs and optional pull-up resistors as shown in Figures 3.7-2 and 3.7-4; however, this option is available as 64 output bits only.

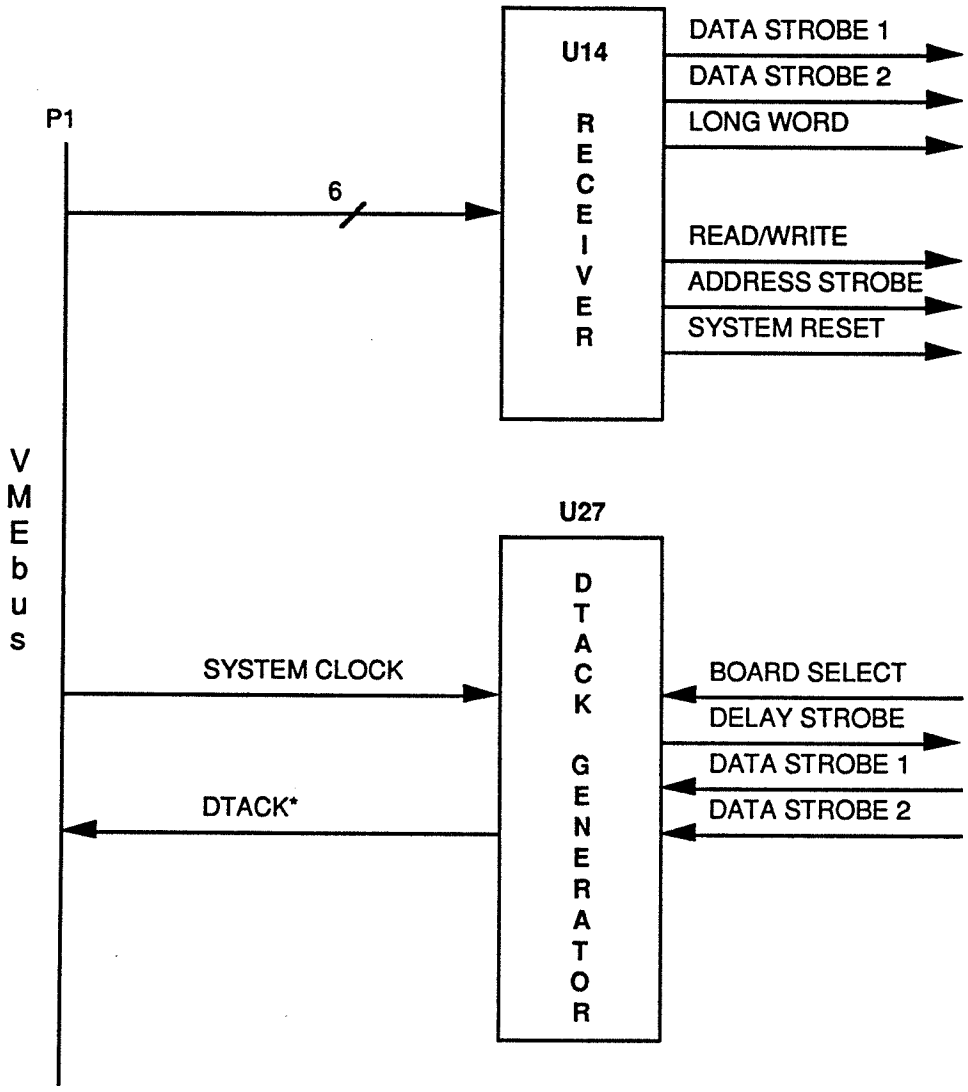


Figure 3.3-1. Control Section Diagram

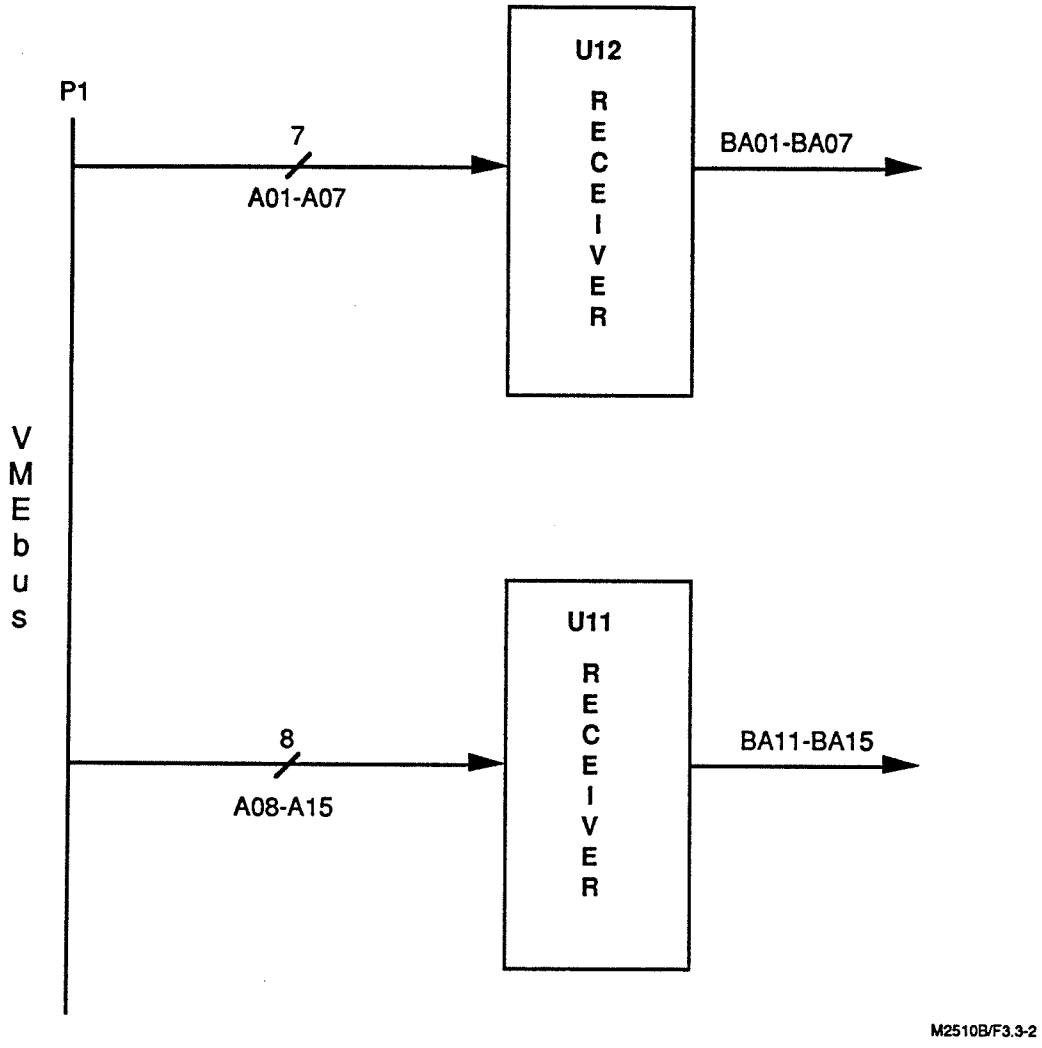


Figure 3.3-2. Address Receiver Block Diagram

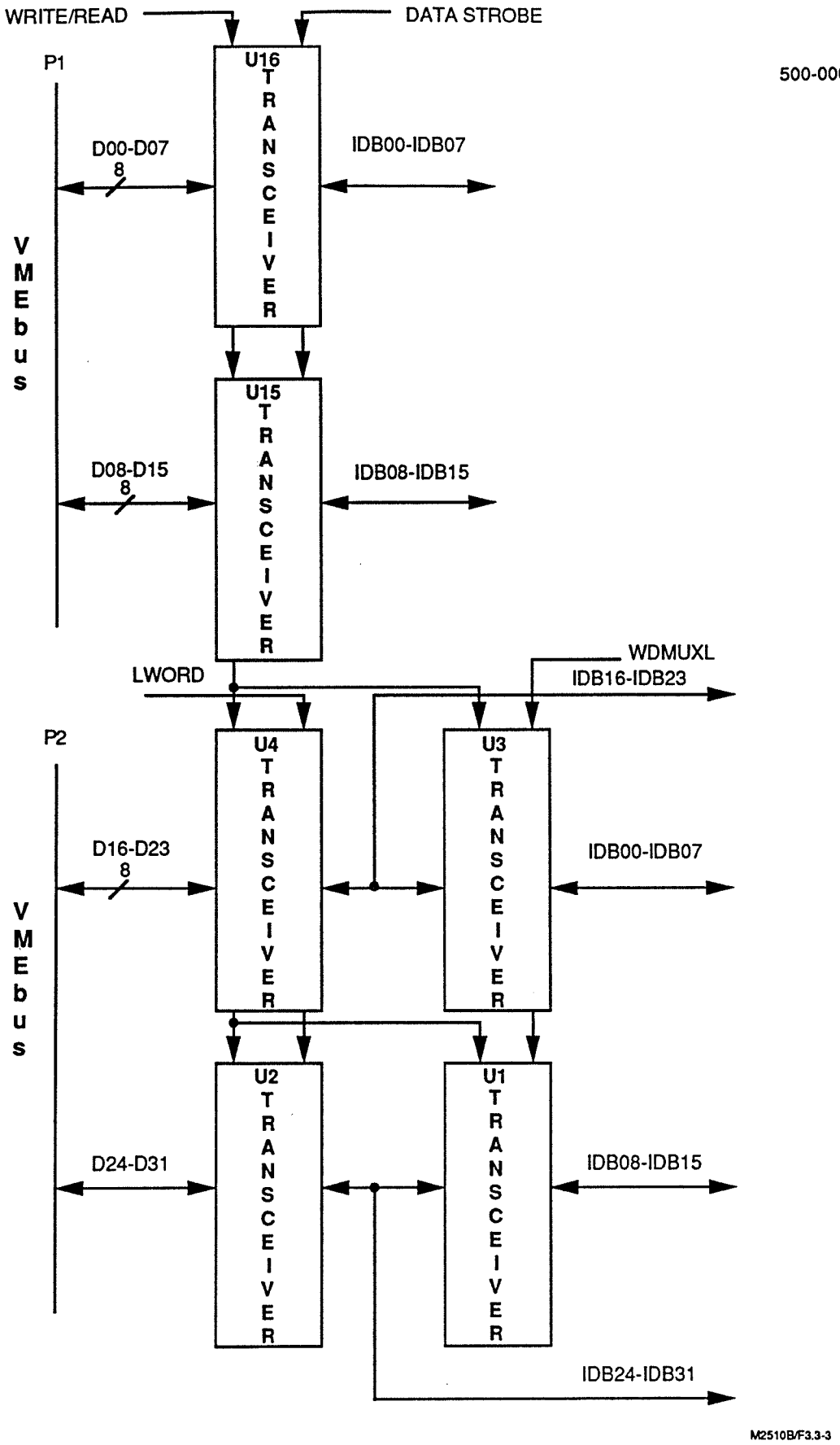


Figure 3.3-3. Data Transfer Block Diagram

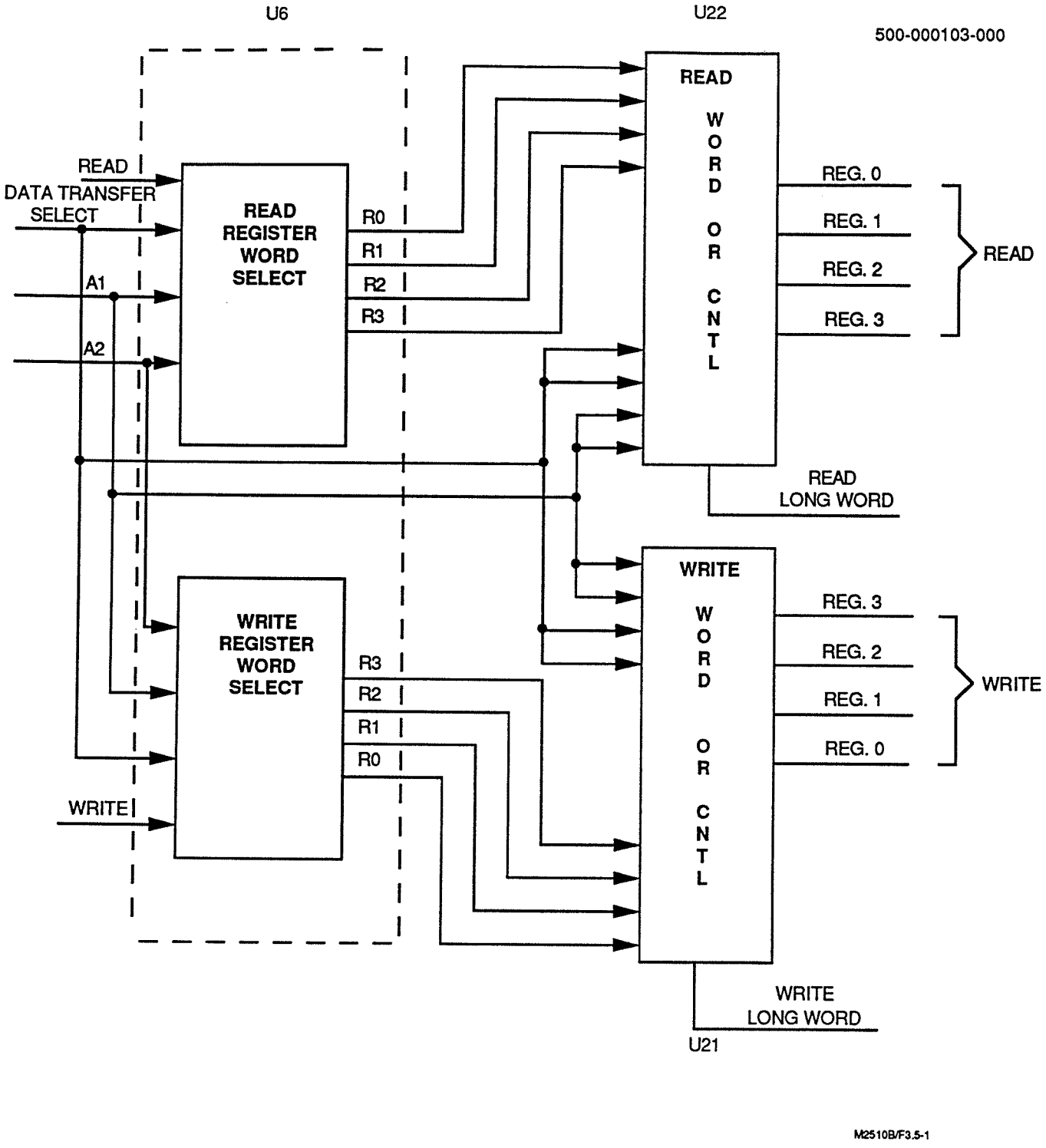


Figure 3.5-1. I/O Register Control Logic Block Diagram

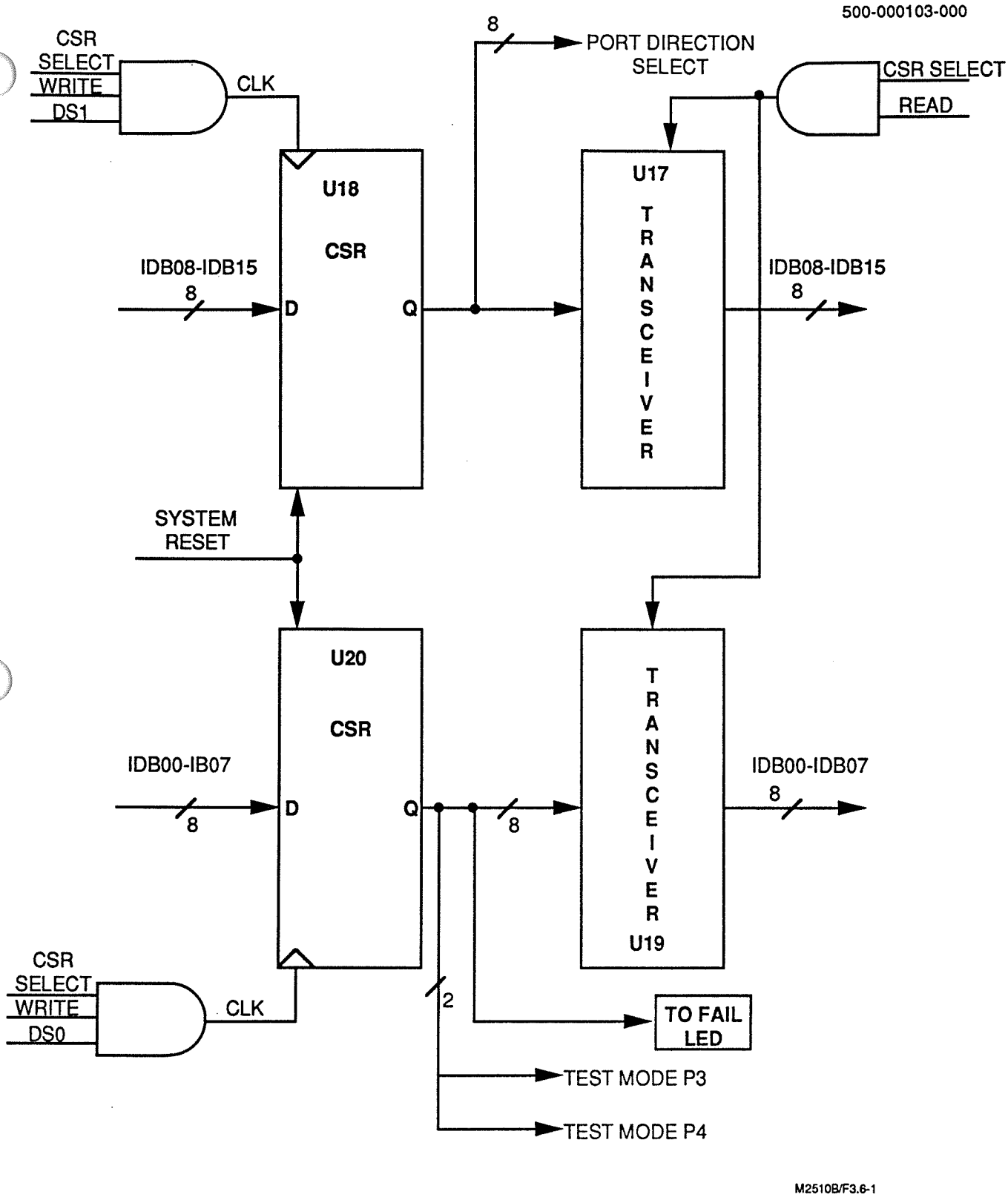


Figure 3.6-1. CSR Control Logic Block Diagram

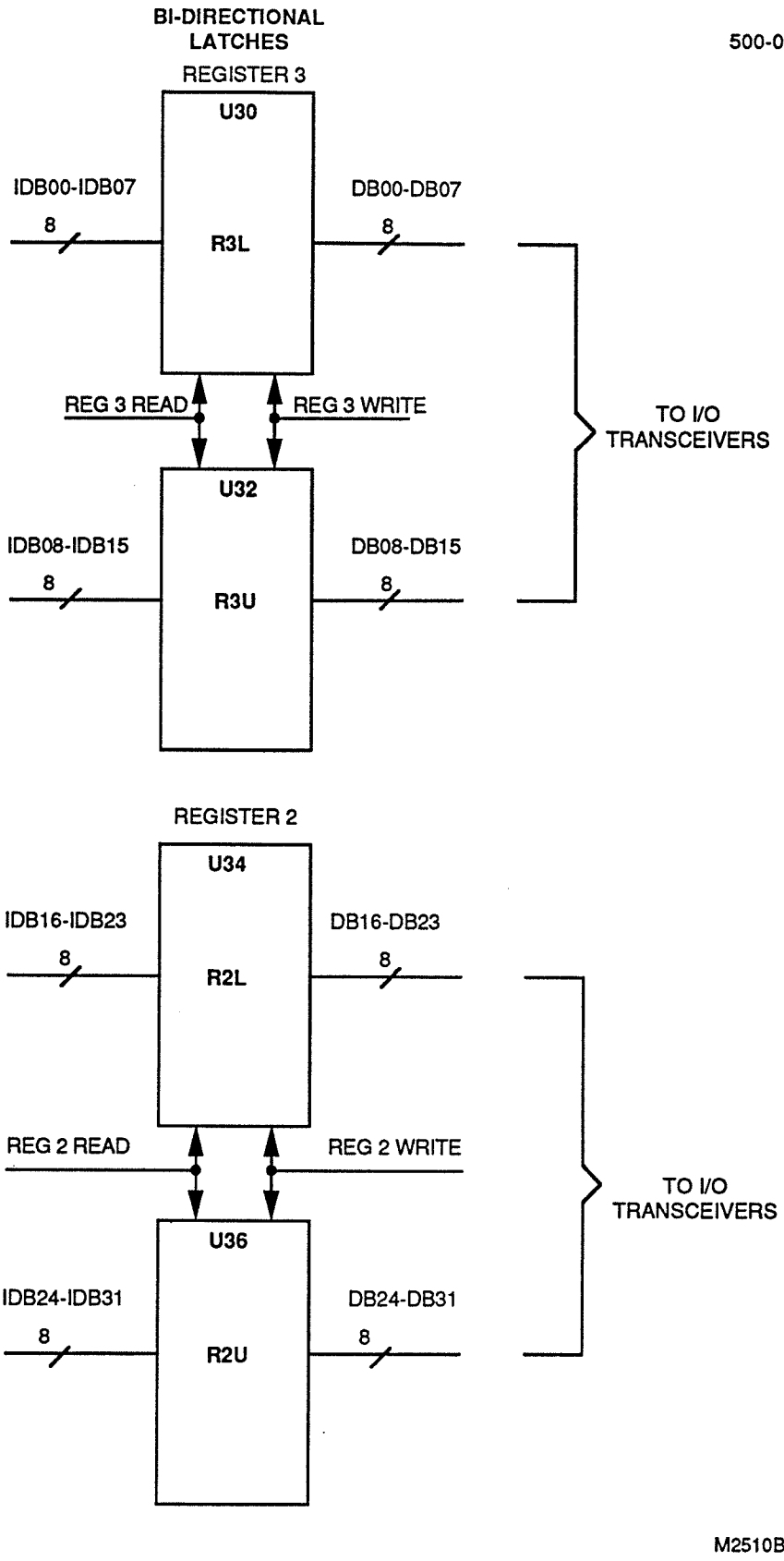


Figure 3.7-1. I/O Registers Bank A Block Diagram

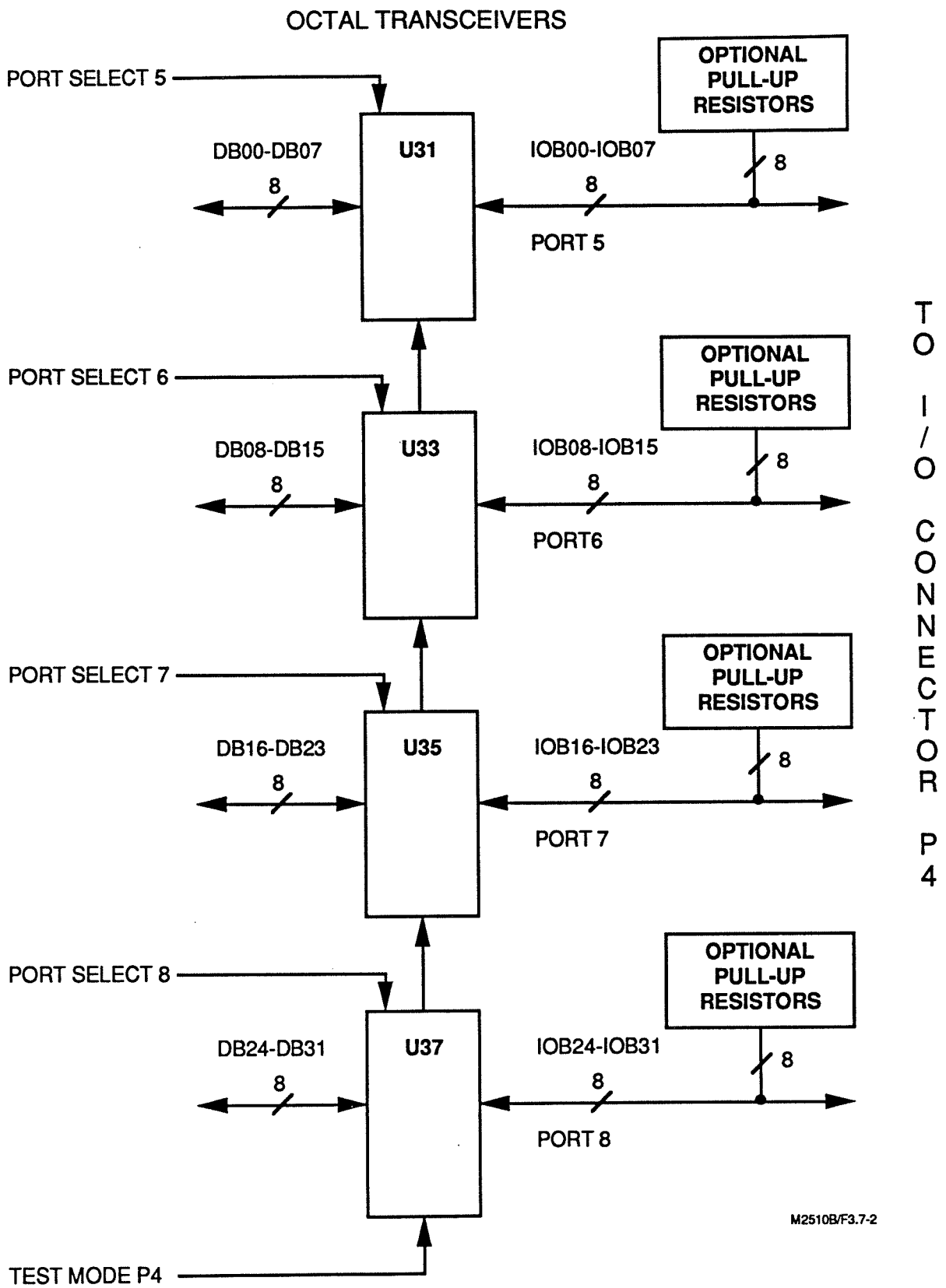


Figure 3.7-2. I/O Ports Bank A Block Diagram

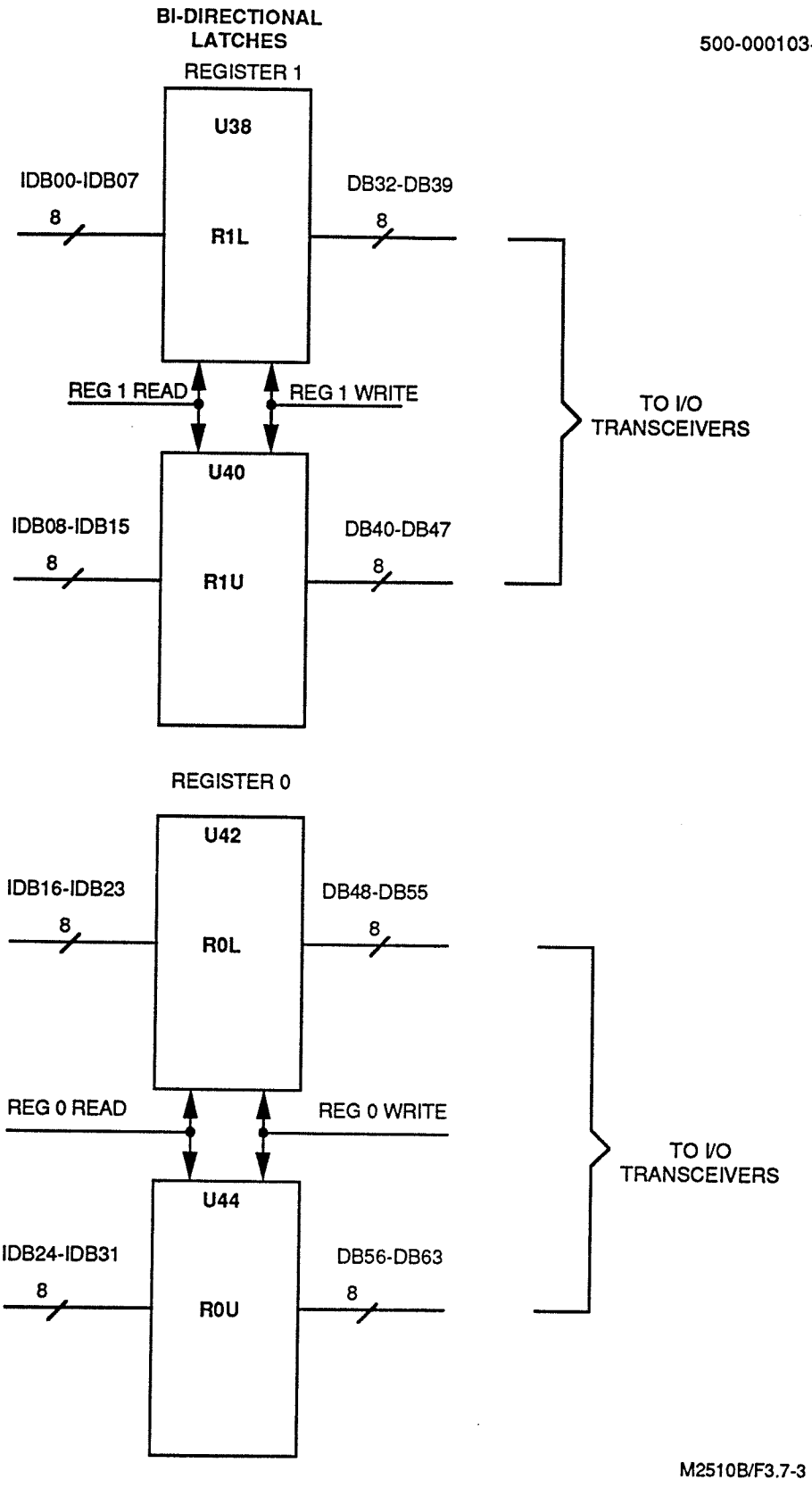


Figure 3.7-3. I/O Registers Bank B Block Diagram

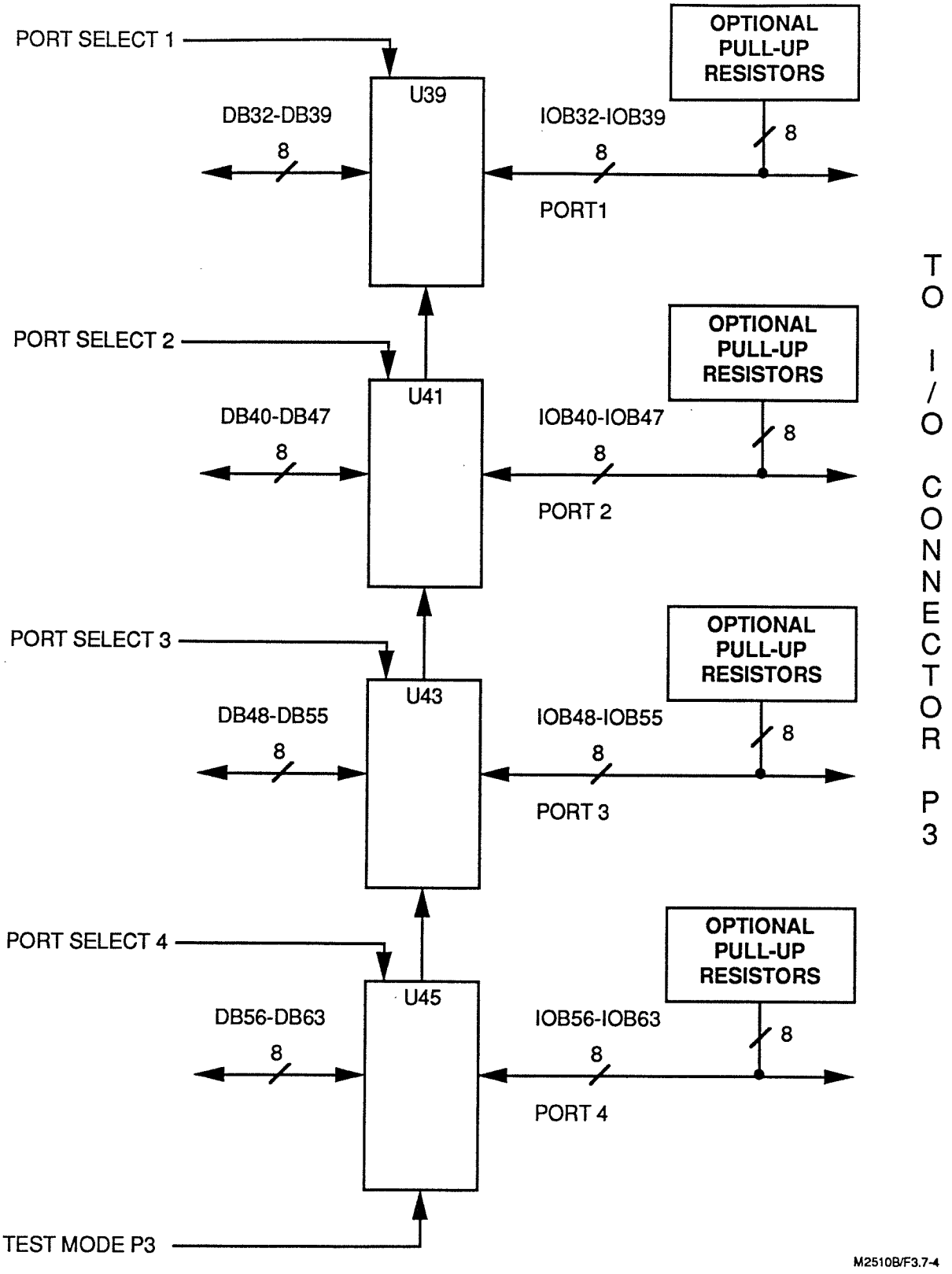


Figure 3.7-4. I/O Ports Bank B Block Diagram

SECTION 4

PROGRAMMING

4.1 REGISTER MAP

The VMIVME-2510B contains eight 8-bit I/O Data Registers and a 16-bit CSR. The I/O Data Registers allow access of 64 I/O channels and are addressable as two 32-bit long words, four 16-bit words, or as eight 8-bit bytes (see Table 4.1-1). The CSR is addressable as a 16-bit word or as two 8-bit bytes (see Table 4.1-2).

The register numbering is based on the hexadecimal address of each register; whereas, the input/output channel numbers are based on the CPU bit numbering and location of the least significant byte in a long word. For example, if a long word is written to address XXX4, the least significant byte will be placed in data register DR7, with bit 0 of DR7 being the least significant bit of the long word. Figure 4.1-1 shows a basic VMIVME-2510B programming flow chart.

4.2 DETAILED PROGRAMMING

4.2.1 Built-in-Test

The Built-in-Test feature of this board lends itself to two basic modes of testing, off-line and on-line. The first, off-line, is characterized by the I/O ports being disabled from the field electronics such that on-board testing will not affect any external equipment. This off-line mode of test is initiated by setting CSRU to all ones and setting both Test Mode bits in CSRL to zero. The VMIVME-2510B has a separate test mode bit for each I/O connector. Setting a test mode bit to "0" allows for Data Register loopback testing whereby the programmer can write to a Data Register and read back the data for comparison. While a Test Mode (TM) bit is active, for an I/O connector, all testing will be transparent to the user equipment associated with that connector. A Test Programming Flowchart is shown in Figure 4.2-2.

Table 4.1-1. Data Register Address Map

RELATIVE ADDRESS*	MNEMONIC	NAME/FUNCTION	PORT
$XXX0	DR0	Data Register 0	4
$XXX1	DR1	Data Register 1	3
$XXX2	DR2	Data Register 2	2
$XXX3	DR3	Data Register 3	1
$XXX4	DR4	Data Register 4	8
$XXX5	DR5	Data Register 5	7
$XXX6	DR6	Data Register 6	6
$XXX7	DR7	Data Register 7	5

M2510B/T4.1-1

* XXX of the address is determined by Data Register address select switches S3 and S1. See Figure 5.5-1

Table 4.1-2. CSR5 Address Map

RELATIVE ADDRESS*	MNEMONIC	NAME/FUNCTION
$YYY0	CSRU	CSR Upper Byte
$YYY1	CSRL	CSR Lower Byte

M2510B/T4.1-2

* YYY of the CSR address is determined by CSR address select switches S4 and S2. See Figure 5.5-2

Table 4.1-3. I/O Data Register Bit Definition

I/O DATA REGISTER BIT MAPS

$XXX0 DR0, PORT 4

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
I/O DATA REGISTERS							
I/O63	I/O62	I/O61	I/O60	I/O59	I/O58	I/O57	I/O56

$XXX1 DR1, PORT 3

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
I/O DATA REGISTERS							
I/O55	I/O54	I/O53	I/O52	I/O51	I/O50	I/O49	I/O48

$XXX2 DR2, PORT 2

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
I/O DATA REGISTERS							
I/O47	I/O46	I/O45	I/O44	I/O43	I/O42	I/O41	I/O40

$XXX3 DR3, PORT 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I/O DATA REGISTERS							
I/O39	I/O38	I/O37	I/O36	I/O35	I/O34	I/O33	I/O32

2510B/T4.1-3/1

Table 4.1-3. I/O Data Register Bit Definition (Concluded)

I/O DATA REGISTER BIT MAPS

$XXX4 DR4, PORT 8

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
I/O DATA REGISTERS							
I/O31	I/O30	I/O29	I/O28	I/O27	I/O26	I/O25	I/O24

$XXX5 DR5, PORT 7

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
I/O DATA REGISTERS							
I/O23	I/O22	I/O21	I/O20	I/O19	I/O18	I/O17	I/O16

$XXX6 DR6, PORT 6

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
I/O DATA REGISTERS							
I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8

$XXX7 DR7, PORT 5

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I/O DATA REGISTERS							
I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

M2510B/T4.1-3/2

Table 4.1-4. CSR Bit Definitions (All Bits of the CSR are Read/Write)

$YYY0 CSRU (PORT DIRECTION CONTROL FOR REGISTER DR0 THROUGH DR7)*

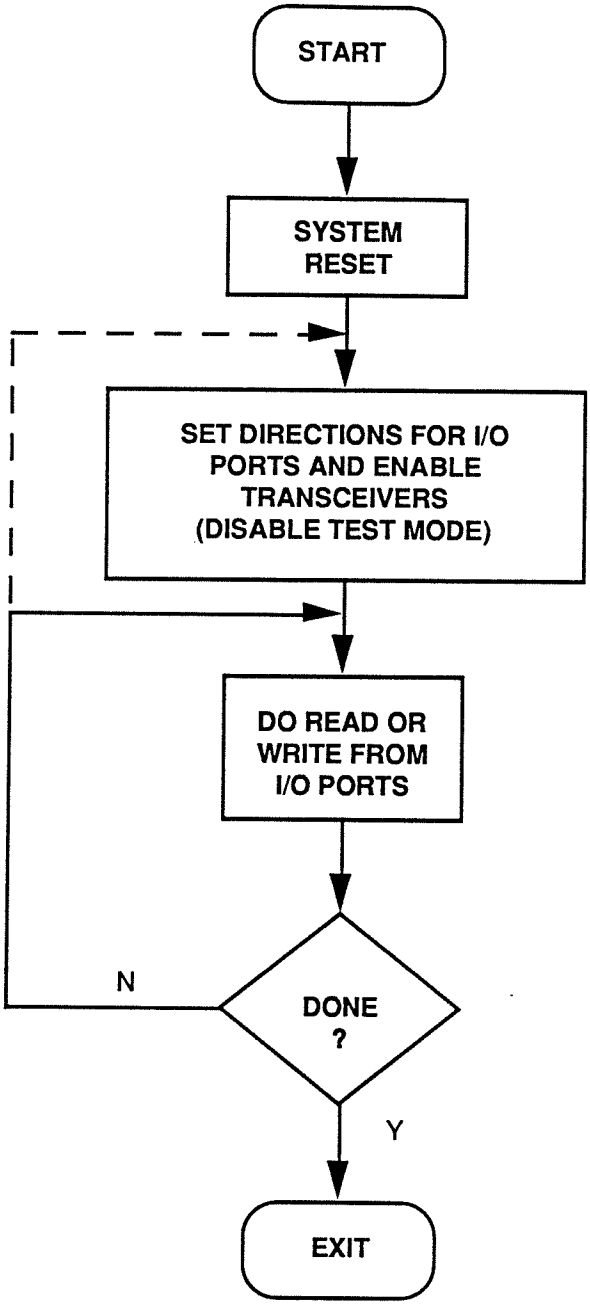
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
I/O DATA REGISTERS							
Port 1 (DR3)	Port 2 (DR2)	Port 3 (DR1)	Port 4 (DR0)	Port 5 (DR7)	Port 6 (DR6)	Port 7 (DR5)	Port 8 (DR4)

$YYY1 CSRL (TEST MODE AND FAIL LED CONTROL)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
I/O DATA REGISTERS							
TEST MODE P3 0 = Test Mode 1 = Normal	FAIL LED 1 = Off 0 = On	TEST MODE P4 0 = Test Mode 1 = Normal					
			[← USER-DEFINED STORAGE →]				

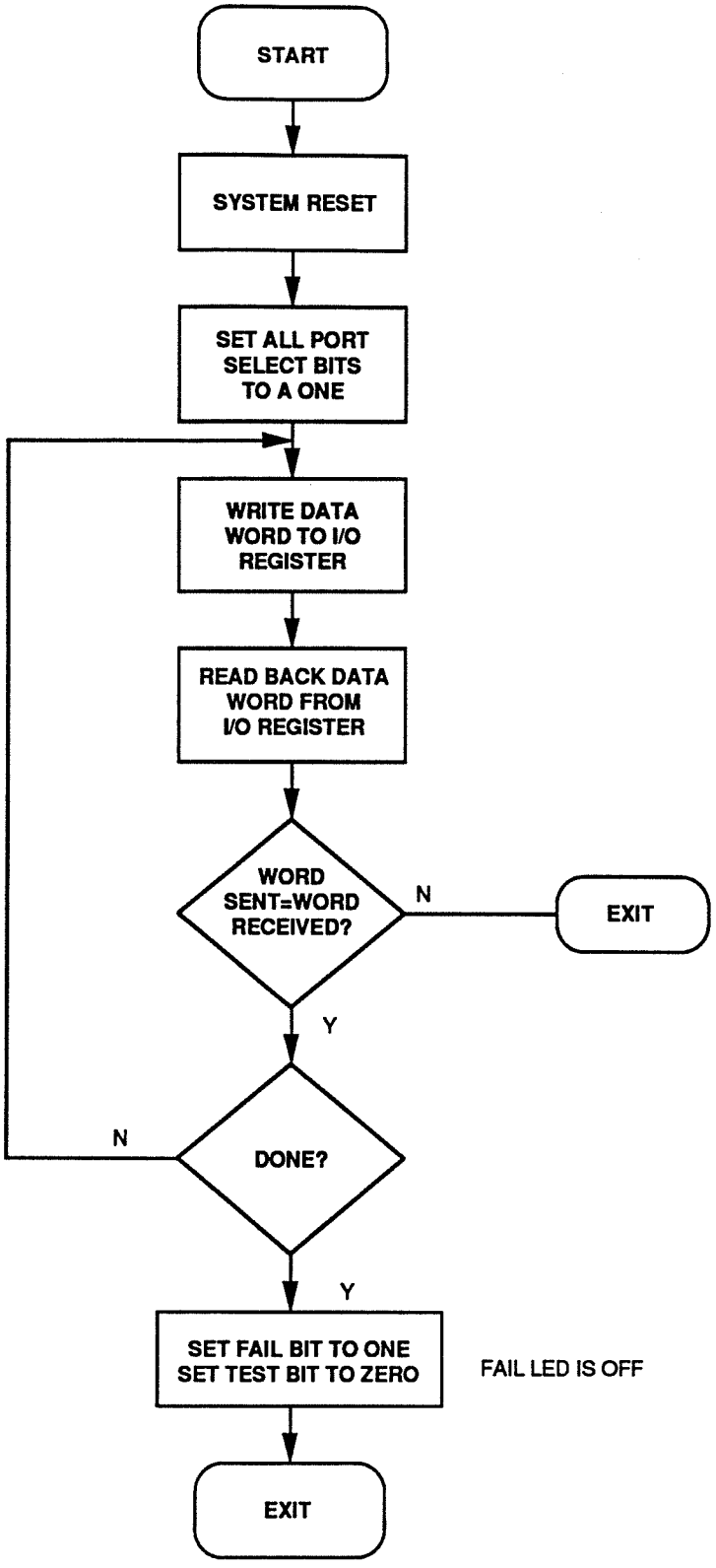
* IF THE PORT DIRECTION BIT = 1, THEN THE PORT IS AN OUTPUT PORT.
IF THE PORT DIRECTION BIT = 0, THEN THE PORT IS AN INPUT PORT.

M2510B/T4.1-4



NOTE: At System Reset, I/O Transceivers are "TRI-STATED" and the Fail LED is Illuminated

Figure 4.1-1. Programming Flowchart (Built-in-Test Not Active)



NOTE: At System Reset, I/O Transceivers are "TRI-STATED" and the Fail LED is Illuminated

Figure 4.2.1-1. Programming Flowchart (Built-in-Test Active)

A second mode of test can be performed while the VMIVME-2510B is on-line, (TM=1). All ports that are output ports can be tested by performing a read from the corresponding Data Register. This "loopback" mode of test can be useful when the programmer requires an on-line "health test" of the board. Data loopback can only be performed on a register initialized as an output (i.e., the corresponding port direction bit is a one).

4.2.2 Power-Up/System Reset

Upon power-up or when a system reset is performed, all bits will be cleared to zero in the CSR. Thus the VMIVME-2510B is in the test mode with the front panel LED illuminated and the output drivers are Tri-stated.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES AS SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the card is properly aligned and oriented in the supporting card guides, slide the card smoothly forward against the mating connector until firmly seated.

5.3 JUMPER AND SWITCH LOCATIONS

The physical positions of the jumpers and switches described in this section are shown in Figure 5.3-1.

5.4 ADDRESS MODIFIERS

The VMIVME-2510B is configured at the factory to respond to short supervisory I/O access. This configuration can be changed to short non-privileged by installing jumper J1.

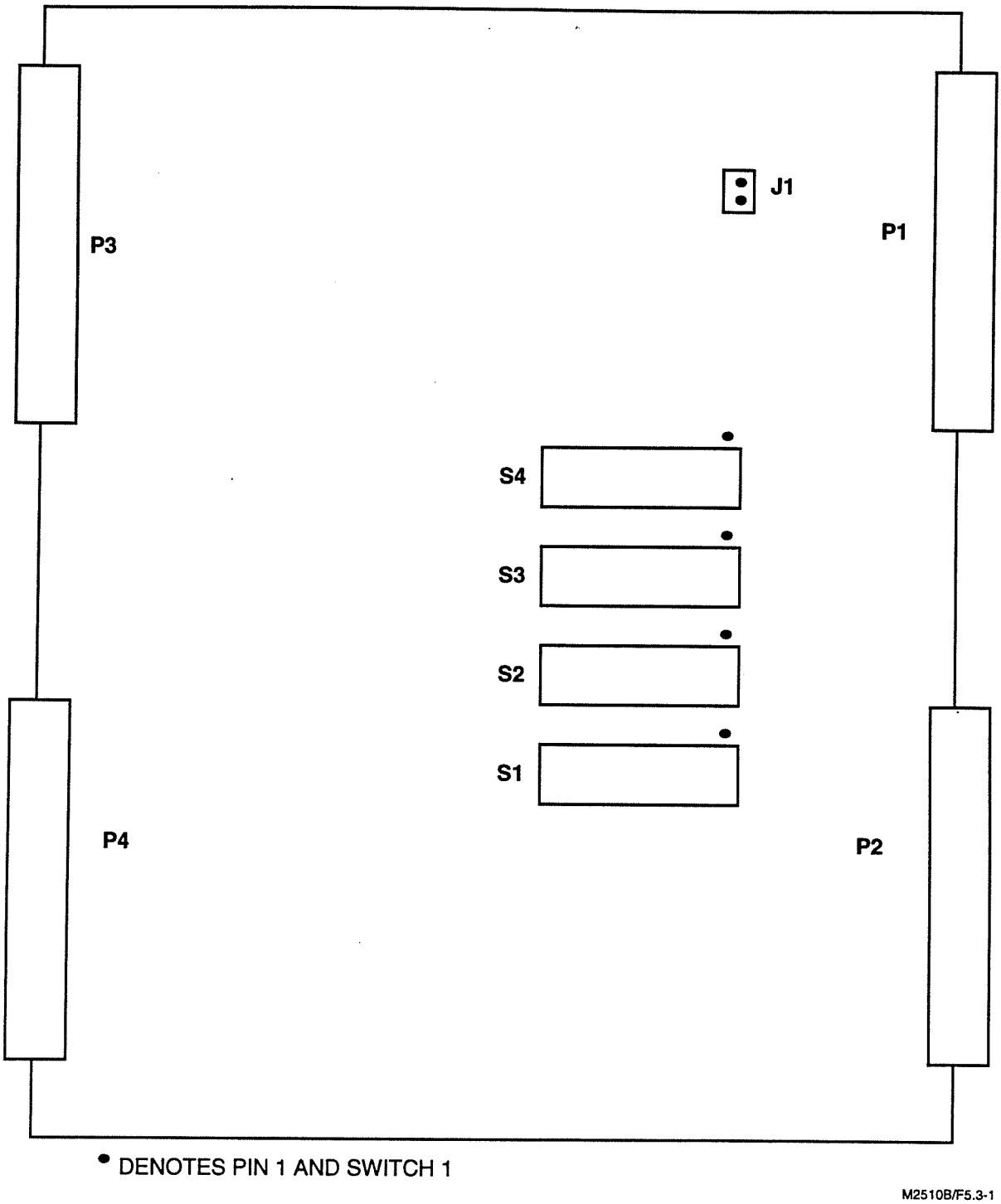


Figure 5.3-1. Switch and Jumper Locations

5.5 ADDRESS SELECTION SWITCHES

Two sets of board select switches are provided, as described in Section 3.1.2. The switches shown in Figure 5.5-1 select the base address of the Data Registers, and the switches shown in Figure 5.5-2 select the CSR base address. The figures also show the switches used in the addressing scheme.

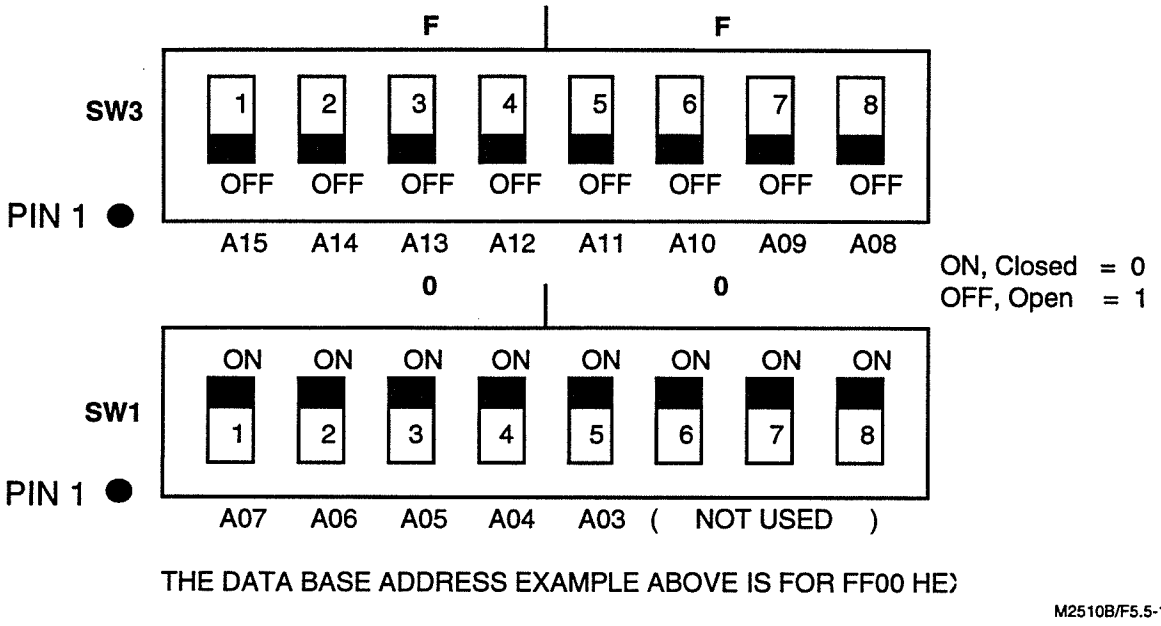


Figure 5.5-1. Data Register Base Address Select Switches, SW3 and SW1

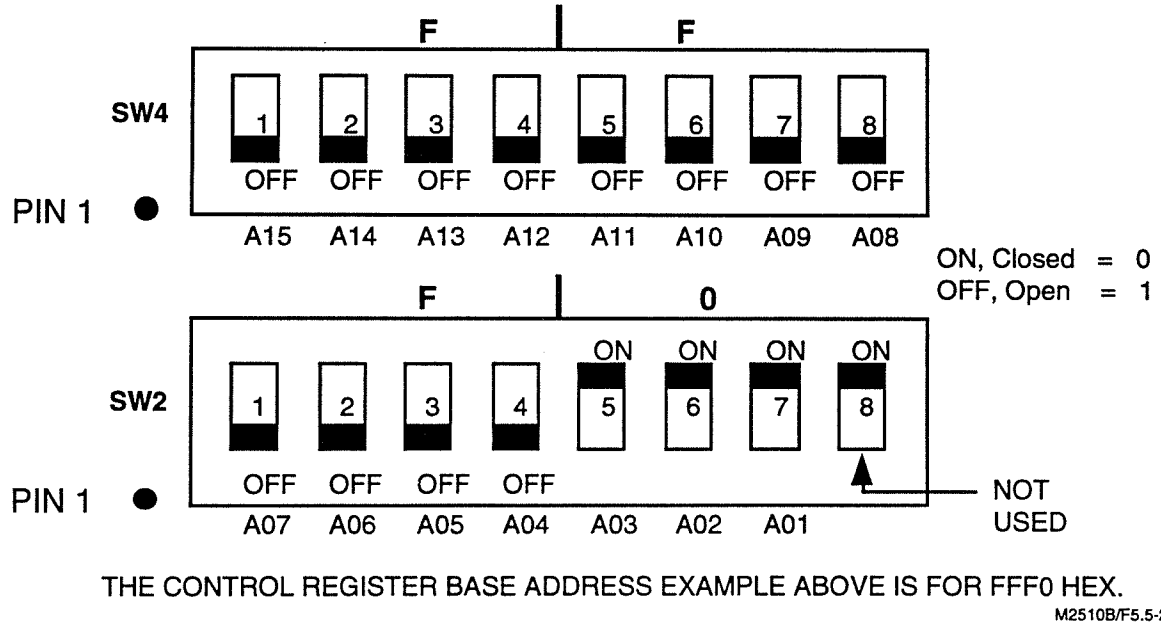
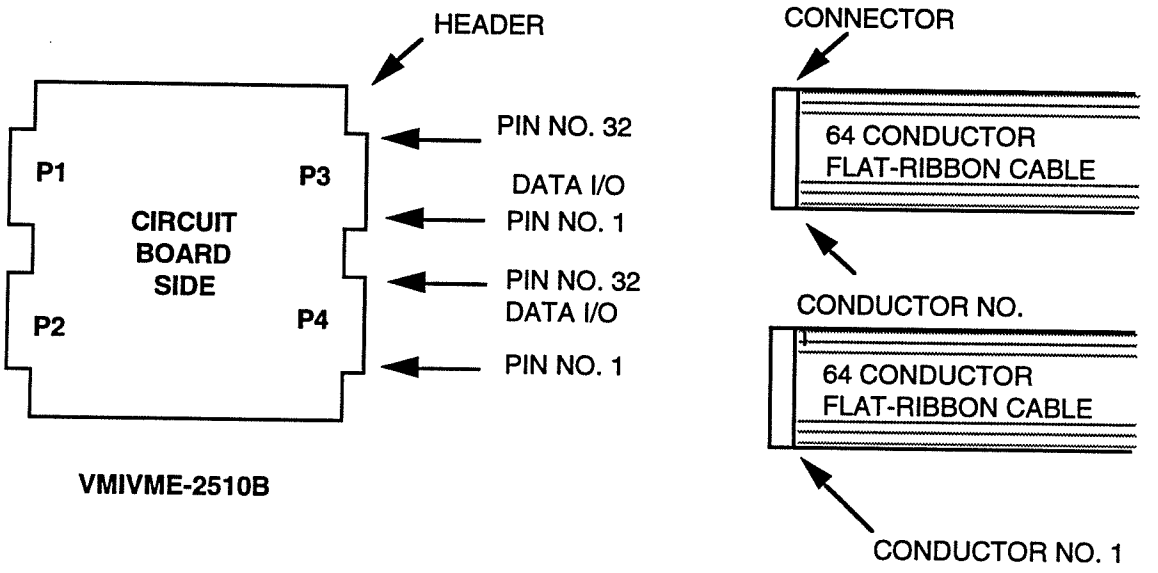


Figure 5.5-2. CSR Base Address Select Switches, SW4 and SW2

5.6 I/O CABLE AND CARD-EDGE CONNECTOR CONFIGURATION

The I/O connectors (P3 and P4) on the VMIVME-2510B are 64-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Applications Guide (VMIC Publication 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning I/O connections are shown in Figure 5.6-1. This figure has conductor no. 1 shown at the bottom of the connector as it plugs into the header, due to pin no. 1 of P3 and P4 being mounted as shown. Tables 5.6-1 and 5.6-2 depict the P3 and P4 connector pin assignments for the 64 I/O channels of the VMIVME-2510B. A compatible flat-ribbon cable connector for the VMIVME-2510B is Panduit No. 120-964-435E and strain relief, Panduit No.100-000-032.



M2510B/F5.6-1

Figure 5.6-1. Cable Connector Configuration

Table 5.6-1. P3 Pin and Channel Assignment

P3*

ROW A PIN	CHANNEL NO.
32	63
31	62
30	61
29	60
28	59
27	58
26	57
25	56
24	55
23	54
22	53
21	52
20	51
19	50
18	49
17	48

P3*

ROW A PIN	CHANNEL NO.
16	47
15	46
14	45
13	44
12	43
11	42
10	41
09	40
08	39
07	38
06	37
05	36
04	35
03	34
02	33
01	32

M2510/T5.6-1

*All P3 Row C pins are connected to ground.

Table 5.6-2. P4 Pin and Channel Assignment

P4*

ROW A PIN	CHANNEL NO.
32	31
31	30
30	29
29	28
28	27
27	26
26	25
25	24
24	23
23	22
22	21
21	20
20	19
19	18
18	17
17	16

P4*

ROW A PIN	CHANNEL NO.
16	15
15	14
14	13
13	12
12	11
11	10
10	09
09	08
08	07
07	06
06	05
05	04
04	03
03	02
02	01
01	00

M2510B/T5.6-2

*All P4 Row C pins are connected to ground.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

SIZE	DWG NO	SH	REV
A	132-000103-000	1	M

NOTES:

1. FOR SCHEMATIC DIAGRAM SEE 141-000103-000.
2. FOR TEST PROCEDURE SEE 510-000103-000.
3. FOR DOCUMENT SET SEE 110-000103-000.

REVISION STATUS OF 332
A
B
B
B
B
B
C
C
C
C
C
C

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 89-0003 RELEASE DOCUMENT	3/28/89	M.S.
B	ECO 89-0004 ADD SHEET 8	3/28/89	M.S.
C	ECO 89-0104	8/10/89	M.S.
D	ECO 89-0194	4/10/90	M.S.
E	ECO 90-0180	12/5/90	M.S.
F	ECO 91-0215	8/8/91	K.P.
G	CHANGE TO "ABC" PER ECO 92-0099	6/25/92	A.J.
H	CHANGE QTY OF ITEM 28 PER ECO 92-0177	6/25/92	A.J.
J	CHANGE PER ECO 93-0758	4/4/94	D.F.
K	CORRECTED LOGO P/N PER ECO 94-0681	9/26/94	A.J.
L	CHANGE PER ECO 98-0256	5/15/98	A.J.
M	CHANGE LED P/N PER ECO 99-0010	1/27/99	

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON: 2 PL. DECIMALS ± 3 PL. DECIMALS ± ANGLES ± FRACTIONS ±	DRAWN: S. WURTZ	4/27/88
	PROJ.ENG.: M. SPANGLER	3/28/89
	ENG.MGR.: P. RAINOSEK	3/29/89
	PROD.: D. FOWLER	4/3/89
	Q.A.: S. KEAGLE	4/4/89
MAGNETIC MEDIA FILENAME FOR PACKAGE: A000103M.EXE		

VMIC® HUNTSVILLE, ALABAMA 35803-3308
VME MICROSYSTEMS INTERNATIONAL CORPORATION

ASSEMBLY DRAWING
VMIVME-2510B

SIZE	FSCM NO.	DWG NO.
A	OBPH5	132-000103-000

SCALE		SHEET
NONE		1 OF 7

REWORK LEGEND:

A. REWORK INSTRUCTIONS SHALL BE ACCOMPLISHED ON THE COPPER REVISION(S) INDICATED AND WILL BECOME A PART OF THE ASSEMBLED BOARD.

B. REWORK INSTRUCTION SYMBOLS:

1. PIN ONE DOT ■
2. DRILL HOLE ●
3. DISCONNECT TRACE ×
4. TRACE ON INTERNAL LAYER ------
5. TRACE ON EXTERNAL LAYER ———

INSTRUCTIONS:

NOTES:

1> A. ALL ASSEMBLED BOARDS SHALL BE IDENTIFIED WITH THE ASSEMBLED BOARD PART NUMBER. THIS NUMBER INCLUDES THE CURRENT REVISION LETTER LISTED IN THE "REVISION STATUS OF 332" BLOCK (SEE SHEET 1). THE RESULTING PART SHALL BECOME A 332-000103-ABC (REV).

B. THE PART NUMBER FIELDS "ABC" WILL COINCIDE WITH THE OPTIONAL PARTS INSTALLED IN THE COMPLETED ASSEMBLY. IF NO OPTIONAL PARTS ARE USED IN A FIELD, THAT FIELD WILL DEFAULT TO "0".

C. IF NECESSARY, REMOVE AND REPLACE 332 REVISION LETTER WITH CURRENT REVISION LETTER USING EITHER A REMOVABLE NON-SMEARING BLACK INK OR A LABEL.

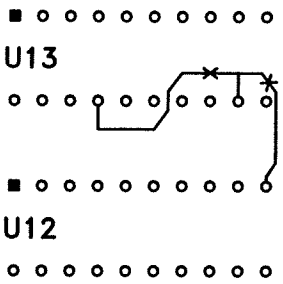
2> SOLDER COMPOSITION COMPLIES WITH MIL-STD-2000.

3> SEE DRAWING 150-000022-000 FOR THE ASSEMBLY AND INSTALLATION OF THE FRONT PANEL.

EFFECTIVITY: DCO IV 2510B (133-000103-000 REV N/R)

INSTRUCTIONS: REWORK

STEP 1 (COMPONENT SIDE)
DISCONNECT U13 PIN 18 FROM U13 PIN 5.
STEP 2 (SOLDER SIDE)
DISCONNECT U13 PIN 18 FROM U13 PIN 17.
STEP 3 (SOLDER SIDE)
DISCONNECT U13 PIN 12 FROM U13 PIN 17.
STEP 4 (SOLDER SIDE)
DISCONNECT U13 PIN 12 FROM U12 PIN 10.
STEP 5 (COMPONENT SIDE)
DISCONNECT U23 PIN 5 FROM U25 PIN 4.
STEP 6 (COMPONENT SIDE)
DISCONNECT TRACE FROM U5 PIN 10 TO U3 PIN 1.
STEP 7 (SOLDER SIDE)
DISCONNECT U27 PIN 6 FROM U28 PIN 13.
STEP 8 (SOLDER SIDE)
CONNECT U25 PIN 4 TO U3 PIN 1.
STEP 9 (SOLDER SIDE)
CONNECT U28 PIN 13 TO U27 PIN 11.
STEP 10 (SOLDER SIDE)
CONNECT U13 PIN 17 TO U14 PIN 17.
STEP 11 (SOLDER SIDE)
CONNECT U13 PIN 18 TO U14 PIN 2.
STEP 12 (SOLDER SIDE)
CONNECT U13 PIN 3 TO U27 PIN 6.
STEP 13 (SOLDER SIDE)
CONNECT U13 PIN 5 TO U27 PIN 1.
STEP 14 (SOLDER SIDE)
CONNECT U13 PIN 12 TO U23 PIN 5.
STEP 15 (SOLDER SIDE)
CONNECT U13 PIN 16 TO U25 PIN 4.



STEP 4

END OF REWORK INSTRUCTIONS

PARTS LIST

VME Microsystems In'tl Corporation

CODE OBPH5 | DRAWING NUMBER 132-000103-000 | REV: M | CHECKER/DATE C. Muggeg 1-19-99

ITEM	ABC	REF. DES.	QTY.	PART NO.	DESCRIPTION	MANUFACTURER	
1			1	333-000103-000	BOARD: PC, RAW, 4 LAYERS (2510B)		
2			1	317-000102-000	F/P ASSY: EXTRUDED EJECTOR, TWO 64 PIN CUTOUTS PANEL MOUNT FAIL LED (SEE NOTE 3)		
3				DELETED			
4			1	324-000103-100	LABEL: ID, 2510B, FRONT PANEL (SEE NOTE 3)		
5				DELETED			
6				DELETED			
7				DELETED			
8				DELETED			
9		U24,26	2	331-300400-600	IC: DIGITAL, QUAD 2-INPUT NAND GATE, PLASTIC DIP	SN74LS00N	(TI)
10		U25	1	331-300404-600	IC: DIGITAL, HEX INVERTER, PLASTIC DIP	SN74LS04N	(TI)
11		U5	1	331-300427-600	IC: DIGITAL, TRIPLE 3-INPUT NOR GATE, PLASTIC DIP	SN74LS27N	(TI)
12		U23	1	331-300432-600	IC: DIGITAL, QUAD 2-INPUT OR GATE, PLASTIC DIP	SN74LS32N	(TI)
13		U28	1	331-300438-700	IC: DIGITAL, QUAD 2-INPUT NAND BUFFER, PLASTIC DIP	SN74S38N	(TI)

ITEM	ABC	REF. DES.	QTY.	PART NO.	DESCRIPTION	MANUFACTURER
14		U6	1	331-304155-600	IC: DIGITAL, DUAL 1 OF 4 DECODER, PLASTIC DIP	SN74LS155N (TI)
15		U21,22	2	331-304157-600	IC: DIGITAL, QUAD 2-INPUT MULTIPLEXER, PLASTIC DIP	SN74LS157N (TI)
16		U27	1	331-304164-600	IC: DIGITAL, 8 BIT SHIFT REGISTER, PLASTIC DIP	SN74LS164N (TI)
17		U14,29	2	331-304240-600	IC: DIGITAL, OCTAL BUS DRIVER, PLASTIC DIP	SN74LS240N (TI)
18		U11,12,17,19	4	331-304244-600	IC: DIGITAL, OCTAL BUS DRIVER, NON-INVERTING, PLASTIC DIP	SN74LS244N (TI)
19		U18,20	2	331-304273-600	IC: DIGITAL, OCTAL D FLIP FLOP, PLASTIC DIP	SN74LS273N (TI)
20		U7-10	4	331-304520-100	IC: DIGITAL, 8 BIT IDENTITY COMPARATOR, PLASTIC DIP	SN74ALS520N (TI)
21		U1-4,15,16	6	331-304645-110	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74(ALS,AS)645A-1N (TI)
22		S1-4	4	351-000000-080	SWITCH: DIP, 8 POSITION, LOW PROFILE, PC MOUNT, TAPE SEAL	ADF-08PCT (AUGAT)
23		U30,32,34,36,38,40, U42,44	8	331-309024-100	IC: MICROPROCESSOR, OCTAL BIDIRECTIONAL BUS LATCH, PLASTIC DIP	AM2952ADC (AMD)
24		P3,4	2	321-000013-105	CONNECTOR: FLAT CABLE, 64 PIN, .114 ANGLED WITH EJECTOR LATCHES, TYPE C, MALE	120-964-033A (PANDUIT)
25		C1-9,11-38	37	315-205000-104	CAP: .1uF, .100 LEAD SPACE, 20%, 50V, Z5U, CERAMIC MONOLYTHIC	C3(15,20)C104M5U5CA (KEMET)
26		D1	1	337-000001-210	DIODE: LED, RED, 5V, 15mA, INTEGRAL RESISTOR & 6" LEADS	558-0102-003 (DIALIGHT)
27		U46	1	331-300402-600	IC: DIGITAL, QUAD 2-INPUT NOR GATE, PLASTIC DIP	SN74LS02N (TI)

ITEM	ABC	REF. DES.	QTY.	PART NO.	DESCRIPTION	MANUFACTURER	
28		J1	1	321-000016-021	TERMINAL: PC BOARD, SINGLE ROW, .025 THICK, GOLD PLATED, TWO POSTS	92983401-02	(PANDUIT)
29		U13	1	321-001320-001	SOCKET: DIP, 20 PIN, .300 ROW, STAMPED & FORMED	2-641602-(3,1,5)	(AMP)
30		U13	1	303-000033-000	PROGRAMMED PAL: PAL A, FILE: 2510B13A.PLD, A PROGRAMMED 16L8A (331-300100-100)		
31		HARDWARE	8	328-250000-010	SCREW: PAN HEAD, PHILLIPS, M2.5 X 10MM, SS		
32		HARDWARE	8	328-250001-025	NUT: METRIC, 2.5MM, HEX, SS		
33		RP1-8	8	321-000007-002	SOCKET: IC, BREAKAWAY STRIP, 10 CONTACTS, TIN/GOLD	3852010-02	(MUPAC)
34		C10	1	315-902001-476	CAP: 47uF, 20%, 35V, RADIAL, ALUMINUM ELECTRO-LYTIC	ECEA1VU470	(PANASONIC)
35		R2,3	2	347-000000-102	RESISTOR: 1K OHM, 1/4W, 5%, CARBON FILM		
36		P1	1	321-000054-001	CONNECTOR: DIN, 96 PIN WITH EXTENDED GROUND PINS, TYPE C	536437-6	(AMP)
37		P2	1	321-000054-002	CONNECTOR: DIN, 96 PIN WITH EXTENDED GROUND PINS, TYPE C	536437-5	(AMP)
38		REF. P1-4	A/R	316-000002-000	LOCTITE: SMALL SCREW THREADLOCKER 222		
39							
40							
41							

ITEM	ABC	REF. DES.	QTY.	PART NO.	DESCRIPTION	MANUFACTURER	
42	1BC	U31,33,35,37,39,41, U43,45	8	331-304645-200	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74AS645N	(TI)
43	2BC	U31,33,35,37,39,41, U43,45	8	331-304640-200	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74AS640N	(TI)
44	3BC	U31,33,35,37,39,41, U43,45	8	331-304641-200	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74AS641N	(TI)
45	4BC	U31,33,35,37,39,41, U43,45	8	331-304642-200	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74AS642N	(TI)
46	A0C		N/A		(NO RESISTORS REQUIRED FOR THIS OPTION)		
47	A1C	RP1-8	8	347-001002-222	SIP: 2.2K OHM, BUSSED, 10 PIN, LOW PROFILE	4610X-101-222	(BOURNS)

NOTES:

PAL LOCATION CHART

U#	PAL #	SHEET #
U13	PAL A	1

REVISIONS

REV.	DESCRIPTION	BY	DATE	APPR.
A	E.C.O. 89-0003 RELEASE DOCUMENT	S.Stanley	4/24/89	M. SPANGLER
B	E.C.O. 88-0004 ADD LINE	S.Stanley	4/24/89	M. SPANGLER
C	E.C.O. 95-0587 REVISED	E.M. GREEN	11/28/95	afj

SIGNATURES		DATE
DRAWN	K.Ward	8/31/87
PROJ. ENG.	M. SPANGLER	4/24/89
ENG. MGR.	P.A.R.	4/25/89
PROD.	DENNIS FOWLER	4/26/89
Q.A.	SHARON KEAGLE	4/26/89

VMIC®
12090 SO. MEM. PKWY.
HUNTSVILLE, AL. 35803-3308
VME MICROSYSTEMS INTERNATIONAL CORPORATION

VMIVME-2510B SCHEMATIC

SIZE		DWG NO.	REV.
B	0BPH5	141-000103-000	C
SCALE			SHEET 1 OF 4

ASL 1A4
P1
PAL16L8A U13
B16 AM0 2
B17 AM1 4
B18 AM2 6
B19 AM3 8
A23 AM4 11
C14 AM5 13
A20 IACK* 15
1A6 DS0* 17
1D4 T26SNS 3
1D6 BSH 5
J1 7
9
2D8 2A6 WRITE EN L 12
14
1A4 WRITE L 16
1A6 DS1 * 18
GND 10 VCC 20 +5
O 19 2C7

SHTIOL
74LS520 U9
1D1 BA15 2 BA14 4 BA13 6 BA12 8 BA11 11 BA10 13 BA09 15 BA08 17
P0 P1 P2 P3 P4 P5 P6 P7 P=Q
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 19
GND 10 VCC 20 +5
S3 ADF-08

DEVISL
74LS520 U7
1D2 BA07 2 BA06 4 BA05 6 BA04 8 BA03 11
S1 ADF-08
1C2 2D8

1D8 BSH
74LS164 U27
A B CK CLR
QA QB QC QD QE QF QG QH
T26SNS 1D8
P1 A10 SYSCLK 8
+5 R2 1K
+5V

U46 74LS02
DSDELSTBH 1B4
DTACH 13 DSH 12 U28 74S38 11 DTACK* A16

DSH
WRITEH
GDS1L
74LS00 U26
74S38 U28
74ALS645-1 U15
P1 C8 C7 C6 C5 C4 C3 C2 C1 D15 D14 D13 D12 D11 D10 D09 D08
DIR G A B
11 IDB15 12 IDB14 13 IDB13 14 IDB12 15 IDB11 16 IDB10 17 IDB09 18 IDB08
1B1
20 10 +5V

GLWORDL 2D7
GDS0L
74ALS645-1 U16
P1 A8 A7 A6 A5 A4 A3 A2 A1 D07 D06 D05 D04 D03 D02 D01 D00
11 IDB07 12 IDB06 13 IDB05 14 IDB04 15 IDB03 16 IDB02 17 IDB01 18 IDB00
1B1
BSH
DTBSL 13 CSRBSL 12 U26 11 2C6

74LS244 U12
P1 A24 A25 A26 A27 A28 A29 A30 A07 A06 A05 A04 A03 A02 A01
18 BA07 3 BA06 16 BA05 5 BA04 14 BA03 7 BA02 12 BA01
1B8 2B8 1A6
20 10 +5V

74LS244 U11
P1 C23 C24 C25 C26 C27 C28 C29 C30 A15 A14 A13 A12 A11 A10 A09 A08
18 BA15 3 BA14 5 BA13 7 BA12 9 BA11 12 BA10 14 BA09 16 BA08
1C8 2C8
20 10 +5V

R3 1K +5
WDMUXL 1A7 DTBSL
74S38 U28 U23
GLWORDL A01L

74ALS645-1 U2
P2 B30 B29 B28 B27 B26 B25 B24 B23 D31 D30 D29 D28 D27 D26 D25 D24
11 IDB31 12 IDB30 13 IDB29 14 IDB28 15 IDB27 16 IDB26 17 IDB25 18 IDB24
3D8 3D4
20 10 +5V

74ALS645-1 U1
11 IDB15 12 IDB14 13 IDB13 14 IDB12 15 IDB11 16 IDB10 17 IDB09 18 IDB08
3B8 3B4 2B5 1C4
20 10 +5V

74ALS645-1 U4
P2 B21 B20 B19 B18 B17 B16 B15 B14 D23 D22 D21 D20 D19 D18 D17 D16
11 IDB23 12 IDB22 13 IDB21 14 IDB20 15 IDB19 16 IDB18 17 IDB17 18 IDB16
3C8 3C4
20 10 +5V

74ALS645-1 U3
11 IDB07 12 IDB06 13 IDB05 14 IDB04 15 IDB03 16 IDB02 17 IDB01 18 IDB00
1B4 2B5 3B8 3B4
20 10 +5V

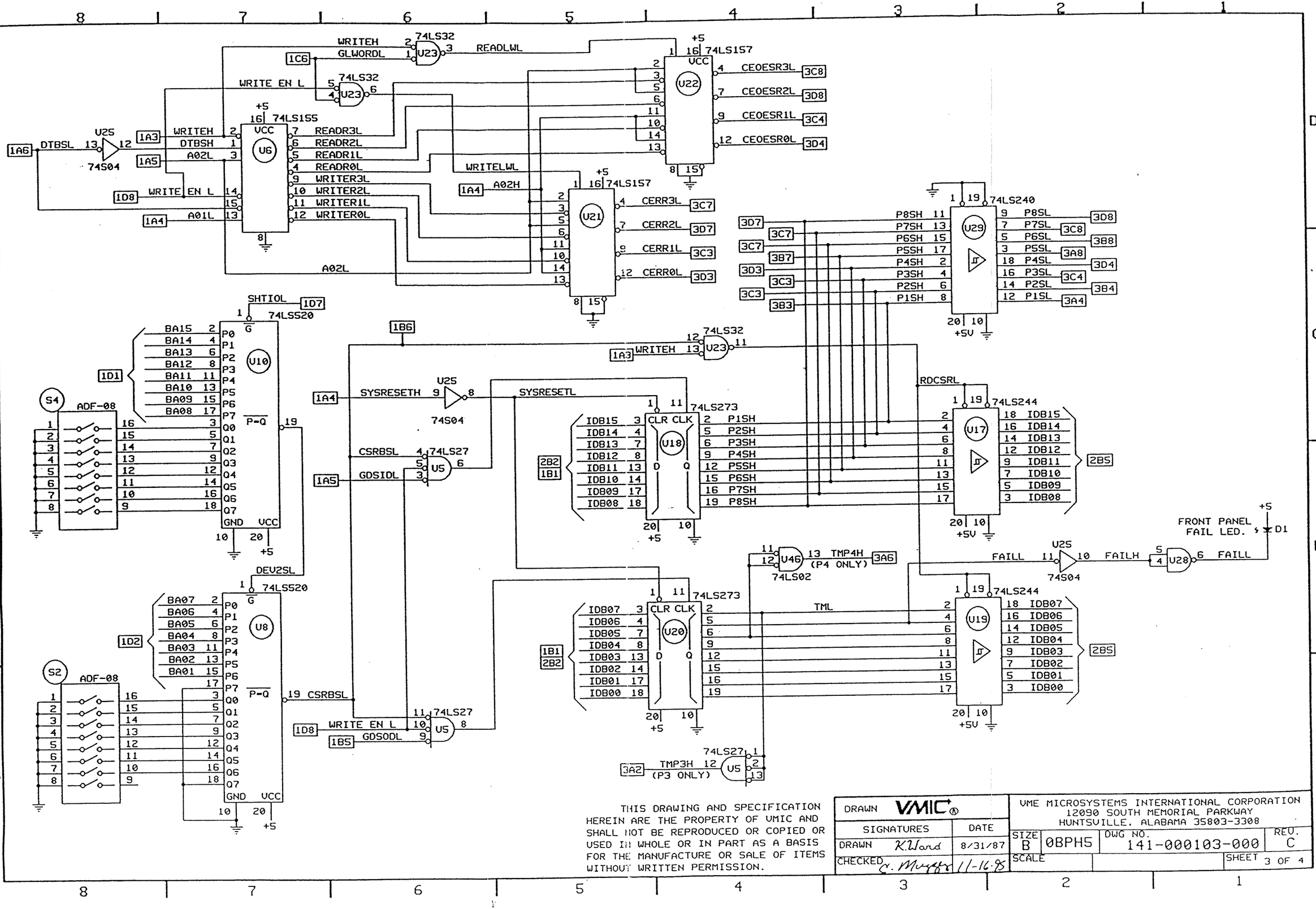
GDS0DH 11 3C4 3C8 U24 12 13
GDS0DL 3 2A7 U24 2 1
74LS00 U24
GDS1DH 8 3D4 3D8 U24 10 9
GDS1DL 6 2B7 U24 4 5
DSDELSTBH 1D3

74LS240 U14
1C8 1D8
P1 A13 A12 C13 A14 A18 C12 DS0* 17 DS1* 2 LWORD* 15 WRITE* 13 AS* 11 SYSRESET* 4 BA02 6 BA01 8
1C2
19 3 DS0H 18 DS1H 5 LWORDH 7 WRITEH 9 ASH 16 14 12
20 10 +5V 2D8

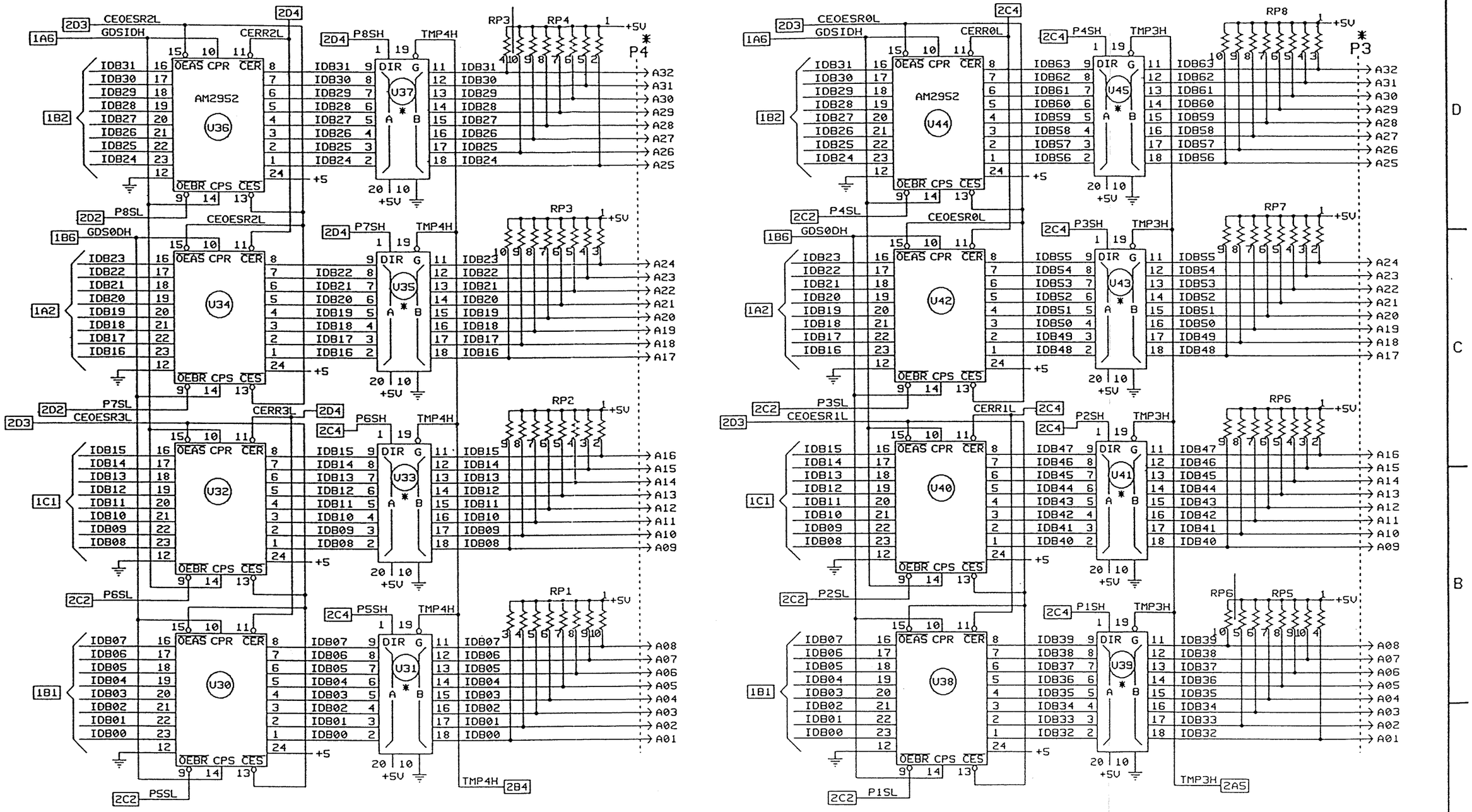
SYSRESETH 2C7 U25 3 4 74LS04
A02L U25 1 2 74LS04 2D6
A01L
ASL U25 5 6 74LS04 1D7 2D8

2D8 2C5
1C8
WRITEL

VMIC®		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE	DWG NO.	REV.
DRAWN K.Ward	8/31/87	B	0BPH5	141-000103-000 C
CHECKED C. Musser	11-16-87	SCALE		SHEET 2 OF 4



DRAWN VMIC®		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE B	DWG NO. 0BPH5 141-000103-000	REV. C
DRAWN K.Ward	8/31/87	SCALE		SHEET 3 OF 4
CHECKED C. Muggli	11-16-87			



*ALL PINS ON ROW C OF P3 AND P4 CONNECTOR ARE CONNECTED TO GROUND.

VMIC

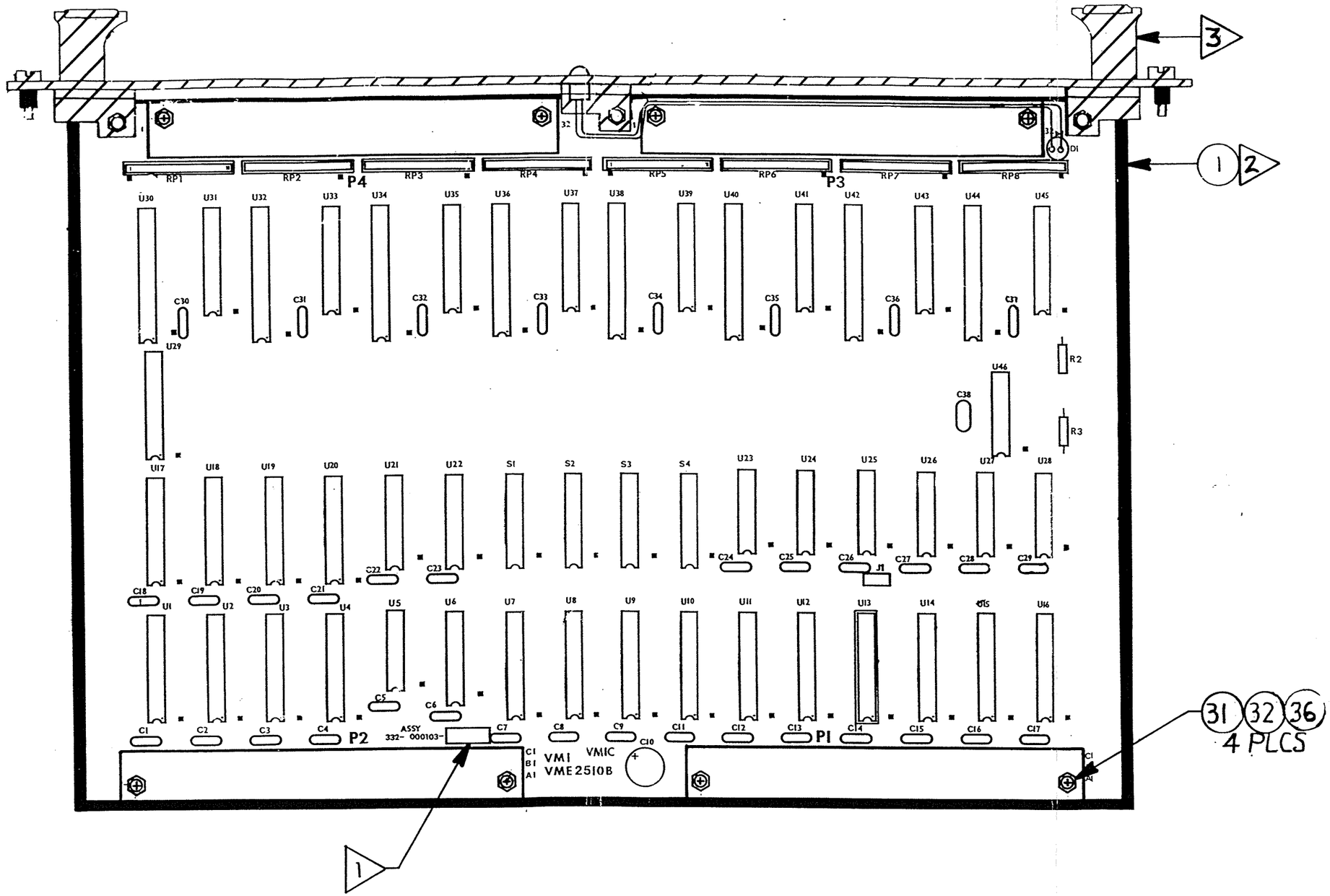
SIGNATURES	DATE
DRAWN K Ward	9/1/87
CHECKED C. Muggy	11-16-95

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5	141-000103-000	C

SCALE

SHEET 4 OF 4



THIS DRAWING AND SPECIFICATION HEREIN ARE THE PROPERTY OF VMIC AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS A BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

VMIC™	
SIGNATURES	DATE
DRAWN S.WURTZ	8/30/88
CHECKED C.Muzzey	1-20-89

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 132-000103-000	M
SCALE 1 TO 1		SHEET 2