APV25 FrontEnd Card and Interconnecting Backplane User Guide

Author: Paolo Musico
Paolo.Musico@ge.infn.it

Rev. 1.0
March 28, 2011

Revision History

Rev.	Date	Author	Description
1.0	28/3/11	Paolo Musico	First Draft

Contents

Introduction

The APV25 FrontEnd Card has been designed to connect an APV25 to 128 GEM readout channels (strips).
Up to 16 FrontEnd boards (2048 channels) are controlled and readout by a single VME64x module (also VME 32 compatible), the Multi Purpose Digitizer (MPD).

The front-end card houses:

- APV25 chip wire bonded on PCB
- Inputs coupling and protection network
- Linear power regulators for 1.25 V and 2.5 V
- Thermometer and unique ID code

A dedicated backplane has been developed to easily connect the front-end board to large GEM (40 x 50 cm) used in the JLAB SBS spectrometer.
The backplane houses up to 5 APV25 boards, distributing power supply and control signals and collecting analog output signals. It also sets the I^2C addresses for the APV25 boards and provides line terminations for high speed digital signals.
The backplane described herein is not a mandatory part of the system: it can be replaced by simpler flat cable connection or more sophisticated active parts.

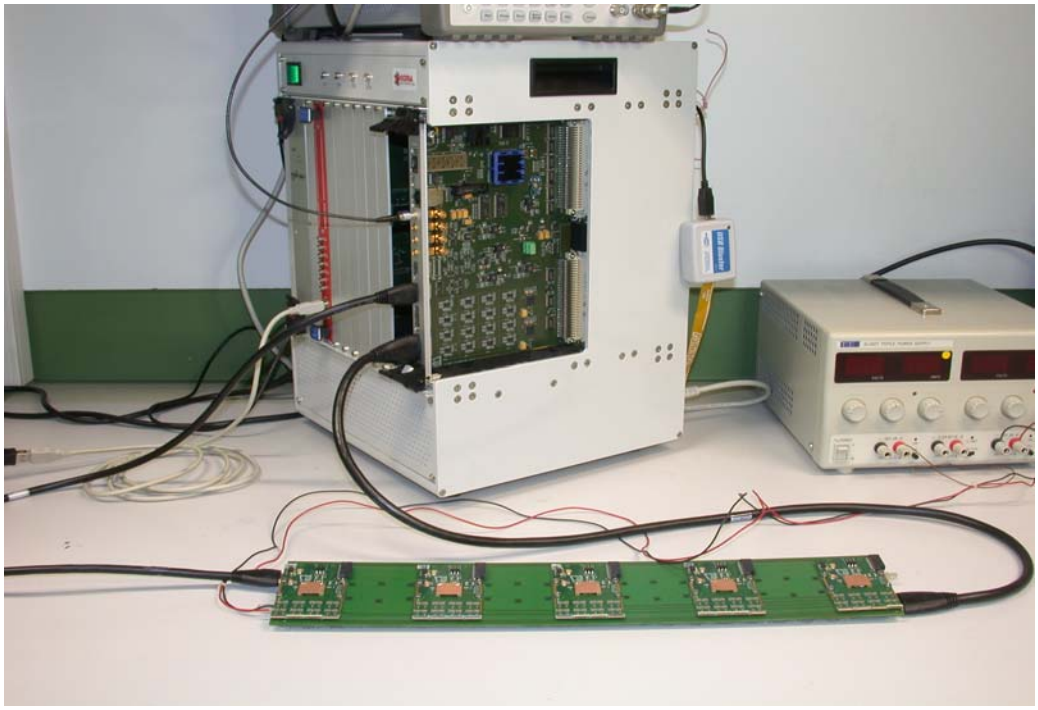

Fig. 1 System composed by 5 front-end boards connected to a backplane, handled by a MPD VME module.

APV25 Front End Card

I/O connectors (see fig. 2 & 3)

GEM side connectors

- J1, J2, J3, J4: PANASONIC p/n AYF313315 high density (0.3 mm pitch) 33 pins FPC connector. Only 32 pins are used and connected to the readout strips. The 33th is left unconnected. The pitch of these connectors is 12.45 mm.

System side connectors

- J5: 26 pin high density flat cable connector for digital controls and power supply, used for small system: ERNI p/n 054595. J5 will mate with: ERNI p/n 214346 used to crimp on 0.635 mm pitch 26 conductors flat cable. We used both twisted and straight flat cable without problems. Total cable length should not exceed 2-3 m. This length is driven mainly by the power supply voltage drop across the cable.
- J11: 3 pin 2.54 mm pitch single twisted pair connector for analog outputs, used for small systems: MOLEX p/n 705510037 (or equivalent). J11 will mate with MOLEX p/n 70066-0002. Cable braid must be connected to pin 3 (see following picture). On the MPD module there is the possibility to invert the polarity of the signal.
- J12: 30 pin high density (0.5 mm pitch) backplane connector for both digital control and analog output, used for large GEM: MOLEX p/n 55560-0307. J12 is used in alternative to J5 and J11.

I^{2}C addressing

APV25 needs to be uniquely addressed for configuration registers setup using I^{2}C bus.
Address is composed by 5 bits, ranging from 0 to 30: address 31 is reserved for broadcast.
In case of using flat-cable connection (in small systems) the I^{2}C addresses must be set via solder jumpers placed on the bottom side of the card: J6 → J10 will set bit 0 to bit 4 respectively (see fig. 3). Logic 1 is set when jumper is shorted.
In case of using backplane connection in large systems, the I^{2}C address is set by the backplane connector related to the position on the backplane itself. The jumpers J6 → J10 must be left open.

LVDS Terminations

High speed LVDS signals lines (clock and trigger) need to be correctly terminated in the system.
R17 is the termination resistor for clock while R19 is for trigger.

R17 & R19 are 100 Ω SMD resistors in 0603 case.
In case of using a backplane both of them need to be removed in all the front-end cards (termination is provided on the backplane).
In case of using flat cable connection, R17 & R19 must be left in place only in the latest board and removed in all others (termination must be placed at the end of the line).

Power supply checking

Input power supply voltage can be checked across tantalum capacitor C9 (see fig 2). It must be in the range 3 – 3.5 V. The current drawn is about 300-400 mA and depends on APV configuration settings.
Local power supplies can be checked across C7 (2.5 V) and C3 (1.25 V).

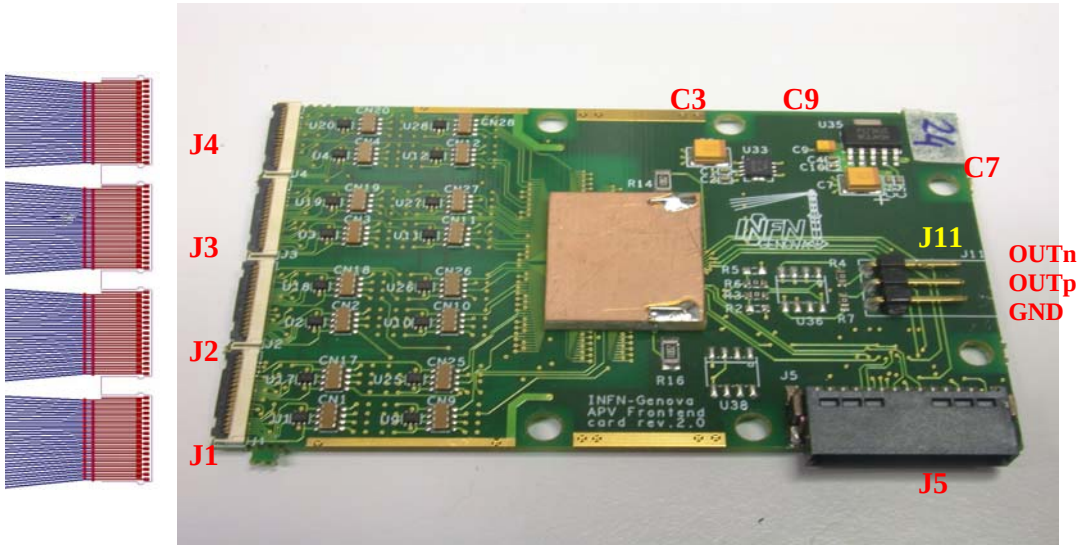

Fig. 2 Top side view of the APV25 front-end card with named components.
Analog output connector (J11) pinout is shown.
On the left the GEM readout Kapton fingers are shown. Top pin of each finger is unconnected.
Exposed gold plated copper bars can be used for ground connections.

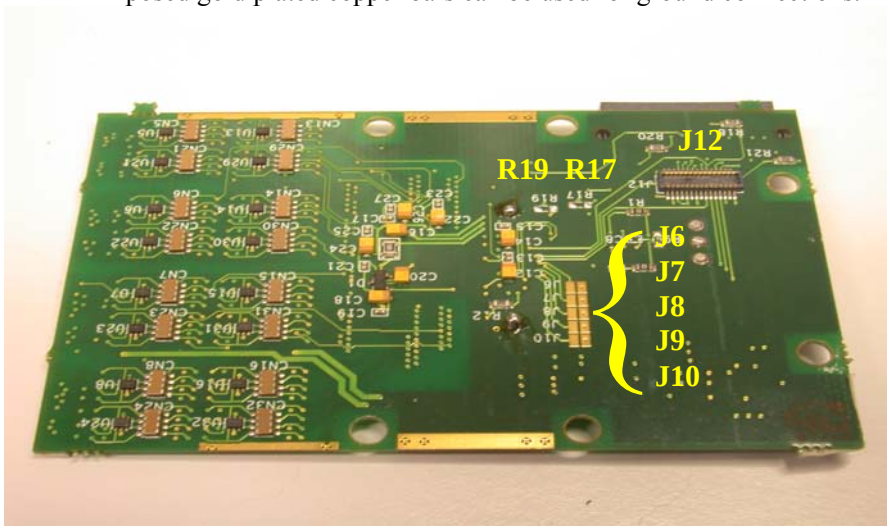

Fig. 3 Bottom side view of the APV25 front-end card with named components.

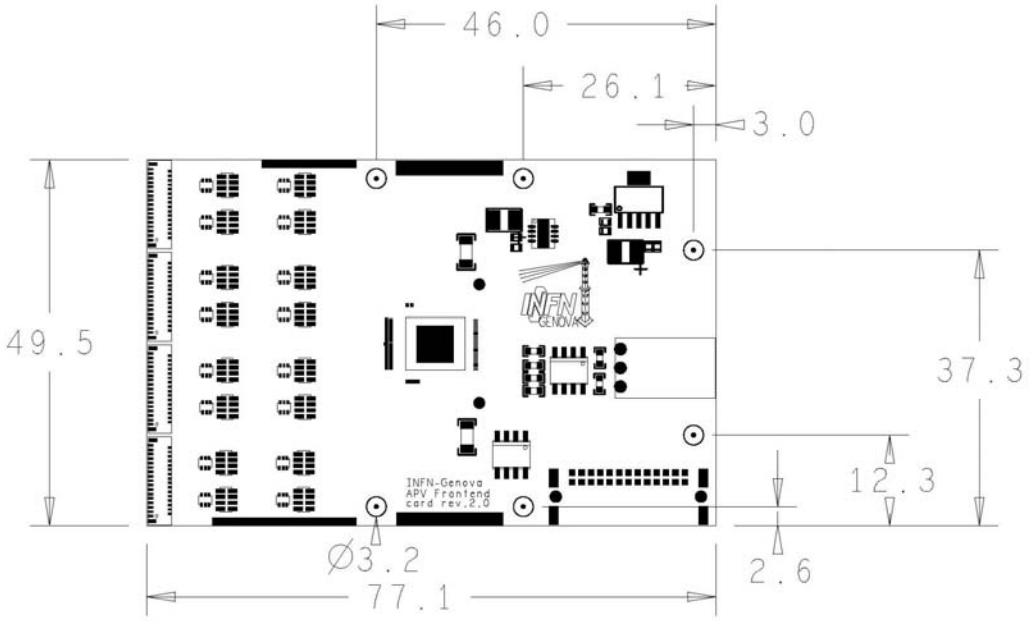

Fig. 4 Front-end card mechanical drawing with dimensions in mm

SBS Backplane

I/O connectors (see fig. 5)

Power supply connectors

- J8 and J12 (one each side) carry the 3-3.5 V power supply. They are 4 pins, 2.5 mm pitch header MOLEX p/n 22-05-7045 which mates with MOLEX p/n 50-37-5043.
  Two connectors are provided for cabling simplification. Cable size must be chosen considering the current drawn: about 300-400 mA each front-end card.
- J10 and J11 are standard FASTON connector used for grounding.

Digital control connectors

- J6: 19 pin HDMI-A connector, SAMTEC p/n HDMR-19-01-F-SM (or equivalent).
  We used SAMTEC cable HPSTP-19-xxxx-S-S for backplane to MPD connection (xxxx is the total length in mm, ranging from 1000 to 9999).
- J9: ERNI p/n 154819. Used only for testing and compatibility with front-end digital connector. Should not be used.

Analog output connector

- J7: 29 pin HDMI-B connector, SAMTEC p/n HDMR-29-01-F-SM (or equivalent).
  We used SAMTEC cable HPSTP-29-xxxx-S-S for backplane to MPD connection (xxxx is the total length in mm, ranging from 1000 to 9999).

I^2C addressing

Lowest 3 LSB of each APV I^2C address are hardwired depending on the position.
Starting from J6 (HDMI-A) these logic values are: 000, 001, 010, 011, 100.
In other words: front-end connected to J1 has 3 LSB = 000, connected to J1 → 001, and so on.
The upper 2 MSB of the I^2C address are set using SW1.
Putting the corresponding lever to ON will set the logic bit to 1.

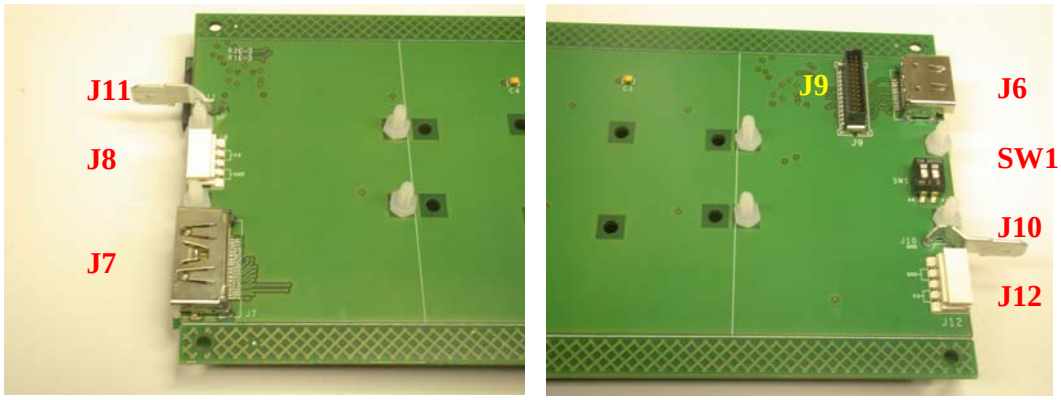

Fig. 5 Left & Rigth sides of the backplane card with named components.

HDMI connectors & cables pinout

J6 pin	Signal	HPSTP-19-xxxx-S-S name
1	T-1wire, ReadClk+, Analog1+	Data2+
2	Ground	Data2 Shield
3	N.C., ReadClk-, Analog1-	Data2-
4	N.C., Read+, Analog2+	Data1+
5	Ground	Data1Shield
6	N.C., Read-, Analog2-	Data1-
7	Trigger+	Data0+
8	Ground	Data0 Shield
9	Trigger-	Data0-
10	Clock+	Clock+
11	Ground	Clock Shield
12	Clock-	Clock-
13	RSTb	CEC
14	N.C.	RESERVED
15	SCL	SCL
16	SDA	SDA
17	Ground	DDC/CEC Ground
18	N.C.	+5V Power
19	N.C.	Hot Plug Detect

Pin 1, 3, 4 and 6 can have different connections on MPD side (set by jumpers), allowing different use of this module.
In case of SBS GEM detector, pin 1 will connect the temperature monitor. Pin 3,4,6 will be left unused.
ReadClk and Read differential LVDS signals have been introduced as other possible control signals, directly generated by MPD FPGA.
Analog1 and Analog2 differential analog signals have been introduced to be compliant with RD51 electronic system. In this case MPD can be directly connected to their front-end electronic boards. On MPD these signals are directly connected to ADC channels.

J7 pin	Signal	HPSTP-29-xxxx-S-S name
1	Out1+	Data2+
2	Ground	Data2 Shield
3	Out1-	Data2-
4	Out2+	Data1+
5	Ground	Data1Shield
6	Out2-	Data1-
7	Out3+	Data0+
8	Ground	Data0 Shield
9	Out3-	Data0-
10	Out4+	Clock+
11	Ground	Clock Shield
12	Out4-	Clock-
13	Out5+	Data5+
14	Ground	Data5 Shield
15	Out5-	Data5-
16	Out6+ (MPD side only)	Data4+
17	Ground	Data4 Shield
18	Out6- (MPD side only)	Data4-
19	Out7+ (MPD side only)	Data3+
20	Ground	Data3 Shield
21	Out7- (MPD side only)	Data3-
22	N.C.	CEC
23	N.C.	RESERVED
24	N.C.	RESERVED
25	Out8+ (MPD side only)	SCL
26	Out8- (MPD side only)	SDA
27	Ground	DDC/CEC Ground
28	N.C.	+5V Power
29	N.C.	Hot Plug Detect

Future Revision

All the informations previously reported are related to fornt-end card version 2.0.
A future revision is foreseen to have better placement around the Jlab GEM module.
In this revision the only modification is that the input connectors have been moved on the opposite side of the board.
The topmost pin of all the four input connectors is now connected to GND.
This new revision will be produced in april 2011.

The following pictures show the new version of the front-end card.

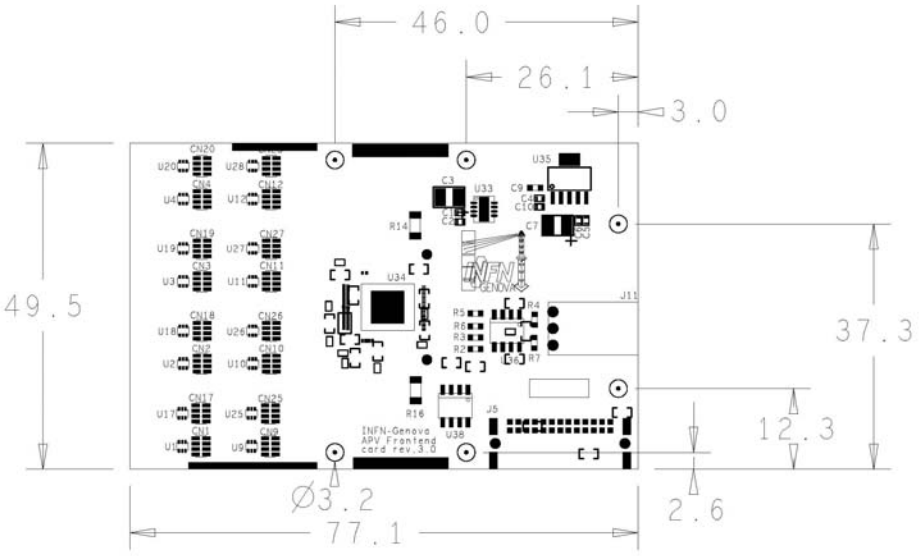

Fig. 6 Top view of the new revision. All the dimensions are unchanged.

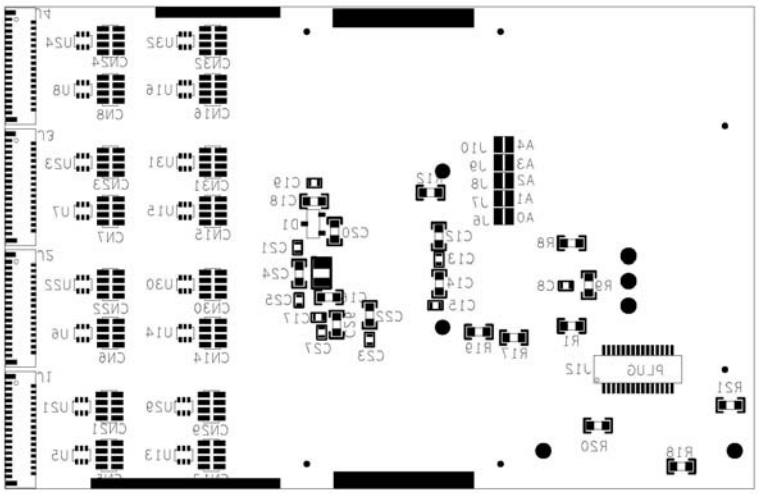

Fig. 7 Bottom view of the new revision.

References

- "APV25 User Guide v 2.2", 5th September 2001, Lawrence Jones (RAL)
- …