VETROC Tests Report

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Introduction: VETROC Board

The VETROC board is a high-rate pipelining TDC which together with a crate trigger processor (CTP) is self-triggering. The TDC words have a Dynamic Range of 32 bits, and each board has 128 channels for data input. Up to 17 boards (2176 channels) may be used with a single CTP. The VETROC has a bandwidth of four gigabits per second. The VETROC accepts any differential input (ECL, LVDS, etc.) from 100 mV to 4 V. The price for one board is less than $2000.

Triggers can be formed in two ways. The first method is a front panel trigger using external NIM electronics. This is useful for manually sending signals and simple triggers. The second method is triggering with a global trigger processor (GTP), essentially the same thing as a CTP, which uses data from the VETROC to form triggers. GTP triggering is useful for more complicated triggers such as cluster finding algorithms. The GTP trigger is coded in VHDL and burned onto field programmable gate arrays (FPGAs). The FPGA programming is done in the Altera made Quartus software. So far the VETROC has been tested with a simple M out of N trigger where a trigger is considered to have been formed if M channels out of a group of N channels see a hit. A cluster finding algorithm which detects clusters of two, three or four adjacent tubes firing has also been tested successfully.

Figure 1 shows how the data flows through the data acquisition system. Data is created by some external source such as a detector or a pulser and is sent into the VETROC. When the data arrives it is held in a buffer until a trigger is created. The GTP then checks the data to see if the trigger conditions are met and is capable of forming triggers at 31.25 MHz. This trigger data is then passed to the trigger interface (TI) which contains a 250 MHz clock that syncs the whole DAQ system. The TI can also used to set a minimum holdoff time after a busy signal is formed from a trigger which allows for a consistent and understandable dead time to be set. The trigger information is then sent to the signal distributor (SD) module which communicates that information to the other modules. Finally the CPU queries the VETROC to see if a trigger condition was met and if it was the VETROC then sends that data to the CPU from which it can be accessed and analysed.

Benchmark Test Results

The following tests were done with the GTP forming triggers based on a simple M out of N adjacent channels firing with $N = 5$ and $M = 1$ or $M = 2$. The first important aspect of the DAQ to test is if it can produce accurate TDC data. For this test a single 40 ns pulse was sent to two channels of the VETROC at a rate off 10 kHz from a pulser. One channel is used as a reference channel to remove the internal clock reference. If a reference channel is not used the TDC peaks are much broader than they should be with a width of about 32 ns instead of being a sharp peak (Figure 2). The 32 ns spread is a result of the VETROC forming triggers at a rate of 31.25 MHz. The VETROC should detect the leading and trailing edges of the pulse and they should be 40 ns apart. Figure 3 shows the TDC results seen in Figure 2 but uses a reference channel to remove the internal clock reference. Now two sharp peaks 40 ns apart are clearly visible as desired. For these tests a timing resolution of 1 ns was used, however timing resolutions as low as 20 ps have been observed by the DAQ group.

Using the same data as in Figure 3 the TDC time difference between successive hits in the same channel was calculated. This should show a difference of 40 ns since the widths of the pulses were 40

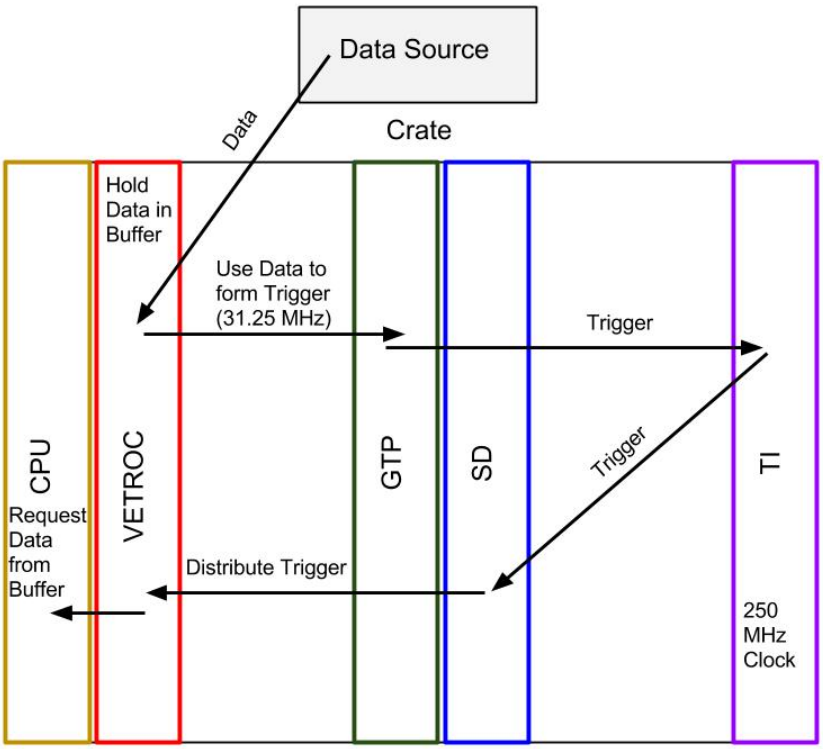

Figure 1. Data Flow Diagram. This diagram shows how the signal from a data source travels through the data acquisition system.

ns wide. This also allows the variance in time difference measured by the TDC to be examined. The results of this test can be seen in Figure 4. As expected the successive hits in the same channel are about 40 ns apart confirming that the VETROC is measuring the correct pulse width. The RMS of the time difference is about 0.5 ns indicating that the TDC data is reasonably tightly grouped. As a sanity check to be certain that our timing resolution was actually one ns a test was performed where the pulser sent pulses of varying width and then plotted these against the time difference between successive hits in the same channel (Figure 5). If the slope of this plot is equal to one then we have a one-to-one correspondence between nanoseconds read out by the TDC and nanoseconds in pulse width demonstrating that our TDC is really measuring in nanoseconds. The plot in Figure 5 is linear with a slope of one and an $r^2 = 1$ confirming our timing resolution of one ns.

Another important aspect of the DAQ system to measure is the amount of dead time seen at different data rates. Dead time results from the system going busy with a current event and being unable to record a new event. The TI sends a busy signal every time the system is handling data and unable to record new data. The amount of time the system stays busy for is not always constant, but one can set a holdoff time in the read out list for the TI which will force the system to go busy for a certain length of time. By setting a holdoff time one makes the dead time more understandable as the busy times never vary. The DAQ system sends data to the CPU in blocks of 100 events meaning that it stores 100 events in a buffer and only sends these across the back plane to the CPU when there are 100 of them. There is also a buffer which stores up to 10 of these 100 event blocks. Adjusting the number of events in a block or the

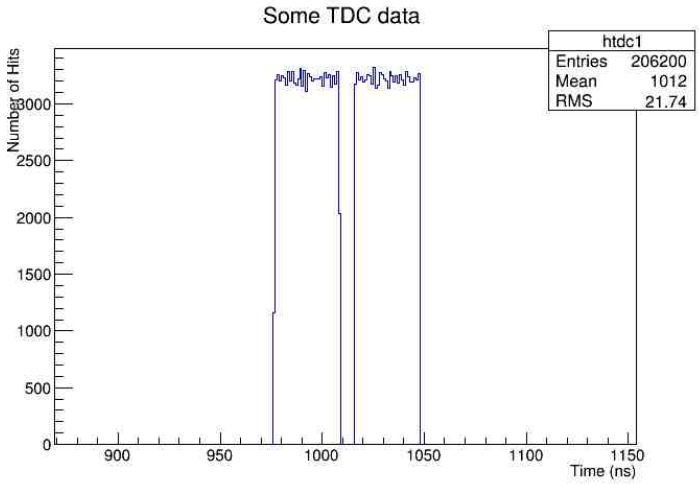

Figure 2. TDC Data without Reference Channel. Without a reference channel the TDC peaks are spread out due to the internal clock.

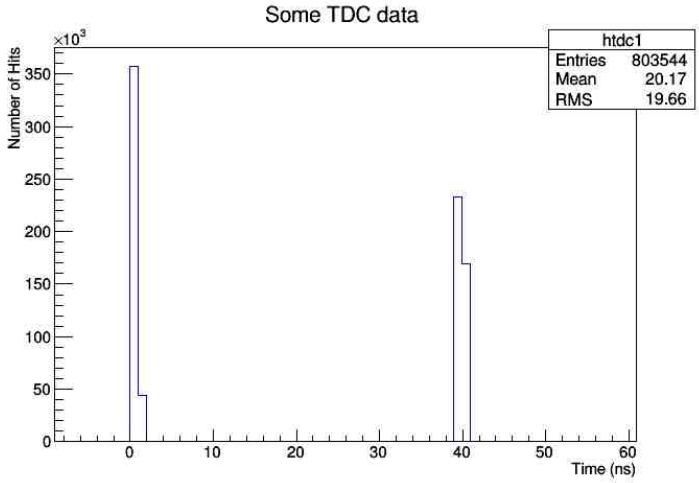

Figure 3. TDC Data with Reference Channel. With a reference channel the TDC peaks are sharp and located where they are expected.

number of blocks to buffer affects the maximum speed at which the system can operate. The numbers 100 events and 10 blocks were chosen as they seemed to be reasonable values but it is likely these could be further optimized.

Figure 6 shows a plot of busy signals output by the TI per second vs. the number of events sent to the VETROC per second for hit multiplicities one and five. A hit multiplicity of one means the system is receiving single pulses at whatever the data rate is and a multiplicity of five means the system is receiving a burst of five pulses at the data rate. Note that there is zero dead time if there are 100 times as many events sent to the VETROC as there are busy signals because the events are read off in blocks of 100. For example a data rate of 200,000 Hz that had a busy signal rate of 2000 Hz had zero dead time and a

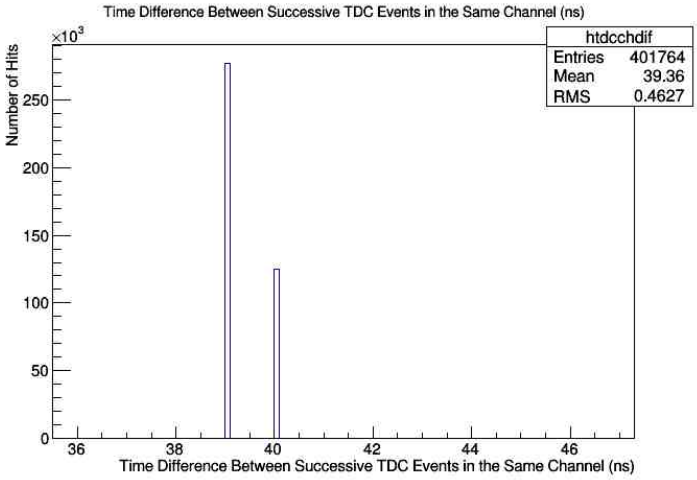

Figure 4. TDC Time Difference Between Successive Hits in the Same Channel. As expected the hits are about 40 ns apart with an RMS of 0.5 ns.

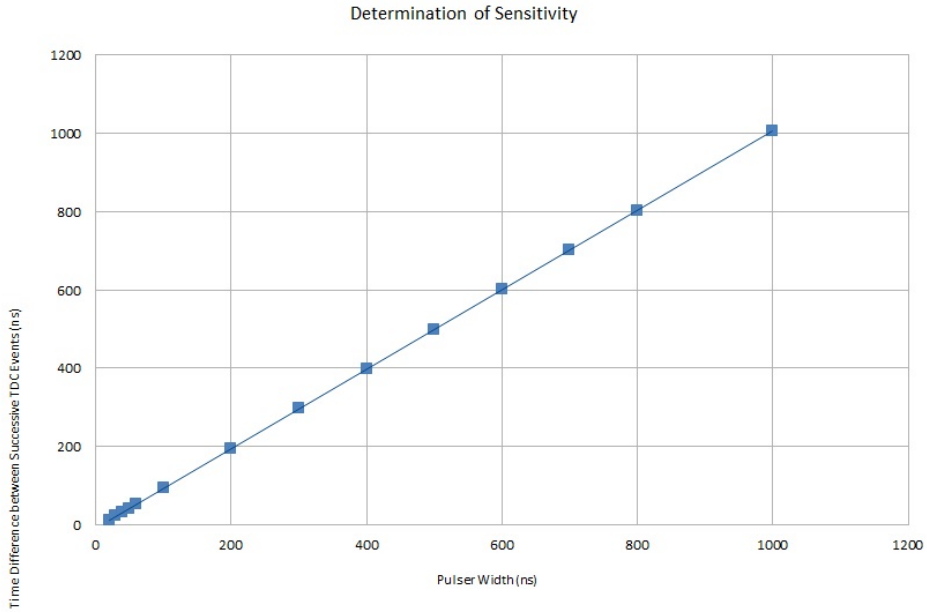

Figure 5. Pulse Width vs. Time Difference Between Leading and Trailing Edge. The slope is linear and equal to one thus one ns measured by the TDC corresponds to a one ns increase in pulse width as expected.

data rate of 100,000 Hz with a busy signal rate of 800 Hz has a dead time of 20 percent. Another way to see this data is to look at the percentage dead time vs. the data rate as shown in Figure 7. As expected the tests with a hit multiplicity of five have greater dead time than those with one as there is more data

to process with multiplicity five. For a hit multiplicity of one zero dead time was observed up to data rates of ∼250 kHz and for hit multiplicity five up to ∼166 kHz. Above these data rates the dead times begin to increase until the system fails around 520 kHz and there is 100 percent dead time.

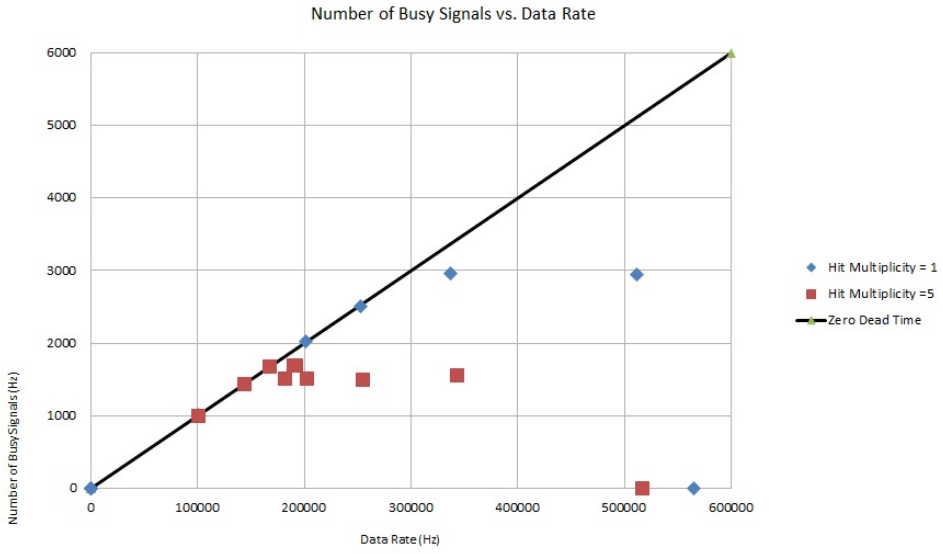

Figure 6. Data Rate (Hz) vs. Busy Signal Rate (Hz). The black line represents zero dead time. The system fails above rates of about 520 kHz.

The final benchmark test performed on the VETROC TDC was to determine its two-hit resolution. The two-hit resolution is a measure of how close two signals can be together and still be distinguished by the TDC as two separate events. To measure the two-hit resolution of the TDC a single pulse, a leading and a trailing edge, was sent into the VETROC. By making the width of that pulse smaller and smaller until the TDC stops distinguishing the leading and trailing edges as separate the two-hit resolution can be determined. Figure 8 shows the time difference between the pulses leading and trailing edges vs. the percent of events where the TDC correctly distinguished the leading and trailing edges as two separate signals. For pulse widths as small as 8.8 ns (114 MHz) 100 percent of both edges were correctly detected and for pulse widths of 7.2 ns (139 MHz) the TDC resolved both edges correctly only 90 percent of the time. Below 7 ns the TDC begins to miss edges more and more frequently.

Conclusion/Future Work

The DAQ system has so far only been tested with a few (five or less generally) channels receiving data simultaneously. In more realistic scenarios like the A_1^n experiment to run in hall A hundreds of tubes will be collecting data at one time so testing the system with more tubes is important. Further the DAQ system has only been tested with nicely ordered data from a pulser and should be tested with random data from a source such as cosmics or some other real data. To these ends William and Mary has moved a prototype detector with 90 PMTs to the test lab at Jlab. This prototype detector is planned to be tested with a fastbus DAQ system and then with the VETROC DAQ system. This will give an opportunity to test real random data on many tubes at once.

A cluster finding algorithm for triggering has been successfully implemented for the VETROC DAQ

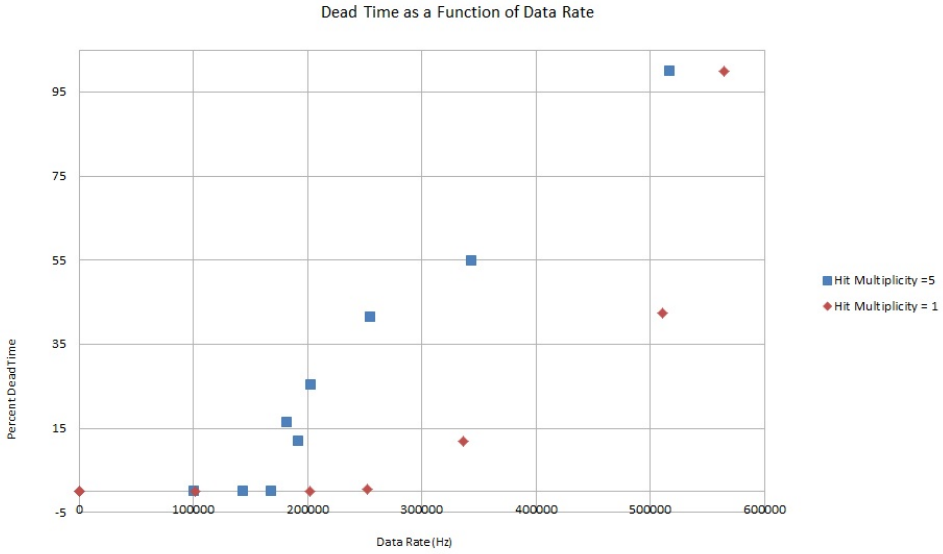

Figure 7. Percentage Dead Time vs. Data Rate. This plot shows the increase in dead time as the data rate increases for hit multiplicities one and five.

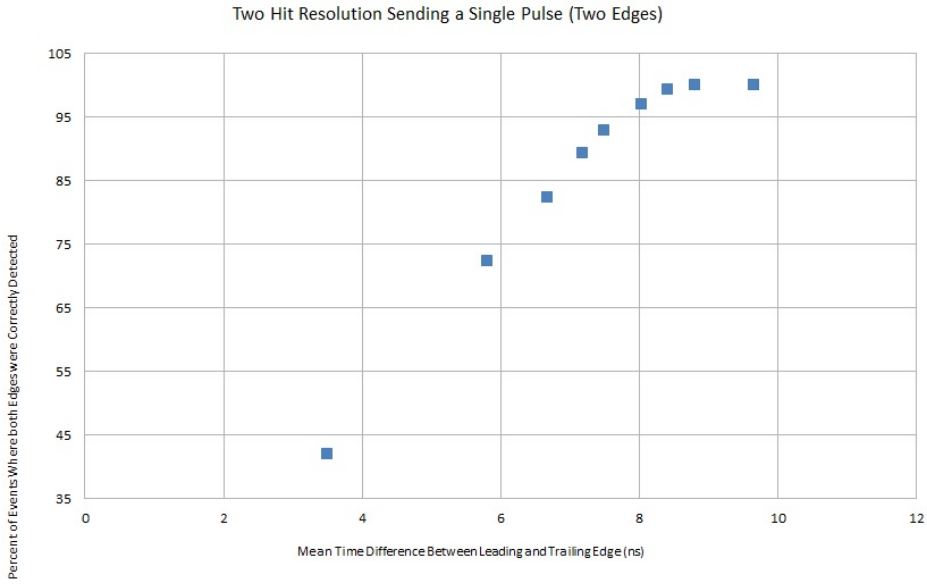

Figure 8. Determination of Two-Hit Resolution. Plot showing the pulse width vs. the percentage of times the TDC correctly observed both edges.

system but it will likely need refinements after it is tested with real data. Further analysis software will also need to be developed as this project proceeds. There is also an issue with the CODA read out list

where sometimes the last buffer from the previous run is read out as the first buffer of a new run causing old data to be seen in a new run. Overall the VETROC board looks to be a powerful way to form triggers and collect data. It is able to read thousands of channels at a high data rate while having extremely good timing resolution. Its flexibility and precision will allow it to be adapted for use in a wide array of experiments at Jlab in the coming years.