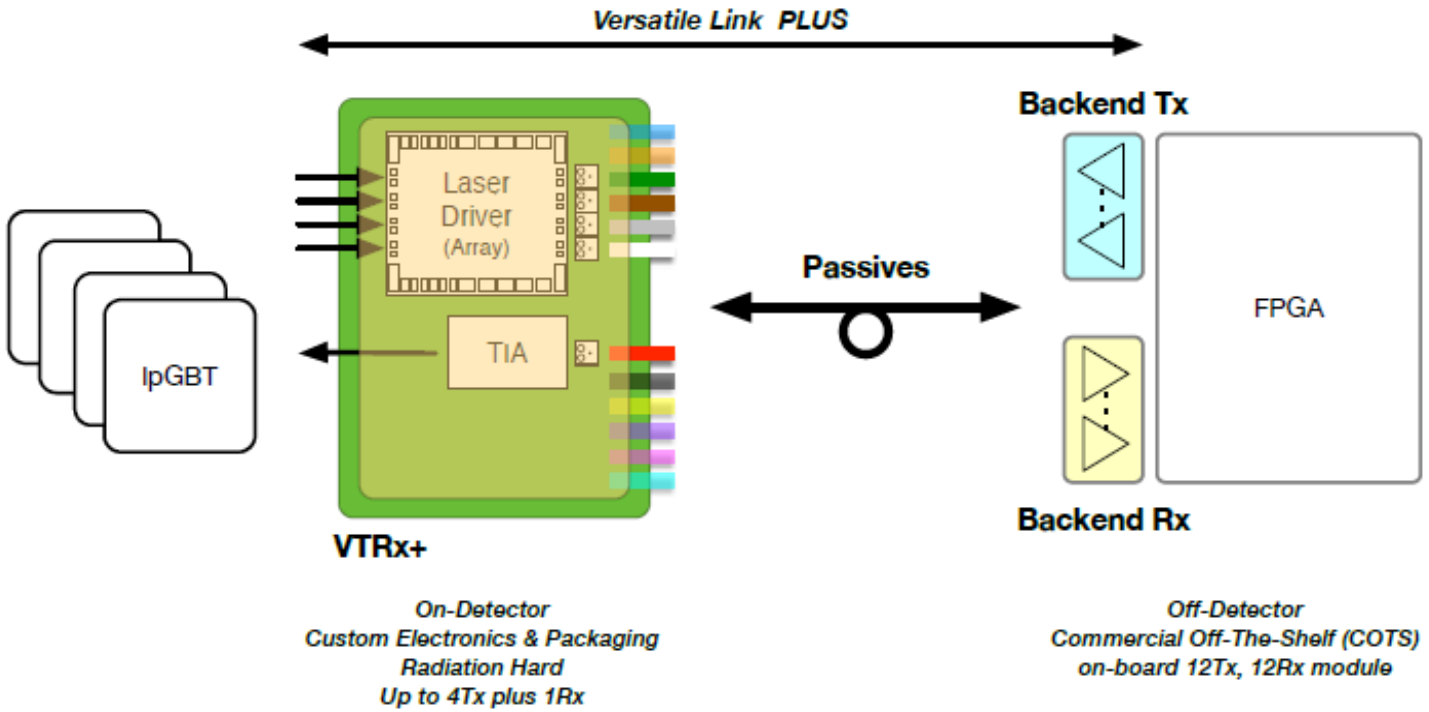
CERN Rad Hard Components for TDIS - (updated 1/23/22 - EJ)

- 2nd generation data transmission components
  - lpGBT, VTRX+ (for High Luminosity LHC)

- 2nd generation power conversion components
  - bPOL12V, bPOL2V5, linPOL12V (for HL LHC)

- Estimate number needed and cost to instrument TDIS mTPC

Versatile Link+ (lpGBT)



uplink

5.12 or 10.24 Gb/s

downlink

2.56 Gb/s

lpGBT uplink modes

5.12 FEC5 – 4.48 Gb/s user data

5.12 FEC12 – 3.84 Gb/s user data

10.24 FEC5 – 8.96 Gb/s user data

10.24 FEC12 – 7.68 Gb/s user data

FEC = Forward error correction

(FEC12 more robust than FEC5)

Data transmission components

- lpGBT – includes some of GBT-SCA functionality (I2C, GPIO)
  - **35 CHF** (~$35)
  - Pre-series parts available in small quantities
  - Production quantities for users at beginning of **2023**

- VTRx+ **(**** 4 Tx, 1 Rx ****)**
  - **200 CHF** (~$200)
  - Pre-series parts available in small quantities
  - Production in monthly batches starting 2022
  - Batches reserved for LHC experiments through 2024
  - Other users after end **2024**

1 – SAMPA in Triggered Mode

- Modest experiment trigger rate (~6 KHz)
- High channel hit rate (~1 MHz)
- Small mTPC drift time (1.5 µs)
- More efficient to operate the SAMPA chips in triggered mode than in continuous mode

- Set channel thresholds below pedestal – all channels report samples for each trigger
- 2 µs capture window, 20 MHz ADC sampling (40 samples/window, 10 bits each = 400 bits/ch/trig)
- 50 bit header + 20 aux bits for each channel => 470 bits/ch/trig => 15,040 bits/chip/trig

- 25 KHz triggers => 376 Mb/s/SAMPA
- Use 3 e-links @ 160 Mb/s each from SAMPA to lpGBT
- lpGBT: 5.12 Gb/s FEC12 supports 24 e-links @160 Mb/s each
- **8 SAMPA → 1 lpGBT → 1 VTRx+**

1 – SAMPA in Triggered Mode

- **32K** channels => **1000** SAMPA
- lpGBT cost: $35 x 125 = $4,375
- VTRx+ cost: $200 x 125 = $25,000
- **Total: $29,375**

- (Suggest 20% more for spares)

Notes:

- Front-end card with 8 SAMPA + 1 lpGBT + 1 VTRx+ may not be the optimal solution for the geometry of the mTPC.
- 1 lpGBT can support 12 SAMPAs when operated at 10.24 Gb/s FEC12. Negatives: Front end card becomes more complex with additional SAMPAs; receiving end of 10.24 Gb/s link is more expensive.

2 – SAMPA in Streaming Mode (DAS)

- **ALICE card**: 2.5 SAMPA → 1 GBT (SAMPA V4 – 160 ns shaping time)
- Can stream **ALL** ADC samples at **5 MHz** sampling rate (DAS mode)
- Also can stream at **20 MHz** sampling with zero suppression applied (DSP mode)

- For **SAMPA V5**, DAS mode must be at **10 MHz** sampling to be equivalent (80 ns shaping time)
- Can do: **2 SAMPA → 1 lpGBT** at **10 MHz** sampling (DAS mode)
- lpGBT 10.24 Gb/s FEC12

- **8 SAMPA → 4 lpGBT → 1 VTRx+** (unlike VTRx, VTRx+ has **4 TX**, 1 Rx)

- lpGBT cost: $35 x 500 = $17,500
- VTRx+ cost: $200 x 125 = $25,000

- **Total: $42,500**

3 – SAMPA in Streaming Mode (DSP- zero suppression)

- **1 MHz** average hit rate per channel, **20 MHz** ADC sampling
- Frame = 1000 samples = 50 µs => 50 hits/frame/ch
- Zero suppression: 1 hit ~ 9 samples (3 pre, 3 above threshold, 3 post) (**80 ns** shaping time)
- 1 hit = 100 bits (ADC = 90, TDC = 10)
- Bits/frame/ch = 5060 (100 bits/hit x 50 hits/frame + 50 (header) + 10 (counter))
- SAMPA bits/frame = 161,920 (5060 bits/frame/ch x 32 ch)
- **SAMPA bit rate = 3.24Gb/s** (161,920 / 50 µs)
- Use 11 e-links @ 320 Mb/s each

- **2 SAMPA → 1 lpGBT** can handle **1 MHz** average hit rate per channel with **20 MHz** ADC sampling (zero suppression applied) - lpGBT 10.24 Gb/s FEC12

- **8 SAMPA → 4 lpGBT → 1 VTRx+**
- (**$42,500)**

Recommendations

- For TDIS buy enough lpGBT to allow for the streaming option
- A streaming architecture will incur additional costs at the concentrating units (FELIX PCIe cards) where 4x the number of transmission links must be handled

- Since **lpGBT** are relatively cheap, buy enough to cover other prototyping work (e.g. SoLID). No equivalent chip is available.
- **VTRx+** are expensive – buy enough for some prototyping of other projects. Alternative fiber optic transceivers may become available (SMU)

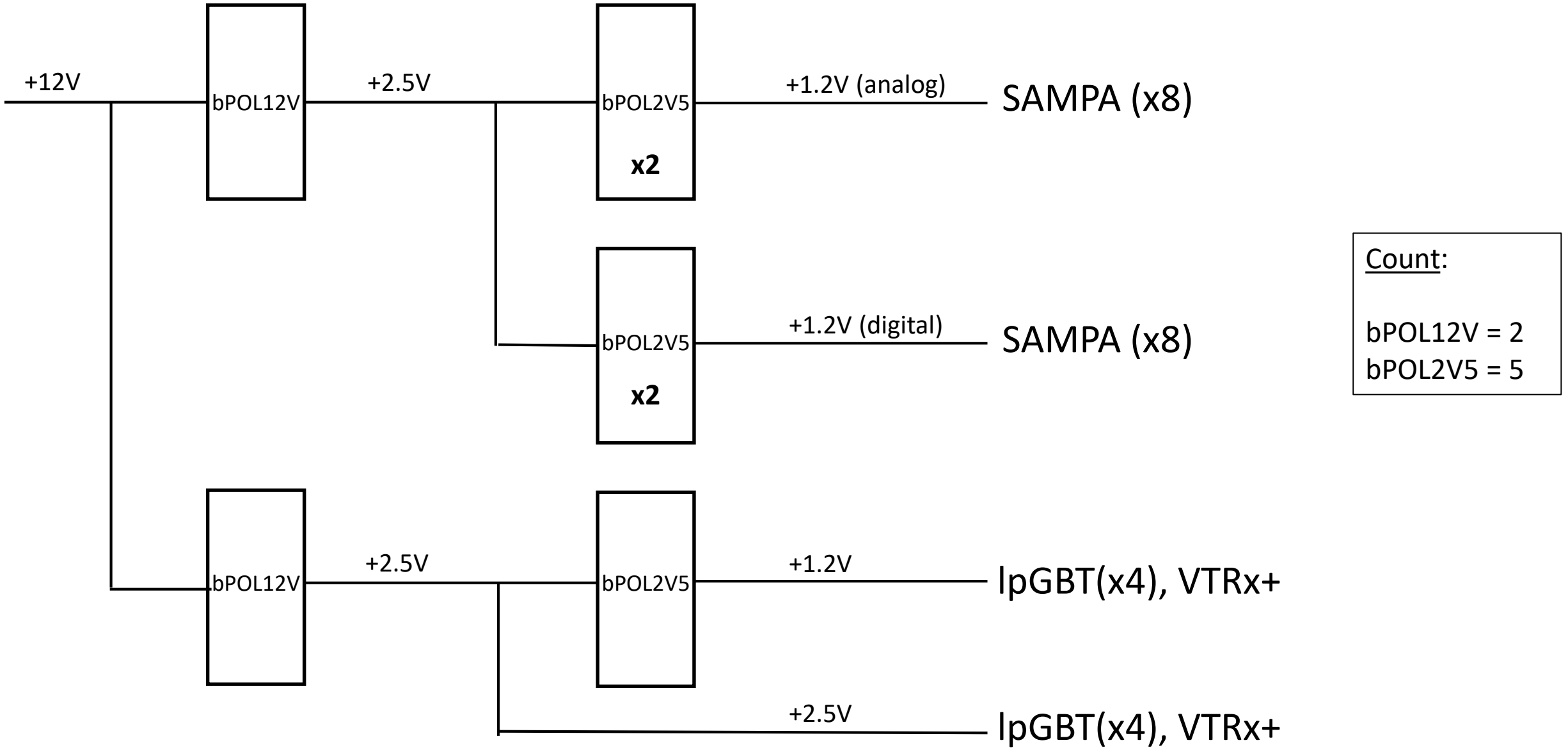
Power (DC-DC converters)

- **bPOL12V** (5.5 - 12V input, 0.63 - 5V output @4A)
  - **10 CHF** (~$10)
  - Prototype quantities now
  - Large quantities in early 2022

- **bPOL2V5** (2.1 – 2.5V input, 0.6 – 1.5V output @3A)
  - **10 CHF** (~$10)
  - Prototype quantities now
  - Large quantities in early 2022

- **linPOL12V** (5 – 12V input, dual 0.9 – 3.3V output (80mA @1.4V, 25mA @3.3V))
  - Possibly use for SAMPA reference voltages

Possible Power Architecture (8 SAMPA → 4 lpGBT → 1 VTRx+)



Count:

bPOL12V = 2
bPOL2V5 = 5

Front-end Power Component Cost

- **32K** channels => **1000** SAMPA => **125** FE cards (8 SAMPA per FE)

- bPOL12V cost: $10 x 2 x 125 = $2,500
- bPOL2V5 cost: $10 x 5 x 125 = $6,250
- linPOL12V cost: $10 x 2 x 125 = $2,500 (est. 2 per FE – reference voltage)

- Total FE card power = **$11,250**

TDIS Cost

- FE card data transmission = $42,500
- FE card power = $11,250

- TDIS Total = **$53,750** (32k channels)