# INFN GEM Update:

#### 4/21/21-4/27/21

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#### **Recent Activities:**

### TEDF Activities (Apr. 21-27)

- Had all remaining MPDs for INFN GEMs in TEDF modified.
- Found one APV card that may have disconnected from Kapton fingers on layer J2
- Created noise comparison plots for run 768 and 915 of all 8 MPDs
- Changed spacers on the front plane of the GEM BigBite frame, more clearance now.
- Did a brief (~ 1 hour) test of GEM HV
- With NIM clock from distribution box to input I1 on each MPD. Found that microswitch SW1.1 OFF and SW1.2 ON provides synchronized clock to MPDs in both UVa and INFN crates. After recent MPD firmware update.
- Got mpdLibTest and readHisto macro working for UVa layer in TEDF.
- Since we changed to the synchronized clock and update MPD firmware, the clock phase changed for both INFN and UVa layers. This has altered Low Level Histograms. We have produced sample plots and will use this as a guide for optimal clock phase.

#### Common Mode Comparison: TEDF Apr. 21

Run 768: all MPDs, no modified, narrow RMS, no faraday cage Run 915: all MPDs modified, narrow RMS, no faraday cage Compares MPDs 3-10

Integra

normalized by

Entries

0.01

-600

-200

200

400

600

ADC

commonMode(TAII\_T0) h commonMode(TAll T0) common mode variation [ADC] Entries 2241000 600 Mean x 54 Mean y 3.974 0.06 Run 768, 8 Unmodified Std Dev x 31.18 Run 768 Run 768, 8 Unmodified 400 Run 915, 8 Modified Std Dev v 30.18 Run 915, 8 Modified Entries 41500 0.05 Mean 4.006 200 Std Dev 27.81 0.04 Run 915 0.03 Entries 49140 -200 4.305 Mean 0.02 31.45 Std Dev -400

20

40

60

80

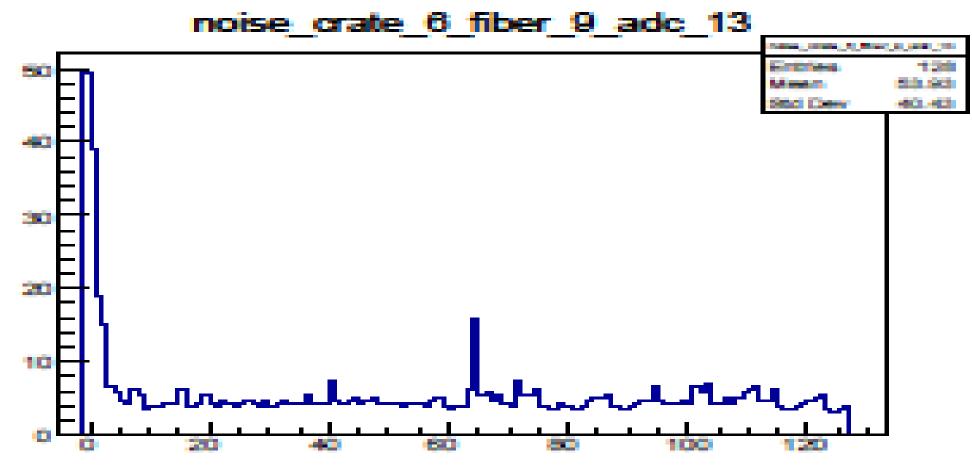
-600

#### APV wise common mode variation distribution

100 apv unique id

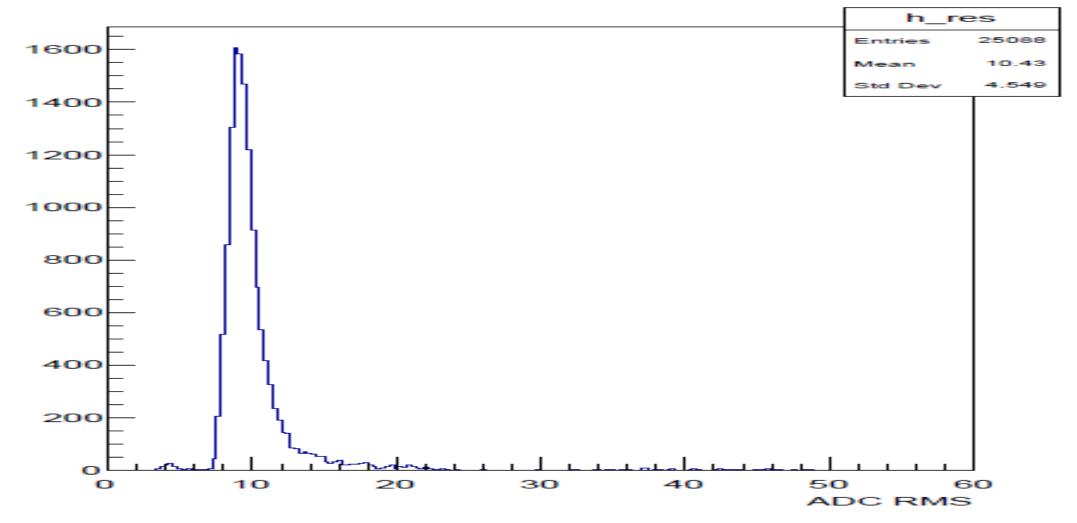
#### Pedestal RMS plots (ADC Value vs Channel #), Run 915 Apr. 22

- For the last APV card on the 3<sup>rd</sup> backplane of MPD 8, on layer J2
- Expect the baseline of the RMS to be around 10 ADC. This one has a baseline of around 5 ADC
- Indicative that the APV ZIF connector has disconnected from the Kapton fingers
- Could be verified with cosmic data
- Should be evaluated when layers are decabled



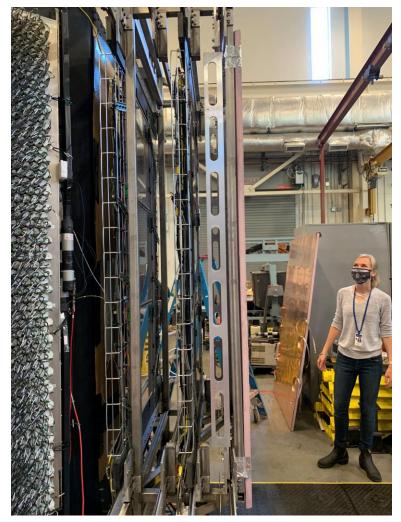
Pedestal RMS plot for all channels (Count vs ADC RMS), Layer JO & J2 Run 915 Apr. 22

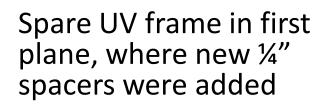
• Raw Pedestal value.



#### RMS of All Channels

# New Spacers BigBite GEM frame and UV frame test Apr. 22





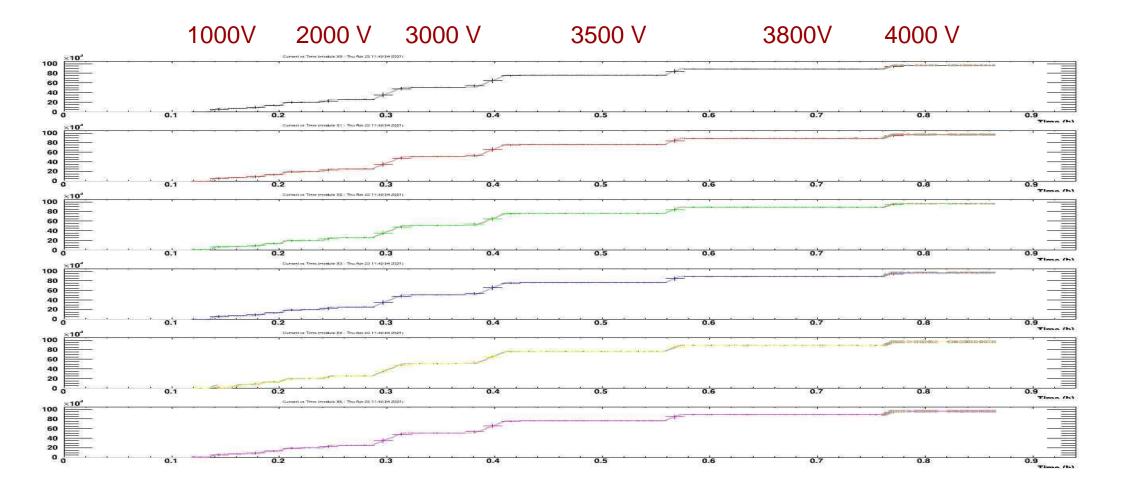


Completed by Sean, Holly, and I Outlined in Red is the new spacer at one corner Rough idea of the clearance

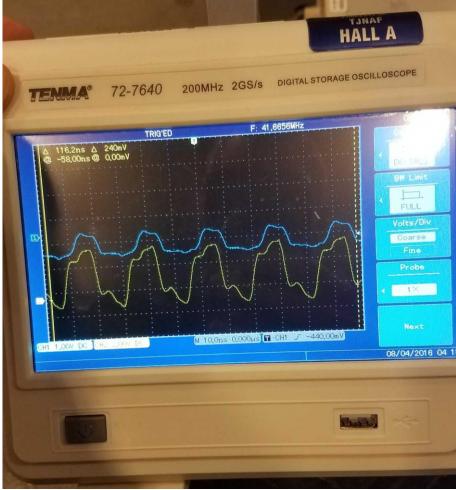


#### Brief HV Test: TEDF Apr. 22

Increased N2 flow to about 340 cc/min per layer Took pedestal runs of 916, 917, 918, 919, 920, 921 and created plots Need to do longer tests, at least a day to check stability.



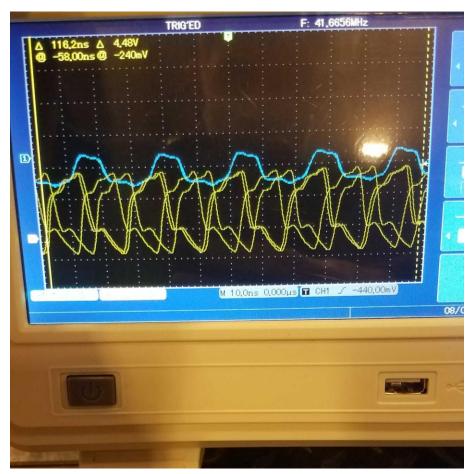
# Clock Distribution and Clock Phase Apr. 26-27



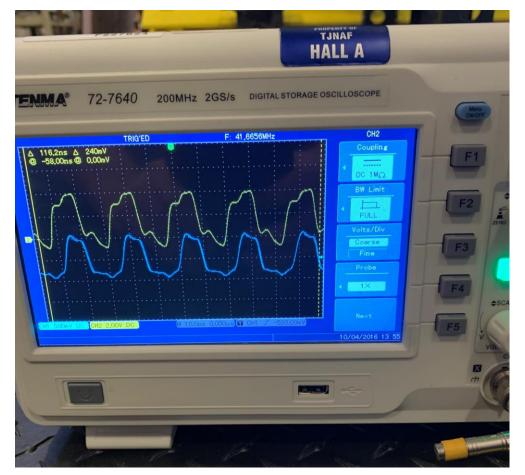
Clock is synchronized. Blue is from NIM distribution box. Yellow is clock from O1 on an MPD in Uva crate. SW 1.1 OFF SW1.2 ON

- Microswitch SW1.1 OFF and SW1.2 ON provides a synchronous NIM clock to all MPDs. Verified with oscilloscope.
- Somehow changing clock microswitch or firmware update caused slight shift in clock phase. Such that Low Level Histograms become flagged as anomaly.
- Definition of process for determining optimal clock phase needs to be understood
- Sean and I both worked on this since Apr. 23
- NIM clock is 41.6 MHz repeating. TTL (internal to MPD) is 40 MHz

# Clock Distribution Apr. 26-27

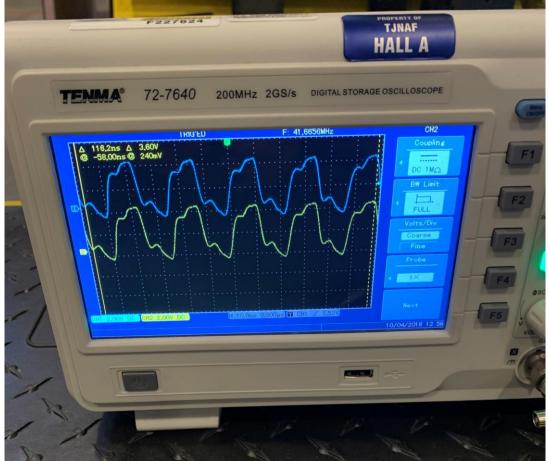


Clock is unsynchronized. Blue is from NIM distribution box. Yellow is clock from O1 on an MPD in INFN crate. SW1.1 ON SW1.2 OFF

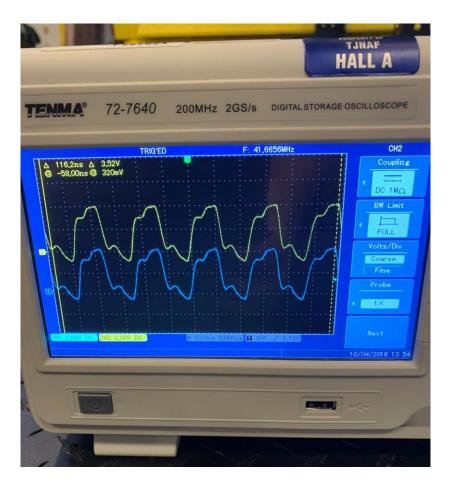


Clock is synchronized. Blue is from NIM distribution box. Yellow is clock from O1 on an MPD in INFN crate. SW1.1 OFF SW1.2 ON

# Clock Distribution Apr. 26-27

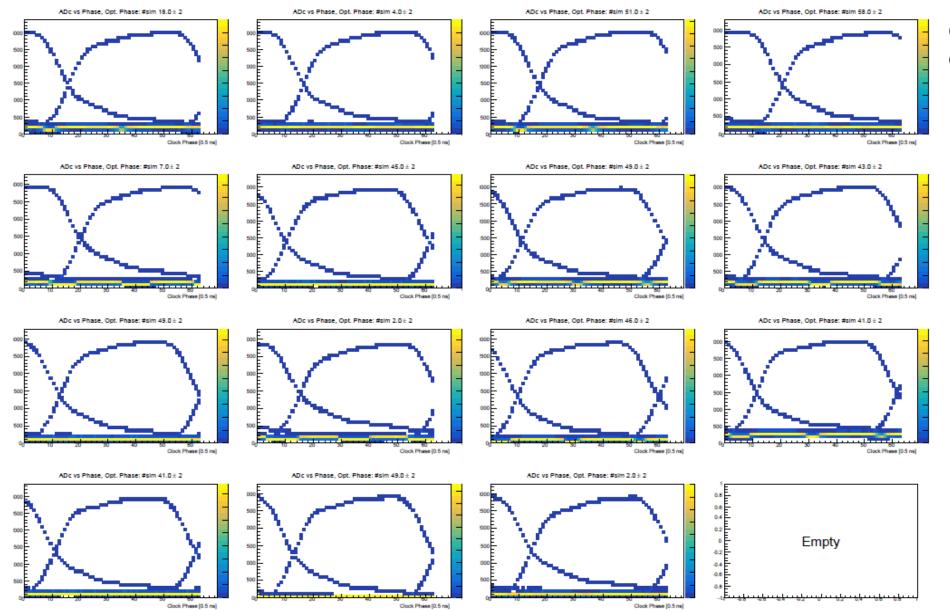


Clock is synchronized. Blue is clock from O1 on an MPD in UVa crate. Yellow is clock from O1 on an MPD in INFN crate. SW1.1 OFF SW1.2 ON



Clock is synchronized. Blue is clock from O1 on an MPD in INFN crate. Yellow is clock from O1 on a different MPD in INFN crate. SW1.1 OFF SW1.2 ON

## Clock Phase Apr. 26-27



What is the best way to determine the optimal clock phase?

# What to do next?

- Test Lab GEM Chambers
  - Change to metal cable trays for layers J1 and J3
  - Resolve Low Level Plots, due most likely to cable connections
  - Evaluate pedestal RMS plots and look for any noise cards, potentially altering APV cards
  - Once pedestals look good, take cosmic data and evaluate Hit Maps
  - If time permits resolve J4
- GEM Chambers in BigBite
  - Setup any remaining software/programs for INFN GEMs in TEDF configuration.
  - Take DAQ runs at least once a day to test DAQ stability.
  - Setup cosmic trigger and scintillators.
  - Systematic check of clock phase with synchronous clock.
  - Take pedestal data and check multiple analysis forms: common mode subtraction, zero suppression, etc. for all TEDF GEMs
  - Look for any noise issues and see if we need to adjust grounding.
  - Test GEM HV for longer, probably will coincide with cosmics.
  - Documentation for LV, Low Level Troubleshooting, and in general. Basically manual update.

# Questions?

