TDIS Meeting 11/14/17

Nilanga update

- getting ready for proposal
- Eric Christy to join TPC and MRI efforts
- Working on draft proposal

Ed update

- Pursuing front end cards and (tested!) readout unit used in ALICE
- SAMPA chip run January/February
- Need to map connector on front end card into our GEMs – only thing we would have to develop
- PCI express platform (only needs high end PC, no crate)
- ALICE and LHCb will both use this (unique FPGAs, interface in ToolKit)
- SAMPA chip is preamp, on front end card
- All is also rad hardened (readout must be in non-radiation area)

Me

- Rolf requesting streaming DAQ budget
- Next meeting's talk – Ed to present draft budget!

Simulation

- Marco working on rates from other particles, also considering readout planes and other materials
- Also looking at occupancies at different radii to help with pad size determination
- Rachel working on Garfied for mTPC design, hasn't moved further on resolution for kaon-TDIS

See Paul's talk! Some discussion during…

- Assumes mTPC
- Useful range for particles is 90 +/- 70 degrees (too much energy loss in target beyond that)
- Nilanga comment… to go down to 200 ns need to have some pattern-recognition programming? Then, do we really need to keep reading for 1 microsecond? Paul just trying to get some idea of pulses likely to overlap on same pad – how much effort do we need to do to disentangle multiple pulses?
- Thia comment that highest rate has strong (~90 degree) angular dependence, likelihood that two tracks come at same angle small
- Total occupancy is more like ~65%
- Bogdan comment that we could look at single hits first, then use multiple hit pads for additional analysis to improve resolution (maybe only 3 pads in a track of 20 would be difficult to distinguish)
- Comparing to ALICE… they have a 4 layer GEM, we would have 3 (or maybe 2 per Nilanga)

- Ed: SAMPA has a 20MHz option – could have 50 ns sampling (but lowest shaping time is still 160 ns) – higher sampling rate could help us distinguish 2 pulses
- Need to add time stamp to data rate calculations
- 4 GB/s, reduced by level 2 (for instance using only 3 TPC sub-chambers) to get lower rate going to disk
- Nilanga noted that ALICE has recognition software, and reduce their rate on the board to 1GB/s
- Also use zero suppression, pulse characterization,…
- 4 GB/s is ***worst*** case (doesn't take occupancy into account, etc.) – doable!
- NIlanga question… can we operate as 10 independent chambers? Yes… stamp to correlate back together.

Bogdan announced mid-February SBS collaboration meeting – should have a TDIS talk

Also – please volunteer for our invited talk at Chile workshop!

Streaming DAQ workshop at MIT end of January, Graham planning to attend