SAMPA response to a test pulse

A charge of approximately 80 fC is injected into the input in a 2.5 ns period. This is accomplished by applying a fast negative voltage step (80 mV) on a 1 pF capacitor connected to the input. The red curves in Figures 1–3 are the expected pulse shapes from the SAMPA shaping circuitry.

The data shown in Figure 1 was acquired with the SAMPA chips in Direct ADC Serialization (DAS) mode. In DAS mode the DSP section of the SAMPA is bypassed and all the raw ADC samples are continuously streamed off the chip. An ADC sampling rate of up to 10 MHz is possible in DAS mode. However, data bandwidth limitations of the ALICE Front-End Card that supports the SAMPA chips restrict the ADC sampling rate to be 5 MHz or less in DAS mode.

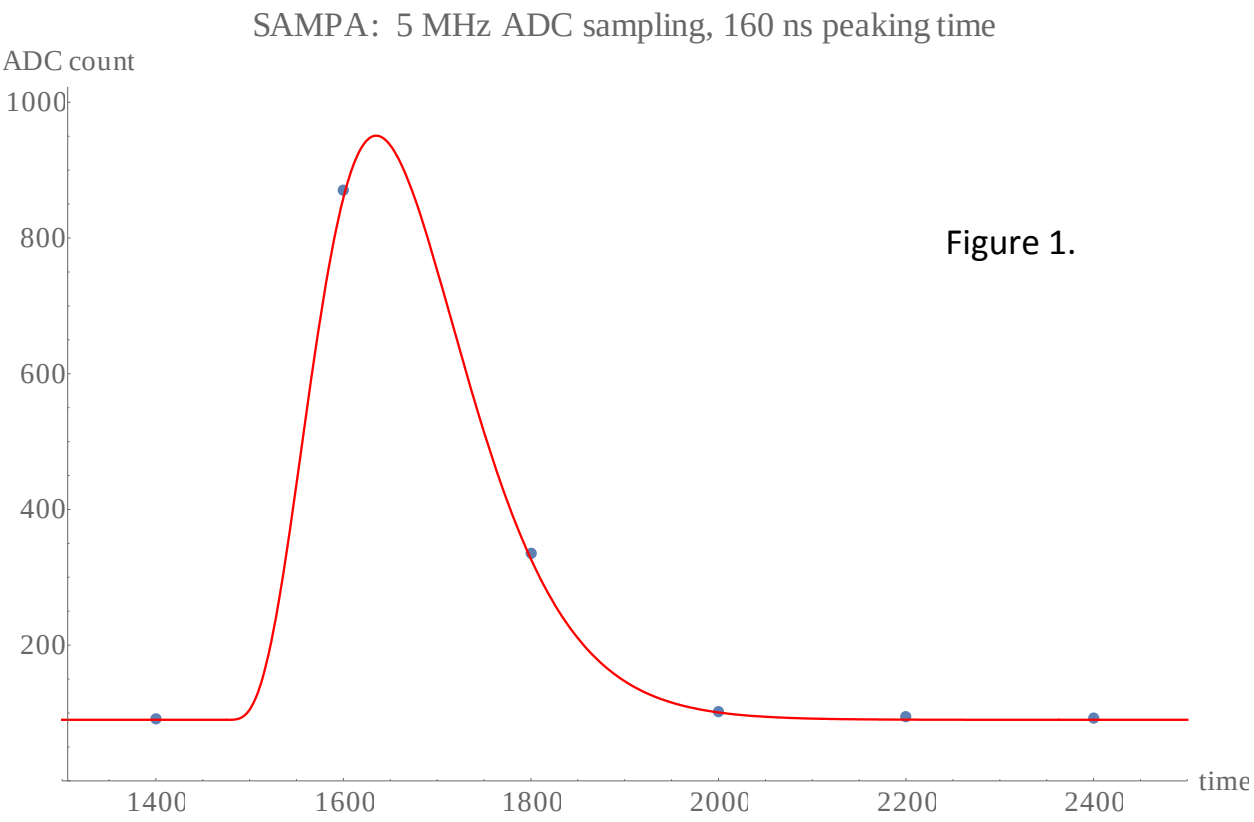

Figure 1.

The data shown in Figure 2 and Figure 3 were acquired with the SAMPA operating continuously with its DSP configured in zero suppression mode. A threshold is set slightly above the baseline (pedestal) for each channel. A group of ADC samples (a cluster) that exceed the threshold is appropriately packetized and streamed off the chip. No triggering signal is required. In the pulse data shown 3 pre-cluster samples and 7 post-cluster samples were included with the cluster data to help visualize the baseline. Data in Figure 2 was acquired with 10 MHz ADC sampling. Data in Figure 3 was acquired with 20 MHz ADC sampling (SAMPA maximum).

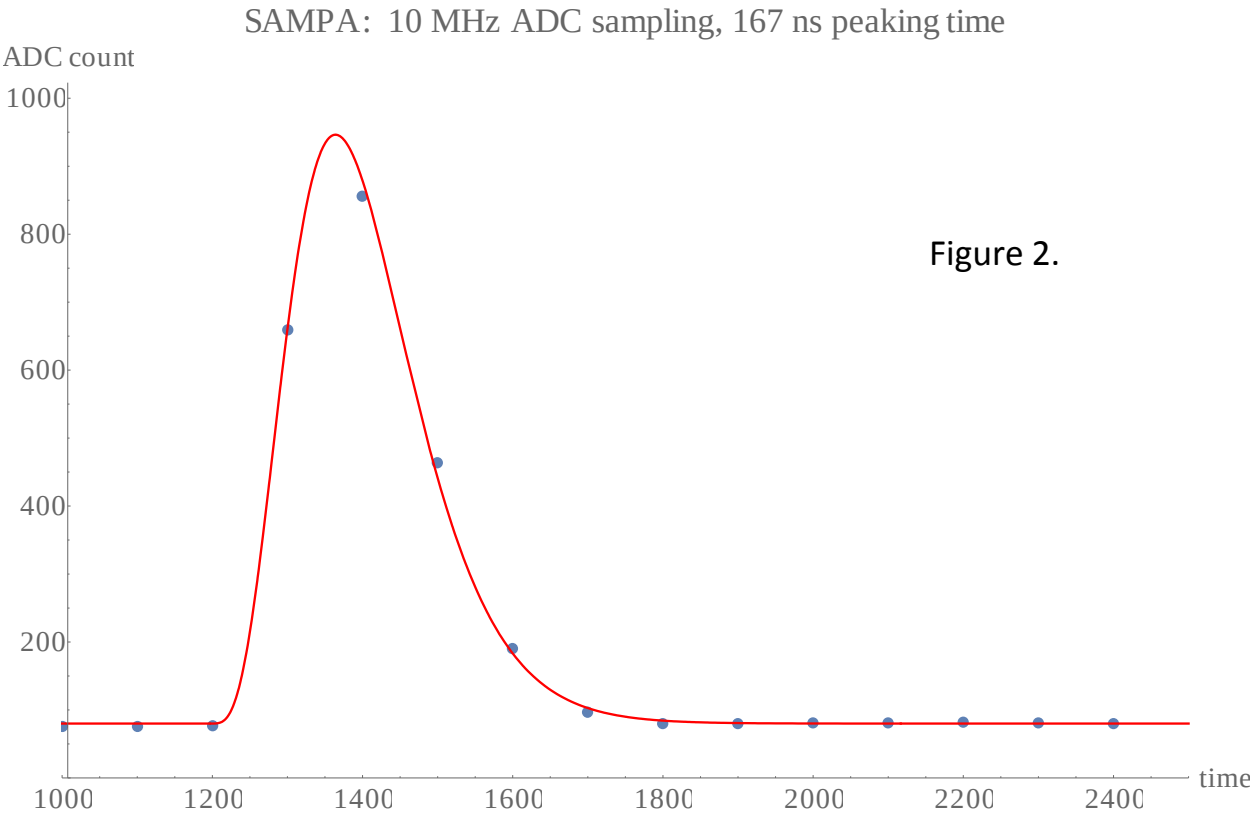

Figure 2.

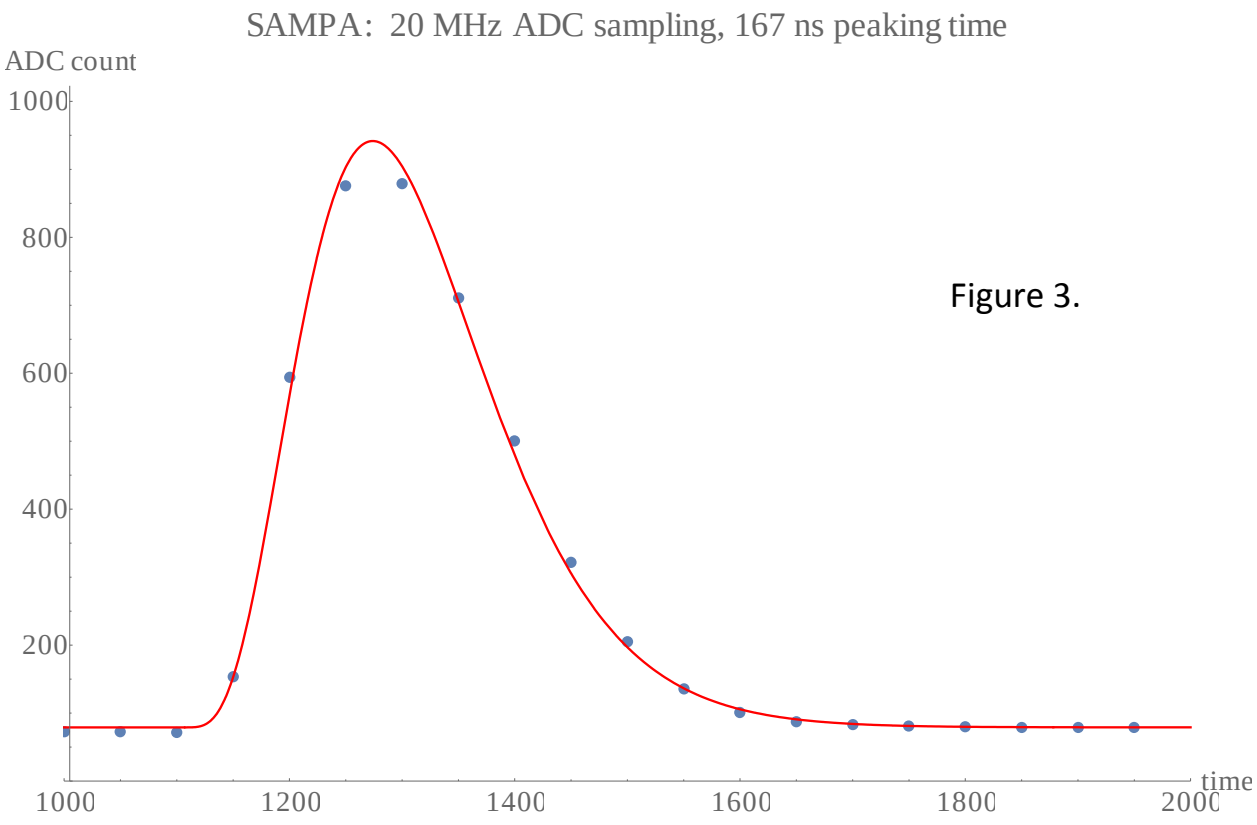
SAMPA: 20 MHz ADC sampling, 167 ns peaking time
ADC count
1000
800
600
400
200
1000
1200
1400
1600
1800
2000
time

Figure 3.