Candidate chips for TDIS RTPC

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Not that many options available

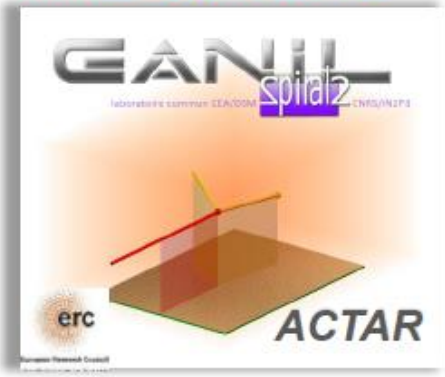
University of Virginia

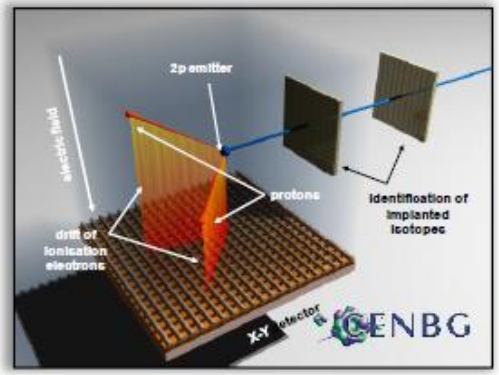
THE GET PROJECT: GENERAL ELECTRONICS FOR TPC'S

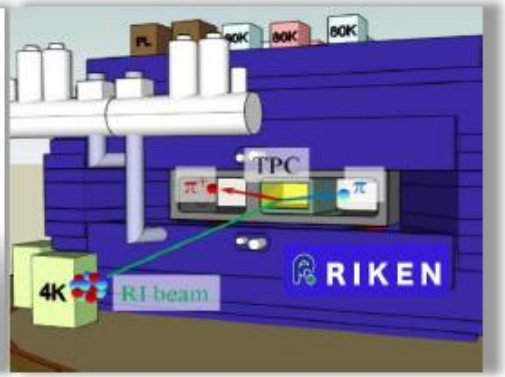
Background

- Following T2K developments, several laboratories involved in nuclear physics, CENBG (Bordeaux), IRFU (Saclay), GANIL (Caen) in France, MSU (United States) and later RIKEN (Japan) decided to join their efforts in the GET project to develop a new and generic readout system for TPC's and active target TPC's
- Funding received from the French National Research Agency (ANR) in France and NSF in USA
- Project started in 2010 and successfully completed in 2014

Initial applications







ACTAR TPC

- Micromegas or GEM
- ~16,000 channels

CENBG TPC

- GEM ampli.
- ~16,000 channels

AT TPC

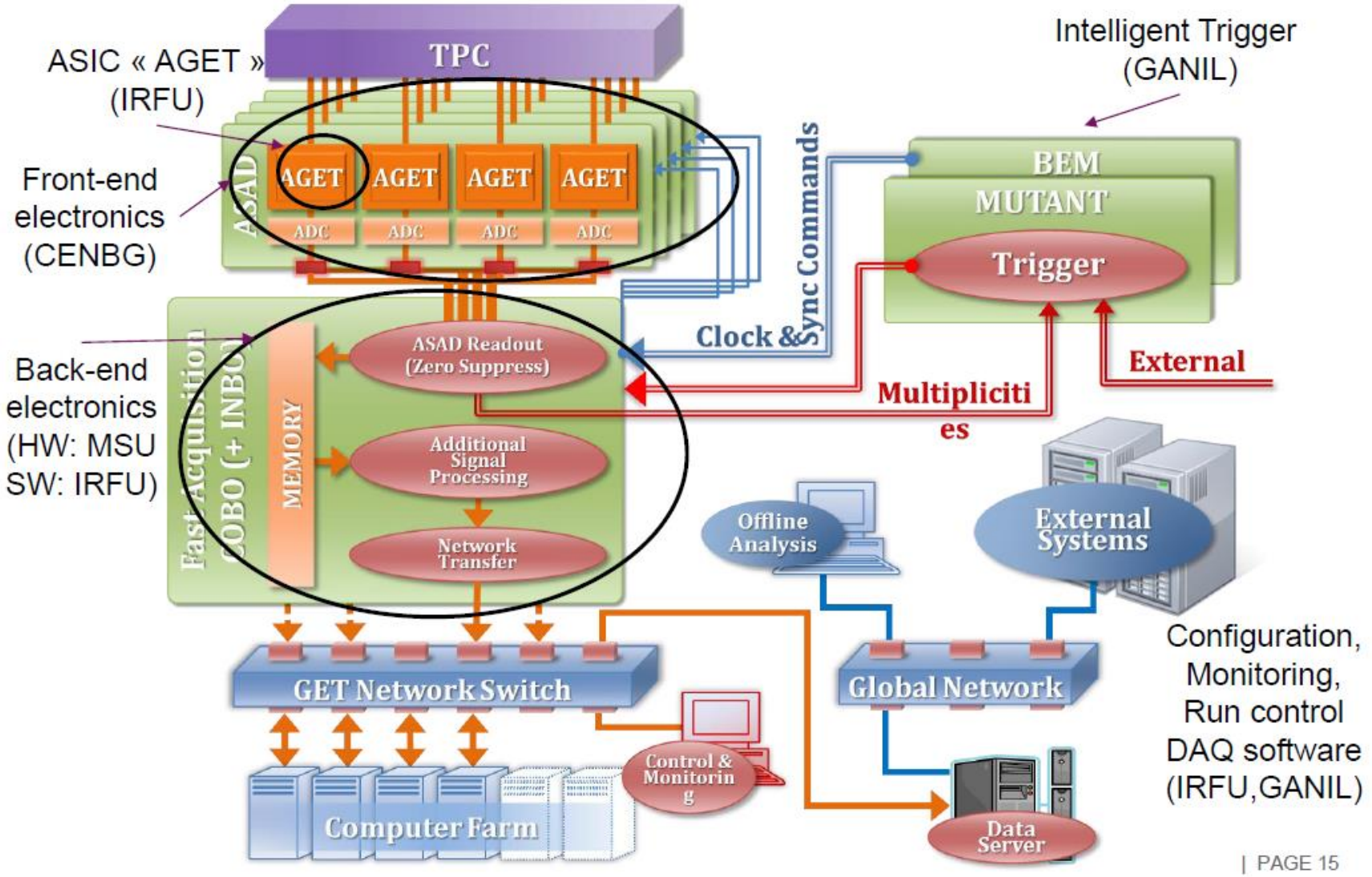
- Micromegas ampli.
- ~10,000 channels

SPIRIT TPC

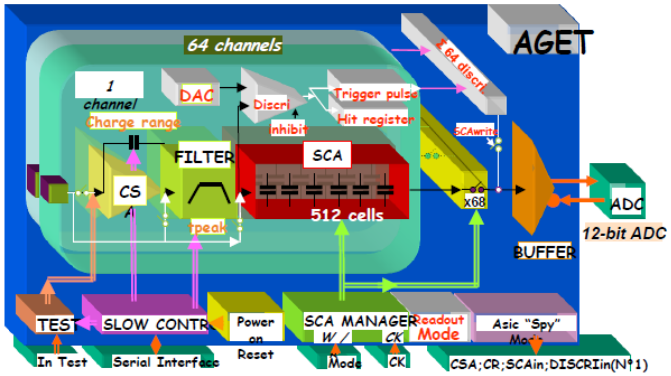
- Wire amplification
- ~12,000 channels

UNIVERSITY of VIRGINIA

ARCHITECTURE OF THE GET SYSTEM



AGET Chip

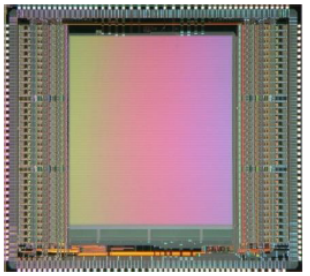


Specifications

Parameter	Value
Polarity of detector signal	Negative or Positive – Selectable by register programming
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2 x 256 cells
Sampling Frequency	1 MHz to 100 MHz
Multiplicity	
Multiplicity signal	Analog "OR" of 64 discriminator outputs
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC [(3-bit + polarity bit) common DAC + 4-bit DAC/channel]
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit, selected or all
SCA Readout mode	1 to 512 cells
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64(68) channels; 1 internal test capacitor per channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel @ 3.3V

Design Facts

- Technology: AMS CMOS 0,35 µm
- Surface: 8,5 x 7,6 mm²
- 700,000 transistors
- Package: LQFP 160 (28 x 28 x 1,4 mm)
- Production volume (up to 2014): 3200 chips



- The characteristics of the chip similar to DREAM chip
  - Not clear if DREAM is just an upgrade of AGET
- Plans to upgrade AGET and made it rad hard
- Had a discussion with F. Sabatie last week at JLab
  - Ask for requirements of RTPC to see what is the best chip option

VMM3

- Would VMM not be a good option
  - Signal peak ADC
  - Signal peak time measurement

VMM2 - Second ASIC prototype in 2014 (digital)

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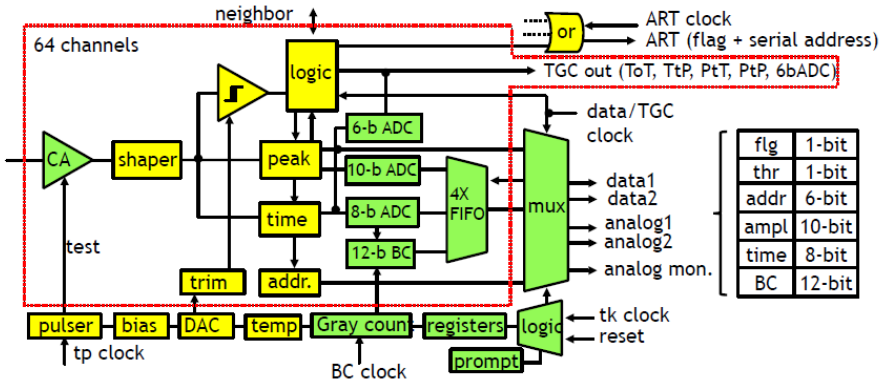

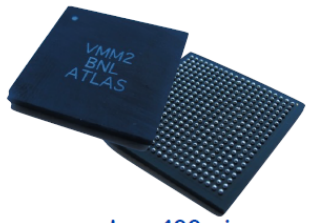

custom 400-pin
21 x 21 mm² BGA
1mm pitch

- All the bugs of VMM1 fixed plus additional functionality
- New Configuration logic registers: 80-bit + 24-bit / channel (1616bits)
- Charge amplifier: input transistor: PMOS 180 nm x 20 mm, 2 mA, adjustable gain 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)
- Peak detector, measurement of the peak amplitude - ADC with current-mode domino architecture 10-bit , 200 ns , sub-mW, for peak amplitude conversion, adjustable conversion time and offset + 6-bit ADC with 25ns conversion time
- Time detector: sub-ns resolution measurement of peak time, 8-bit , 100 ns , same as the 10bit architecture - 12-bit timestamp: - from shared 12-bit Gray-code counter, external BC clock - Complete timing information of 20-bit
- ART: serial output of a flag+ address with a clock reception
- Logic: direct digital output per channel with additional outputs (ToT, TtP, PtT, PtP)
- 4-deep FIFO: threshold-crossing indicator, 10-bit ADC, 8-bit ADC, 12-bit BC
- Readout: 38bit event continuous self-reset operation fully digital continuous up to 200 MHz (additional to the 2 phase analog mode)
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

BROOKHAVEN NATIONAL LABORATORY George Iakovidis - MPGD 2015 15/10/2015