# Streaming Readout Test Stand Proposal

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March 28, 2018

This document outlines the assembly and estimates the cost of a small scale streaming data acquisition system based on the SAMPA front end ASIC (**1,2**). The SAMPA chip was designed for the upgrade of the ALICE TPC and muon chamber detectors at CERN. It is unique in that it can operate in both streaming and triggered modes.

The primary goal of the test stand is to determine if the SAMPA chip is appropriate for use in the TDIS TPC and other detector systems at JLab. To achieve this goal we should:

- understand the SAMPA front end response to detector signals
- learn how to utilize the complex SAMPA DSP functionality to reduce data volume
- deal with a continuous readout data stream and link it with triggered data streams from other sources

The last point goes beyond the SAMPA chip. Continuous readout systems are expected to be used in future experiments at JLab, the EIC, and elsewhere.

The ideal test stand would have the following features:

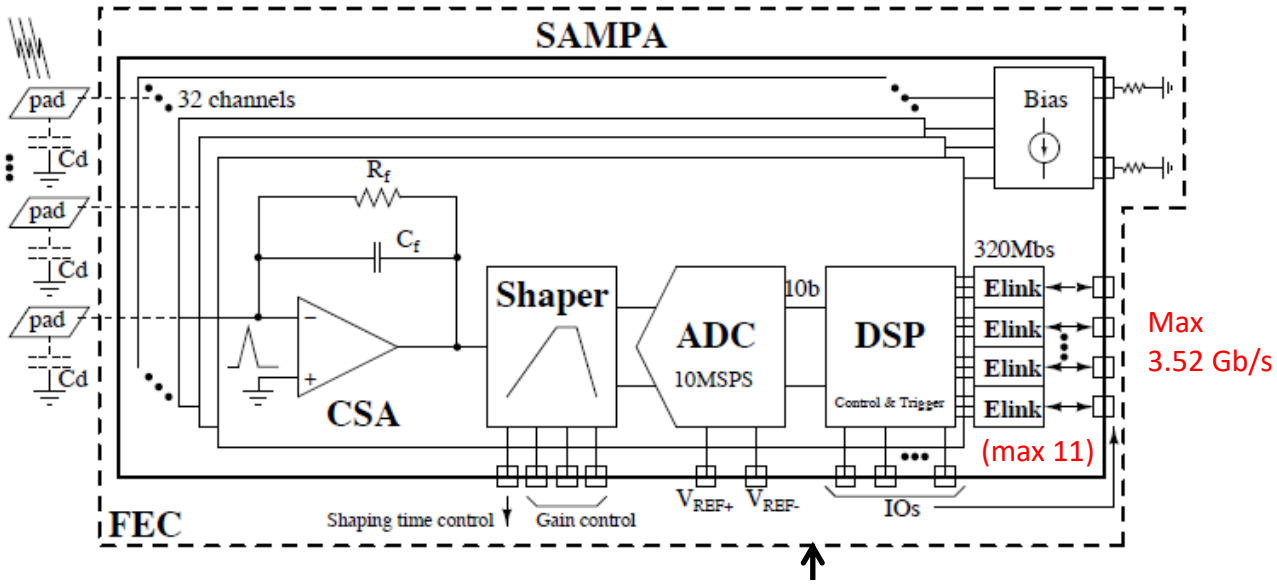
- a mechanism to pulse the inputs in a controlled fashion to study the effects of pileup and high rates on the SAMPA chip
- can connect to an existing detector (e.g. prototype GEM detector at JLab)
- supports enough channels so that common mode effects can be observed and strategies to handle them in the SAMPA chip can be explored
- can operate in a high radiation environment (hall or test beam)
- easily expandable for larger detector tests
- handles high data rates that are expected in experiments
- has an architecture that can be used for the final detector

We propose building a test stand from the actual components used in the ALICE data acquisition upgrade. Such a system has all the features of the ideal test stand. The components that are close to the detector are radiation tolerant. High data rates can be handled. The system is by design scalable. The elegant data transport architecture is a viable candidate for a final solution at JLab.

The idea also has many practical advantages. The SAMPA chip is an extremely complex mixed-signal ASIC. Designing a circuit board that supports this chip is a difficult task (e.g. digital noise coupling to analog front end, crosstalk). Experience (ALICE) shows that several iterations of the PCB are required to meet the design goals. Principals at ALICE have also agreed to share with us all of their development work on the system. This includes FPGA firmware and software tools that configure the SAMPA chip and manage data flow. System hardware components have been verified and tested together. Our development at JLab is reduced to coding (VHDL for data processing and formatting in the FPGAs, and software integration into CODA).

We are fortunate in our timing. The SAMPA ASIC, and ALICE upgrade data acquisition components are now entering their final production runs.

# SAMPA ASIC




Raw data rate (10MHz) = 32ch x 10b x 10M/s = 3.2Gb/s

(20MHz) = 6.4Gb/s

The SAMPA chip (**1,2**) provides 32 channels, each composed of an analog front-end part followed by an ADC. A common digital processor completes the chip.

A Charge Sensitive Amplifier (CSA), followed by two shapers and a non-inverting stage compose the SAMPA front end.

Each of the 32 channels includes its own 10-bit capacitive successive-approximation (SAR) ADC. The converter can operate at 10 or 20 MS/s.

After leaving the ADC, the data can follow two alternative paths: be processed by the DSP or be sent out in direct ADC mode.

In direct ADC mode the chip sends out the data directly, unprocessed, via ten 320 Mb/s eLinks. Since in direct ADC mode the data is not packaged with a header, the eleventh eLink is used to guarantee the synchronization of the data.

In order to process the data a set of 4 independently selectable and configurable filters are made available:

- Baseline Correction 1 (BC1), an infinite impulse response (IIR) filter to cope with slow baseline variations;

- Digital Shaper (DS), aimed at tail cancellation;
- Baseline Correction 2 (BC2), moving average filter aimed at tracking and removing fast variations in the baseline;
- Baseline Correction 3 (BC3), alternative filter, based on limited slope baseline tracking, to complement and/or substitute the functions of BC1 and BC2 with a more robust approach.

The digital section includes also blocks to implement zero suppression, data compression (Huffman coding), pre-sampling (in case of triggered mode), and data formatting.

## SAMPA Specifications

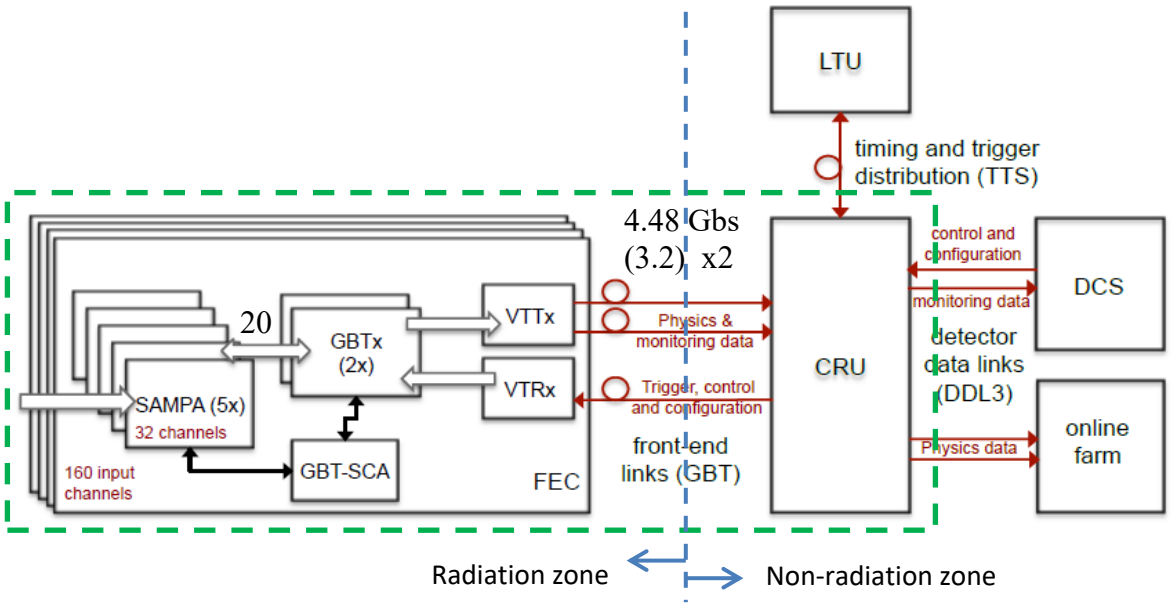
| **Specification** | **TPC** | **MCH** |
|---|---|---|
| Voltage supply | 1.25 V | 1.25 V |
| Polarity | Negative | Positive |
| Detector capacitance (Cd) | 18.5 pF | 40 pF - 80 pF |
| Peaking time (ts) | 160 ns | 300 ns |
| Shaping order | 4th | 4th |
| Equivalent Noise Charge (ENC) | < 600e@ts=160 ns* | < 950e @ Cd=40 pF*<br>< 1600e @ Cd=80 pF* |
| Linear Range | 100 fC or 67 fC | 500 fC |
| Sensitivity | 20 mV/fC or 30 mV/fC | 4 mV/fC |
| Non-Linearity (CSA + Shaper) | < 1% | < 1% |
| Crosstalk | < 0.3%@ts=160 ns | < 0.2%@ts=300 ns |
| ADC effective input range | 2 Vpp | 2 Vpp |
| ADC resolution | 10-bit | 10-bit |
| Sampling Frequency | 10 (20) Msamples/s | 10 Msamples/s |
| INL (ADC) | <0.65 LSB | <0.65 LSB |
| DNL (ADC) | <0.6 LSB | <0.6 LSB |
| ENOB (ADC)** | > 9.2-bit | > 9.2-bit |
| Power consumption (per channel)<br>CSA + Shaper + ADC | < 15 mW | < 15 mW |
| Channels per chip | 32 | 32 |

*$R_{esd}$ = 70Ω

** @ 0.5MHz, 10Msamples/s

# ALICE Upgrade Architecture

A Front End Card (FEC) mounted on the detector supports 5 SAMPA chips. Data from each SAMPA is streamed out onto four 320 Mb/s serial links (1.2 Gb/s total). A pair of Gigabit Transceivers (GBTx) multiplexes this data onto 2 high speed serial links (4.8 Gb/s each); these are driven off the board by fiber optic components. Forward error correction is applied by the GBTx chips, yielding a data payload of 6.4 Gb/s from the FEC. Data from multiple FECs is collected by the Common Readout Unit (CRU). The CRU and host PC process this data and send it by standard high speed networks (40 Gb/s Ethernet) to higher level computing systems. (Ref. **2**)



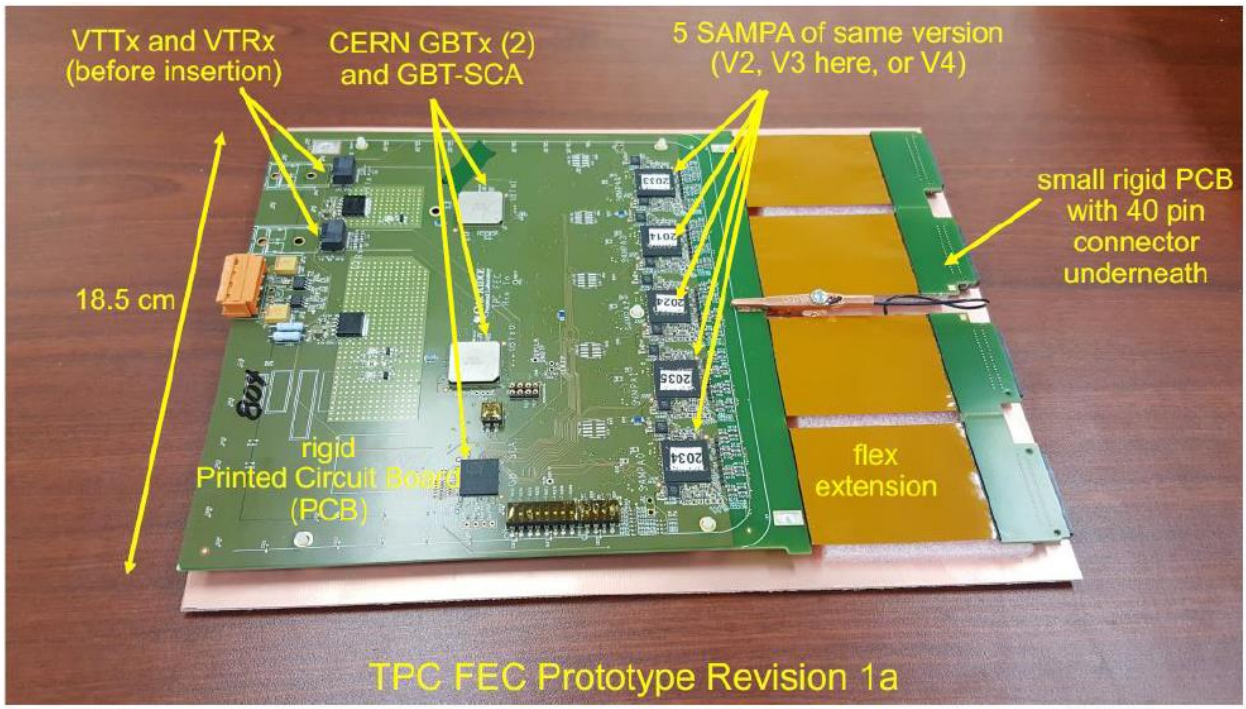

FEC – Front End Card - TPC (160 ch / FEC)
CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU
DCS – Detector Control System
LTU – Local Trigger Unit

CERN Custom ICs (radiation tolerant)

GBTx – Giga-Bit Transceiver (4.8 Gb/s)
GBT-SCA – Slow Controls Adaptor
VTTx – Versatile link fiber optic transmitter (x2)
VTRx – Versatile link fiber optic transceiver

# ALICE TPC Upgrade Front End Card

We will duplicate this card designed by Oak Ridge National Laboratory (ORNL). A custom flex circuit or cable assembly will map the input connectors (right side) to prototype GEM detectors at JLab.



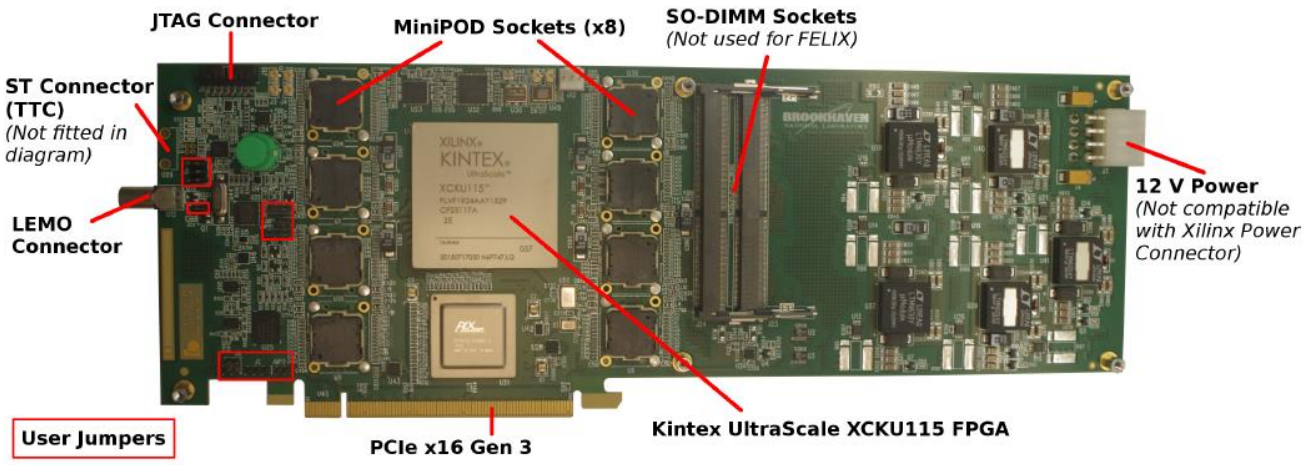

Final production version (ORNL)

# Common Readout Unit (CRU)

The CRU is the interface between the on-detector systems, the online computing system, and the Central Trigger Processor. It multiplexes data from several front-end links into higher speed data links. The CRU is built around a high-performance FPGA that can do sophisticated processing of the data. Trigger, control, and configuration data is sent to front end components by the CRU. It is implemented as PCIe card (Gen 3, x16), and is capable of sustained PCIe transfers at 100 Gb/s.

Because of the high demand of the ALICE CRU within the ALICE collaboration, we will instead use the ATLAS version (BNL-711) of the CRU in our test stand. (Ref. **3**)

BNL-711 V1.5



# Plan of Action

While we can simply purchase the CRU from the ATLAS development team at BNL, the FEC presents a greater challenge. The FEC is designed at Oak Ridge National Laboratory (ORNL) and uses custom ASICs from Brazil (SAMPA) and Europe (GBTx, GBT-SCA, VTRx, VTTx). Due to the different funding streams, purchasing an assembled FEC from ORNL is not possible. An alternative plan is to buy the components and the circuit board and have it assembled. The low risk and economical solution is to buy the circuit board from the vendor that is producing them now for ORNL, and have it assembled by the same assembly house used by ORNL. The NRE and setup costs would be greatly reduced in this case. Unfortunately, ORNL did not want to share their vendor information with us (no reason given). However, they have supplied us with all the manufacturing files and details necessary for us to duplicate the FEC. ORNL has also agreed to let us use their FEC test apparatus to confirm that the FECs we produce are working correctly before we install them in our system.

We plan to initially construct **5 FECs**. This represents **800 input channels** (160 ch/FEC). One CRU will be purchased. A single CRU can support 12 FECs (1920 ch/CRU). One PC platform will be purchased – two CRUs can be supported in it (3840 ch/PC). This illustrates the scalability of the system.

***** Quotations have been requested from three vendors for the production of the FECs. As of now (3/28/18) only one vendor has responded. We believe this quotation to be excessively high, but we will use it in the cost of the system until the other responses have been received. *****

All other costs listed are considered firm.

# Test Stand Cost

**PC** – Dell 7920 Dual Processor (Silver, 6x8GB) **$4,500**

**Ethernet Adapter** - Mellanox MCX4131A-BCAT ConnectX-4 Lx EN Network Interface Card 40GbE Single-Port QSFP28 PCIe3.0 x8 **$400**

**Optical Transceiver** - Mellanox MC2210411-SR4L Optical Transceiver 40Gb/s QSFP MPO 850nm up to 30m **$155**

**Power Supply** – Keysight E3633A 200W (0 - 8V, 20A) ($1519 x 2) **$3,038**

**Common Readout Unit** – ATLAS BNL-711 (24 links) **$10,600**

**Fiber Optic Cable Assembly** – FEC → CRU (5m) **$200**

**Custom Integrated Circuits (6 FEC)**

| | | | |
|---|---|---|---|
| SAMPA | $40 x 30 | = $1200 | |
| GBTx | $50 x 12 | = $600 | |
| GBT-SCA | $35 x 6 | = $210 | |
| VTRx | $200 x 6 | = $1200 | |
| VTTx | $150 x 6 | = $900 | **$4,110** |

**Front End Card** – (**$3114** x 5) **$15,570**

**Total** **$38,573**

# References


(1) http://iopscience.iop.org/article/10.1088/1748-0221/12/04/C04008/pdf

(2) https://cds.cern.ch/record/1622286/files/ALICE-TDR-016.pdf

(3) http://inspirehep.net/record/1505333/files/10.1088_1748-0221_11_12_C12023.pdf