# SuperBigBite DAQ update

Bryan Moffit
Jefferson Lab

SBS DOE Review – November 2015

# Outline

- SBS requirements
  - *Data Event Flow*
- Fastbus Readout
  - *Event Switching*
- FADC HCAL readout
- GEM readout
- Timeline
- Manpower

Jefferson Lab

# $G_E^p$ DAQ requirements

- Focal Plane Polarimeter
  - Front tracker
  - Back tracker GEM 128 K channels
  - 288 channels HCAL on FADC ( 10 samples )

- Electron detector
  - 1800 channels ECAL
  - CDet 2152 Channels ( TDC )

# $G_E^p$ event size (after deconvolution)

| Detector | Channels | Single rate Hz | Occupancy 75 ns in % | Channels firing | Event size (bytes) | Data rate 5 KHz MB/s |
|---|---|---|---|---|---|---|
| Front tracker | 41,000 | 3.3e9 | 18.1 | 7430 | 136,000 | 90 |
| Back tracker | 112,640 | 3.36e9 | 22.4 | 12600 | 230,000 | 150 |
| HCal | 288 | _ | 100 | 288 | 7,200 | 36 |
| ECAL | 1800 + 225 | _ | 100 | 2025 | 8,100 | 45 |
| CDET | 2152 | _ | 10 | 216 | 864 | 4.3 |
| Total | | | | | | 325.3 MB/s |

Includes geometrical matching

HCAL and ECAL occupancies need to be evaluated : using 100 % for now

# $G_E^n, G_M^n$ DAQ requirements

- ## Bigbite
  - GEM 128 K channels
  - Shower 189 blocks (ADC)
  - Preshower 54 blocks (ADC)
  - Scintillator 180 bars 360 PMTs ( ADC/TDC)
  - Cerenkov 550 PMTs (TDC)

- ## Neutron detector
  - 288 channels HCAL ( FADC + high res TDC )
  - CDet 2152 Channels ( TDC )

# $G_E^n, G_M^n$ event size (after deconvolution)

| Arm | Detector | Channels | Single rate Hz | Occupancy 75 ns in % | Channels firing | Event size (bytes) | Data rate 5 KHz MB/s |
|---|---|---|---|---|---|---|---|
| BigBite | GEM | 112,640 | 2.6e9 | 8.7 | 5248 | 62,976 | 300 |
| | Lead glass | 243 | _ | 100 | 243 | 1003 | 5 |
| | Scintillators | 360 | _ | 100 | 360 | 1485 | 7.4 |
| | Cerenkov | 550 | _ | 100 | 550 | 2269 | 11.34 |
| Neutron | HCal | 288 | _ | 100 | 288 | 7,200 | 36 |
| | HCAL time | 288 | _ | 100 | 288 | 1170 | 5.85 |
| | CDET | 2152 | _ | 10 | 216 | 864 | 4.3 |

**Total at 5 KHz 370 MB/s Max**

# Fastbus update

- Use new CODA 3.0 TI and TS
  - More flexibility in programming
  - Event blocking
  - Absolute timestamp for synchronization check
  - Trigger partitioning capability only use a subset of modules

- Asked for modified firmware to DAQ group in May 2015 ( William Gu and Bryan Moffit )

- Firmware being developed and tested

Jefferson Lab

# Fastbus update

- Have sufficient    TDCs,    ADCs,    crates,   SFI,    aux. cards
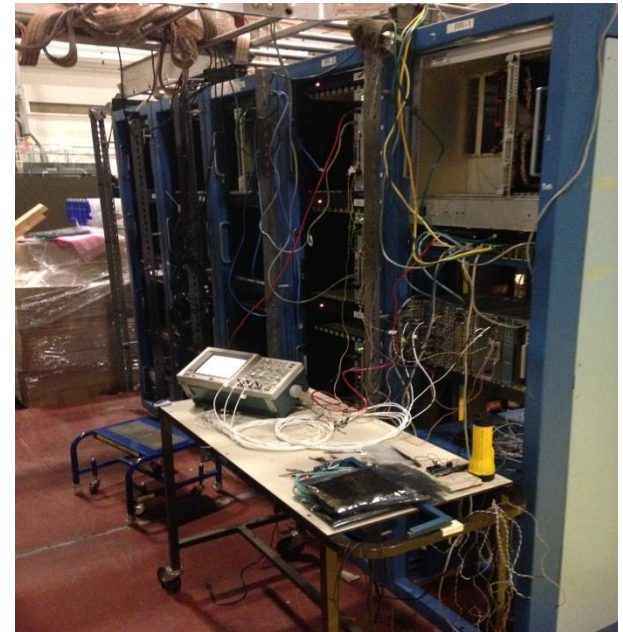
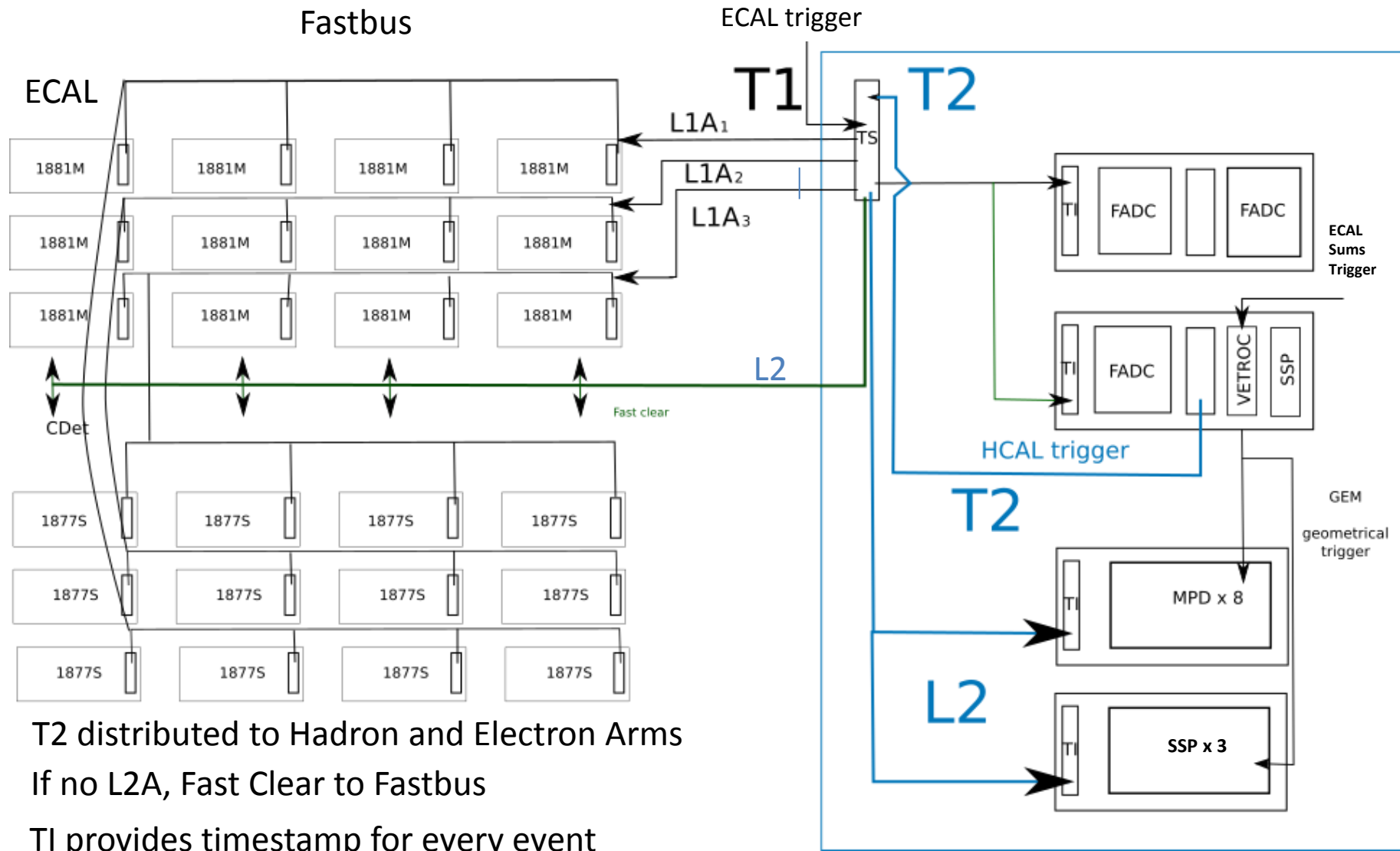| | TDCs | ADCs | crates | SFI | aux. cards |
|---|---|---|---|---|---|
| have | 236 | 113 | 30 | 21 | 15 (20 being made) |
| need | 124 | 94 | 21 | 21 | 30 |

- Making FB faster
  - sparsification – works
  - event blocking – works
  - event switching – being tested
  - merging with pipelining VME – to be tried

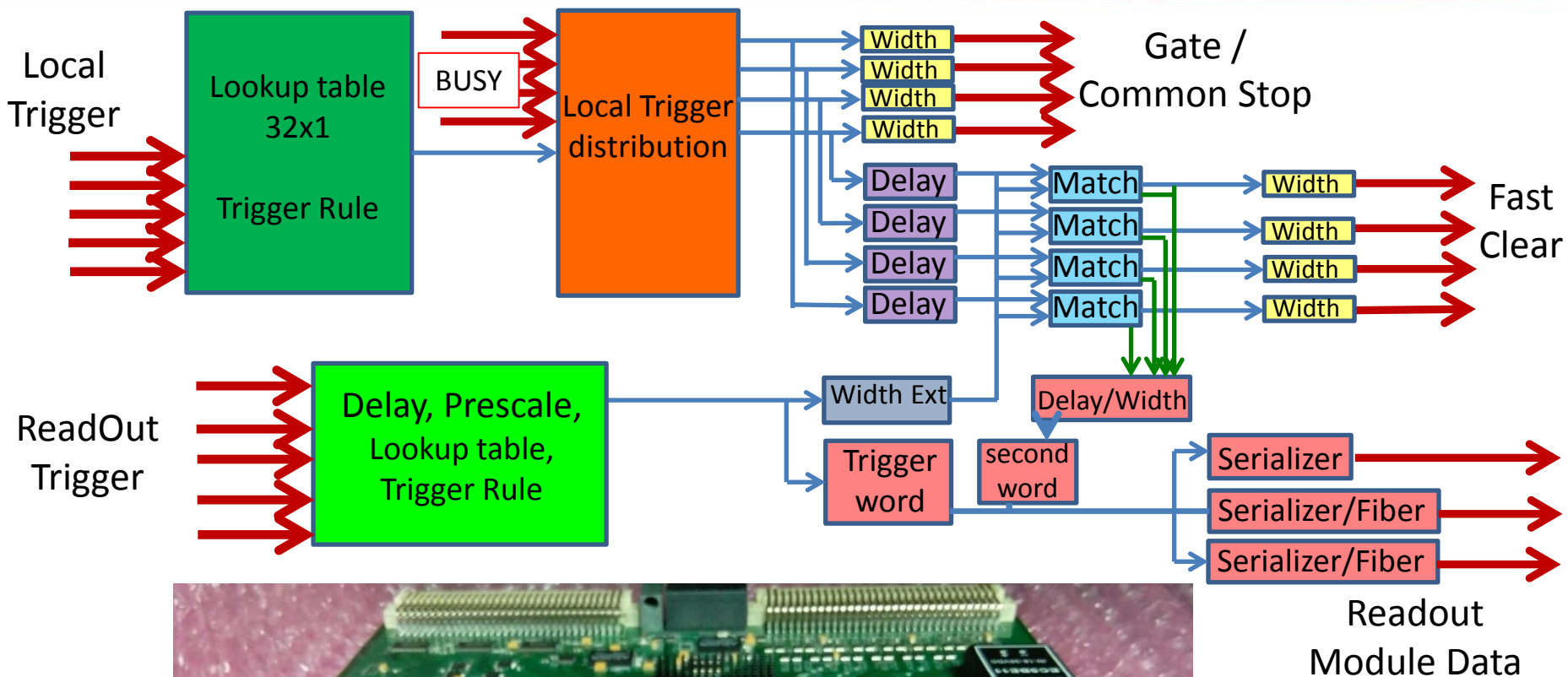- Three large Fastbus systems assembled in the test lab.

# $G_E^p$ DAQ Configuration / both arms



T2 distributed to Hadron and Electron Arms

If no L2A, Fast Clear to Fastbus

TI provides timestamp for every event

# HallA SBS Trigger block diagram

Local Trigger

**Lookup table 32x1**

**Trigger Rule**

BUSY

**Local Trigger distribution**

Width
Width
Width
Width

Gate / Common Stop

Delay → Match → Width → Fast Clear
Delay → Match → Width
Delay → Match → Width
Delay → Match → Width

ReadOut Trigger

**Delay, Prescale, Lookup table, Trigger Rule**

Width Ext

Delay/Width

Trigger word

second word

Serializer
Serializer/Fiber
Serializer/Fiber

Readout Module Data

# Single Crate vs. Trigger Switching

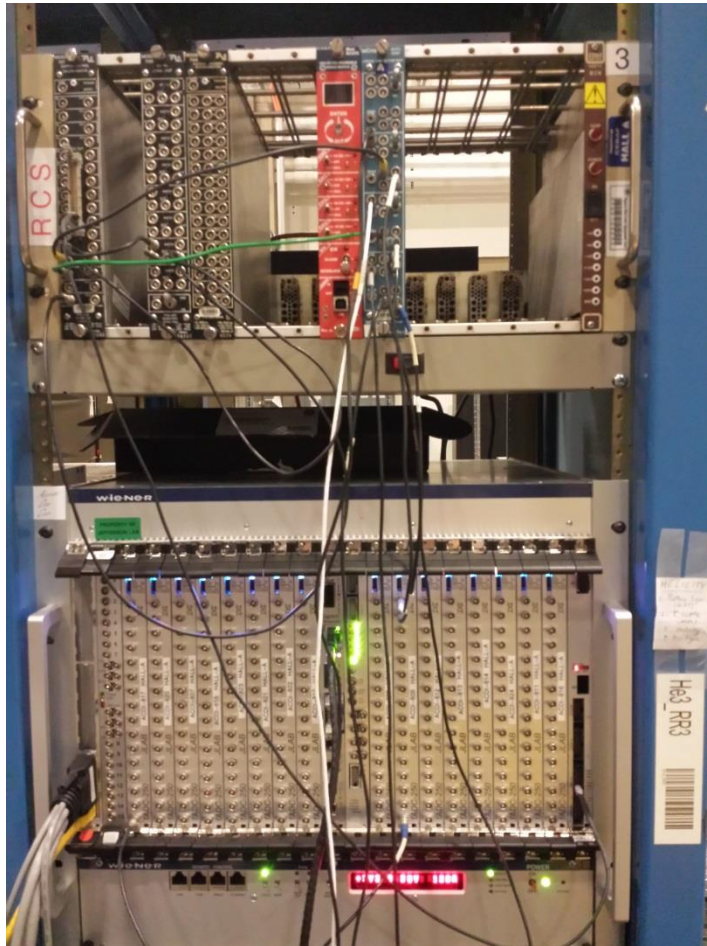Readout trigger rate ~ 5 kHz

Buffer Level = 4

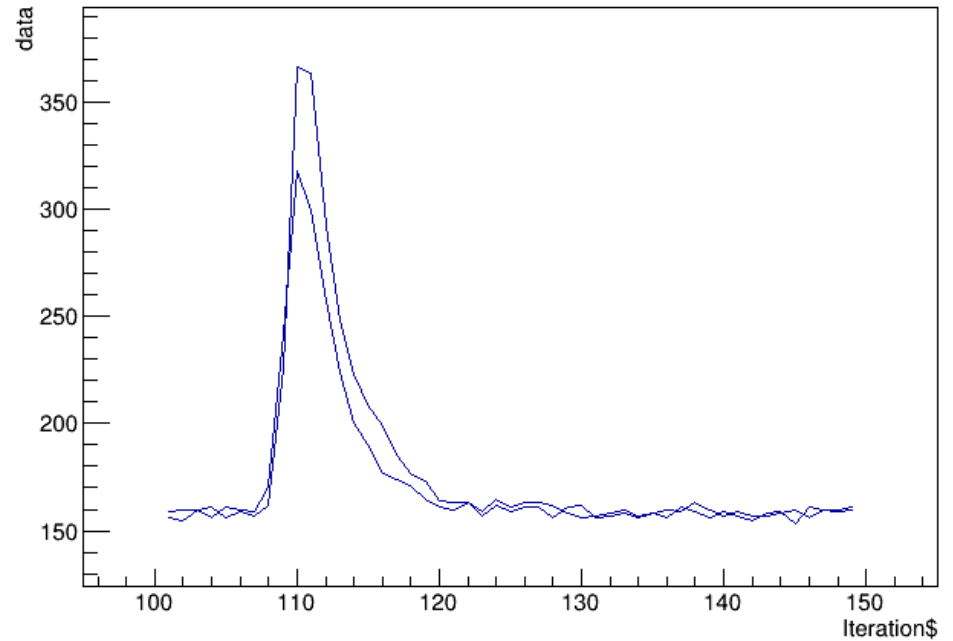8ADC - (reading pedestals on 6 channels in each ADC)
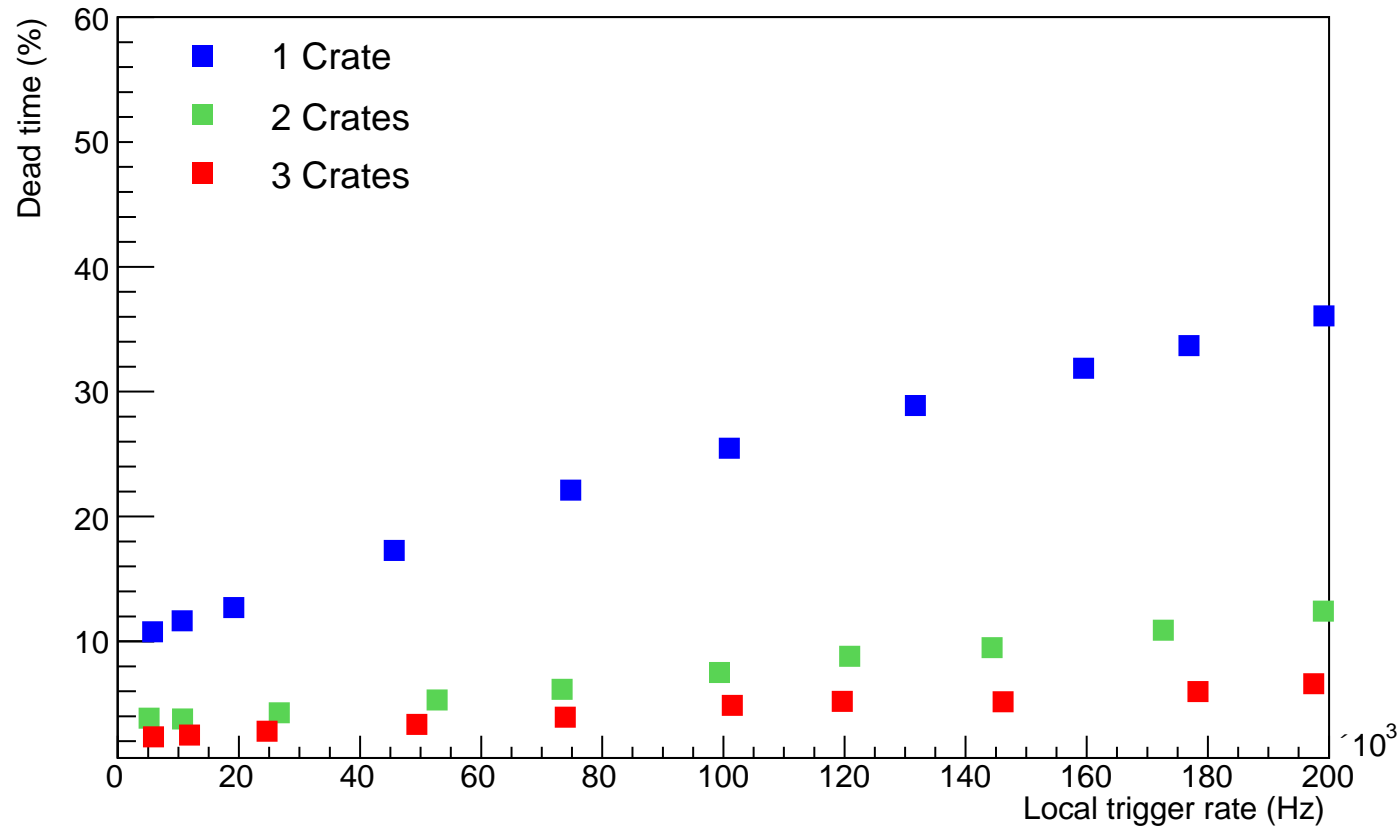
# HCAL

- All FADC 16 delivered
- 2 VXS crates delivered
- 2 Intel Concurrent CPU delivered

- Readout tested
- Development of trigger using HPS firmware and Global Trigger Processor (GTP)
- New VTP ordered

Jefferson Lab

# HCAL FADC electronics



data:Iteration$ {Iteration$<150&&Iteration$>100}

- Cosmics from calorimeter block
- Will test later with HCAL module

HCal Signals to
FADC inputs

Start Frame 32 ns

Drop
last 4 bits

17 bits Σ →  13 bits word
            +
            3 bits time in frame   →  16 bit per channel

17 bits Σ →  13 bits word
            +
            3 bits time in frame   →  16 bit per channel

17 bits Σ →  13 bits word
            +
            3 bits time in frame   →  16 bit per channel

17 bits Σ →  13 bits word
            +
            3 bits time in frame   →  16 bit per channel

FADC

do
for
all
16 FADC
channels

send 2 channels
to CTP
in one 32 bit
word
every 4 ns
@
8 Gbps

- 2 VME switched Serial (VXS) Crates
- JLAB FADC250, a 16-channel 12-bit FADC sampling at 250 MHz
  - 16 FADC in VXS Crate 1
  - 2 FADC in VXS Crate 2
  - If signal pass threshold
  - Integrates signal and subtracts pedestal
  - Sends time frame info
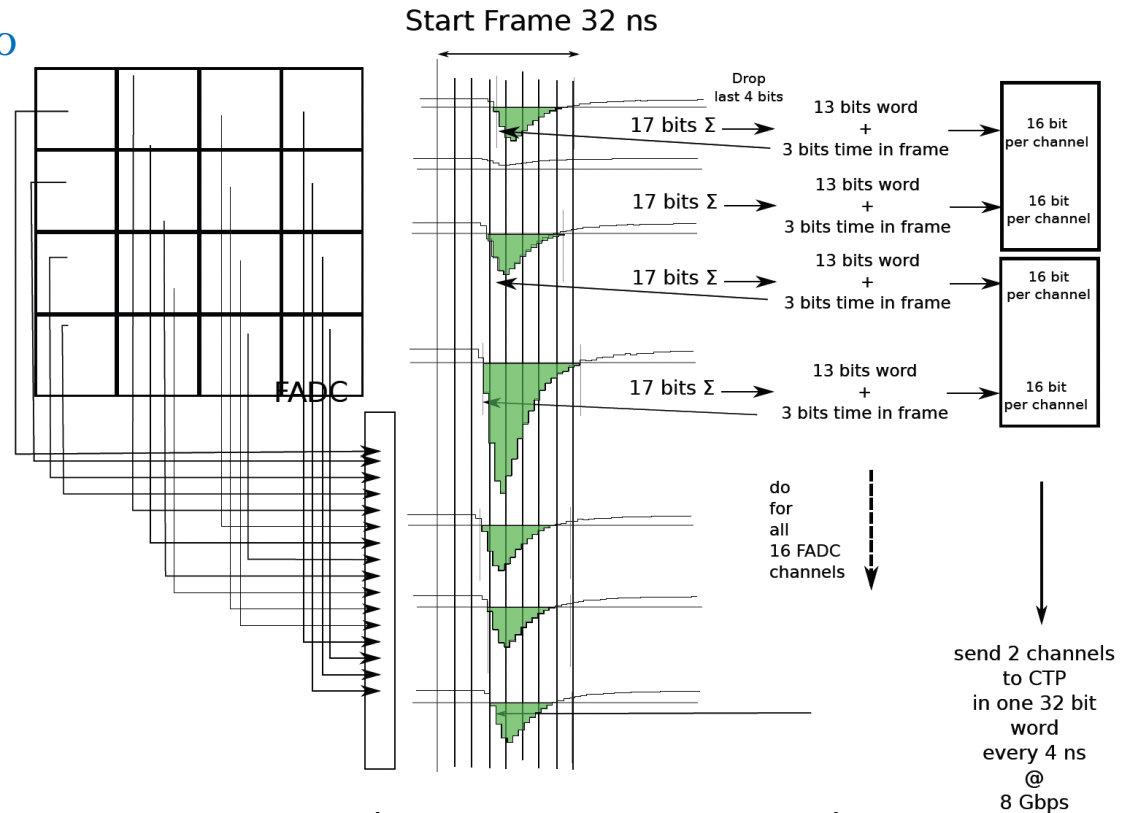
- VTP (Crate Trigger Processor)
  - Located in VXS crates
  - Collects integrated signal and timing from FADC channels
  - Sends data to the second VTP for clustering

# HCAL trigger development

- HPS firmware installed on FADC and GTP
- FADC readout tested with cosmics
- Testing triggering capability

- Need
  - implement decoder for analysis
  - Test using 2 crates and new VTP

Jefferson Lab

# GEM MPD readout

- INFN MPD used for several years using custom C++ package

- Package ported to intel CPU

- New C library written for easy integration into CODA

( Bryan Moffit, Evaristo Cisbani, Danning Di )

- CODA configuration running

- Debugging module initialization

JSA

Jefferson Lab

# GEM optical link readout

- Aurora protocol based
    - Implemented by Paolo Musico. To be tested.

- 2 Gbit optical link to SubSystem Processor (SSP) module
    - 250 MB/s per link

- Readout up to 32 MPD in parallel
    - 8 GB/s bandwidth compared to ~100 MB/s using VME

- SSP library
    - Readout routines – Completed.
    - MPD configuration routines – In progress

- Link from MPD to SSP module
    - Implemented by Ben Raydo. Works.

JSA

Jefferson Lab

# Timeline

| 4th quarter 2015 | 1st quarter 2016 | 2st quarter 2016 | Future |
|---|---|---|---|
| • Finish MPD CODA readout – debug<br>• Finish Fastbus Readout – debug<br><br>• Small scale setup<br>   • 200 KHz L1<br>   • 5 kHz coinc<br>   • Fastbus, MPD, and HCAL FADC<br><br>• Cdet Fastbus<br><br>• Analysis software : check synchronization<br><br>• Test MPD optical readout (SSP)<br><br>• HCAL trigger ordered | • Implement new HCAL Trigger module<br><br>• HCAL cosmics<br><br>• GEM cosmics with MPD<br><br>• Test GEM readout with optical link in high background at UVA<br><br>• Develop GEM analysis software | • GEM installed on BigBite for tritium experiment<br><br>• ECal cosmics<br><br>• DVCS experiment Parasitic test: Fastbus and FADC setup | • Tritium experiment Parasitic test: Fastbus and FADC setup |

# Manpower

- ## Fastbus
  - JLAB : Dasuni Adikaram, Mark Jones, Robert Michaels, Bryan Moffit, William Gu

- ## MPD
  - INFN : Evaristo Cisbani, Paolo Musico
  - UVA : Danning Di, Kondo Gnanvo, Nilanga Liyanage
  - JLAB : Ben Raydo, Bryan Moffit
  - Stony Brook : Seamus Riordan

- ## HCAL
  - JLAB : Alexandre Camsonne, Ben Raydo, Bryan Moffit

# Conclusion

- Fastbus event switching works well
  - Preliminary results show acceptable dead time in experiment conditions
  - Need to develop software and check synchronization

- HCAL:
  - FADC ready
  - trigger implemented and being tested

- MPD:
  - CODA readout implemented
  - Debugging of the software driver
  - Optical readout in progress

- Small scale test setup in a few weeks

JSA

Jefferson Lab