SAMPA chip
Outcome from meeting with developers (Sao Paulo – Brazil)

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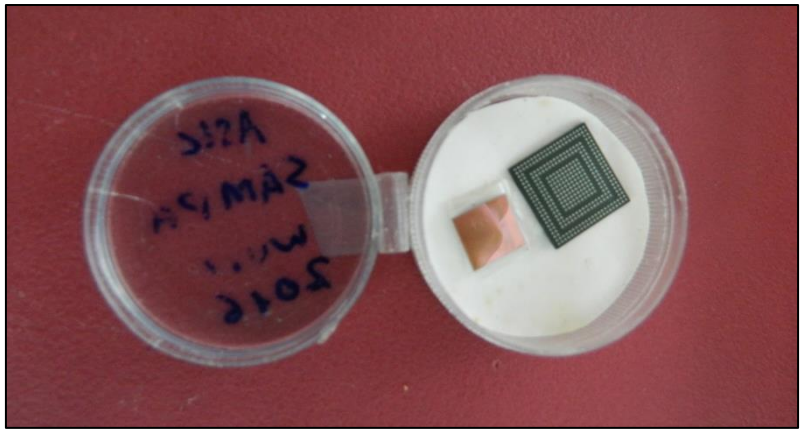
SAMPA chip

- Developed at the University of Sao Paulo (Brazil) for Alice (LHC) upgrade
- Continuous sampling, ideal for high rates TPCs (triggered or trigger-less readout)
- 32 channels per chip
- 160ns of sampling period (studying the possibility to produce 80ns)
- 10 bits ADC
- Base-line correction and zero suppression available



I was at University of Sao Paulo last month, and met professors of the group that developed the chip: Marcelo Munhoz and Wilhelmus Van Noije.

Thanks for the guidance by Ed Jastrzembski for that meeting!

SAMPA – next production schedule

- Feb/Mar of 2018:
  - Alice (LHC) + sPhenix (BNL) to place order for 80k chips
  - TDIS/JLab need 1000 chips
  - We could also enter in this order, to get the U$30/chip
  - Order would be delivered in Aug/Sep of 2018
  - Version 4 (160ns, higher charge rate)
  - We need to check if current specifications attend our requirements

- No other order planned at the moment

Important: are the current specifications of the chip suitable for our use (capacitance, input load limits, etc)? Or would we need development?

We got the manual of the board, I'll upload to our wiki.

SAMPA – other schedule possibilities

- Independent JLab order with manufacturer (Taiwan):
  - Ordering only 1k units would make chips expensive – need estimate
  - Might not be an interesting option

- Other possibility if we are not ready to place order now:
  - Production yield should be on the order of 80%
  - They are going to order counting on a yield of 70%, therefore they expect to have about 8000 spare chips at the end of 2018
  - JLab could get 1000 chips of these – can negotiate on how/when to pay

- Chips for our initial evaluation:
  - They can already provide us 25 chips for our initial tests – just checking their inventory for that
  - No cost for these test chips

Tests of the chips

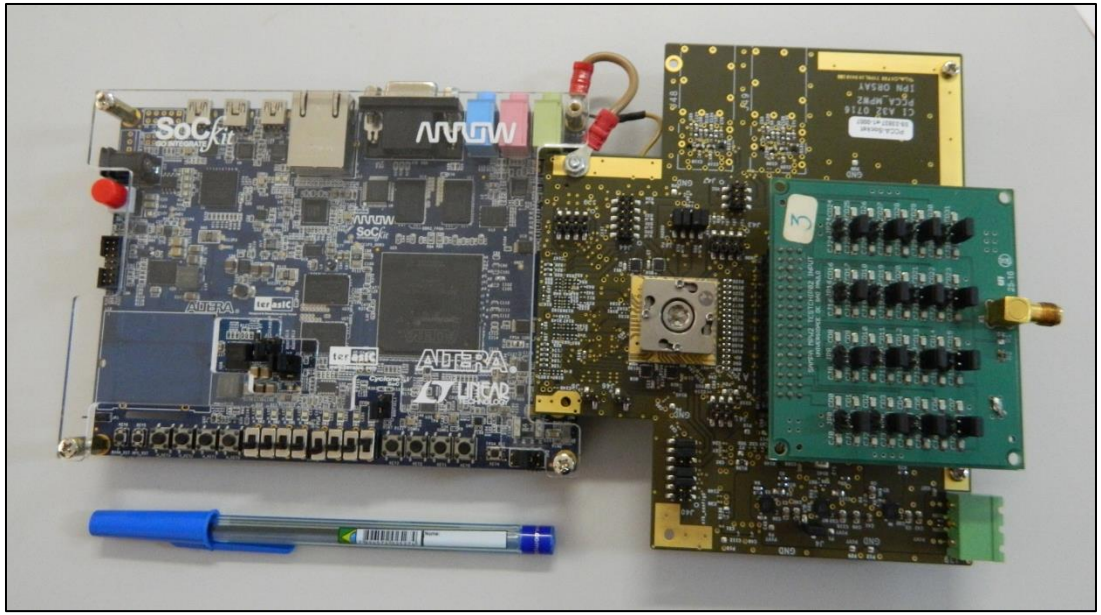
Chips are delivered from manufacturer with no tests

Need to run tests for chip selection

- Lund (UK):
  - Automated tests for large amounts
  - Highly recommended since they have a careful procedure defined
  - Estimated cost of U$10/chip – need to double check this
  - Contact: Anders Oskarsson (anders.oskarsson@hep.lu.se) – also the contact person to get sockets to connect chip to board
  - USP can make the bridge of Lund with JLab when we are ready

Tests of the chips

- FPGA based board for individual tests:
  - Spring based socket – no soldering required
  - Board Terasic DEIO (for interface of FPGA with computer) not fabricated anymore – we would need to develop this interface
  - Tests with pulses of charge possible
  - Alex Kludge (alexander.kluge@cern.ch) – ALICE electronics coordinator. He can provide us with the name of company that produced this board.



Possible future upgrades

- sPHENIX pushing to develop next SAMPA generation with 80ns of sampling:
  - Do we need such feature?
  - Team at University of Sao Paulo working on that is small – they are studying the possibilities to start that development project. They want to know if we would have interest, perhaps even for future projects.
  - Around 2 years for development – chip would be available at end of 2019