Effect of Input Capacitance on Noise for the SAMPA ASIC

Abigail Hellman
University of Virginia
8/12/19

Abstract

The SAMPA ASIC [1] designed for the upgrade of the ALICE experiment at the LHC is under consideration by experiments at Jefferson Lab for the readout of various GEM detector systems. General calculations of the noise for SAMPA type front-end architectures show that for sufficiently high input capacitance, noise grows linearly with capacitance [2]. In this study we will quantify this effect for the SAMPA chip.

Introduction

A block diagram of the SAMPA ASIC is shown in **Figure 1**. A Charge Sensitive Amplifier (CSA), followed by two shapers and a non-inverting stage compose the analog front end. The shaped signal with a peaking time of 160 ns is digitized by a 10-bit ADC that can be operated at up to 20 MSPS. After leaving the ADC the digitized data can follow two alternative paths: be processed by the DSP or be sent out in direct ADC mode (DAS). The DSP can be utilized to perform baseline corrections and data compression (zero suppression, Huffman coding) before sending the processed data off chip in multiple serial data streams. In contrast, direct ADC mode sends out the unprocessed ADC data directly via ten serial data links. The design of the Front-End Card (FEC) that supports the SAMPA chips limits the sampling rate in DAS mode to 5 MSPS.

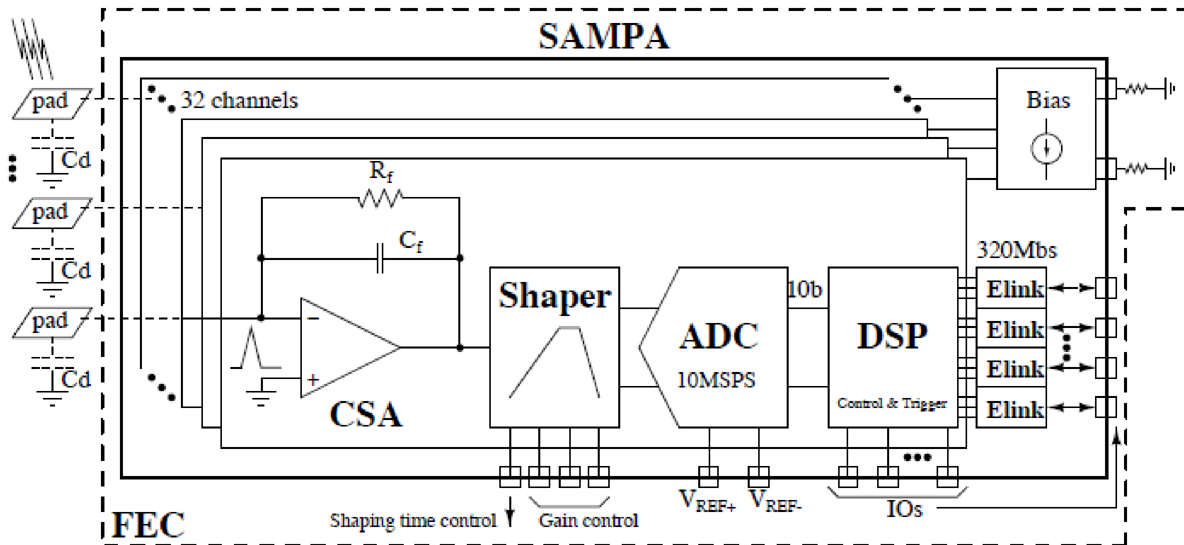


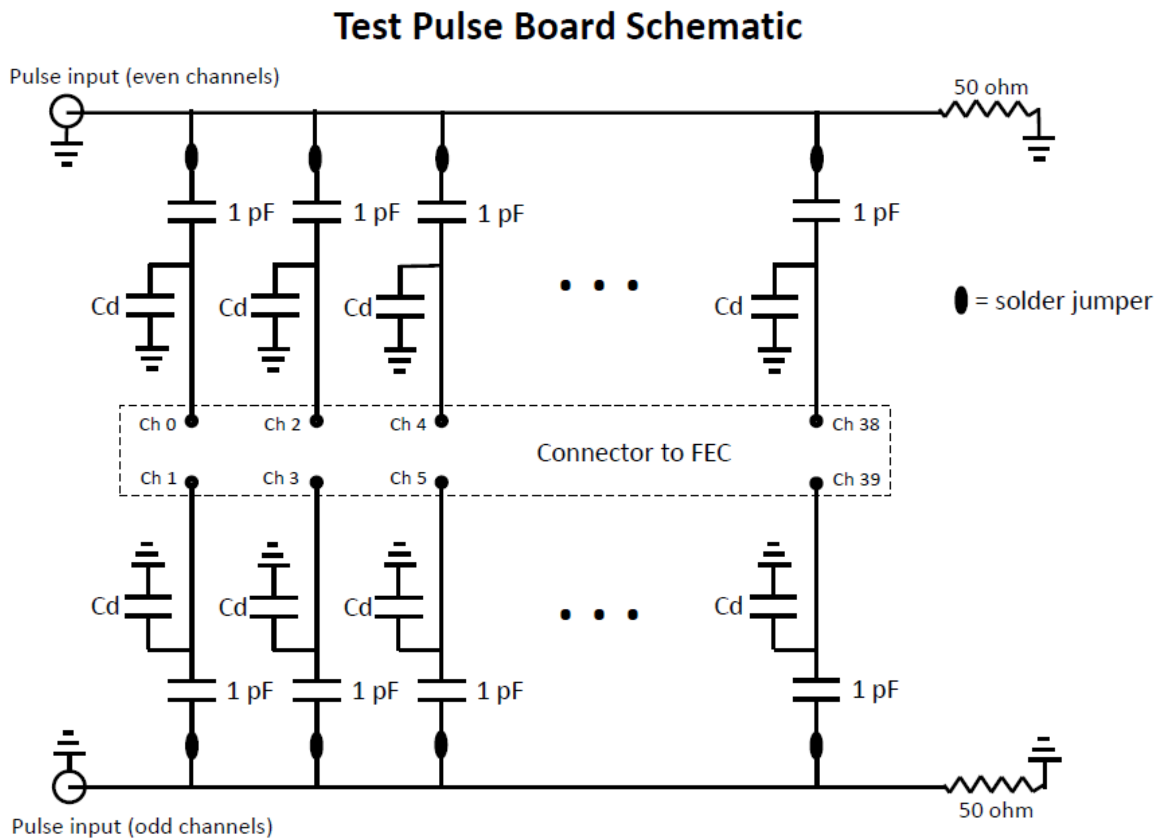
Figure 1.

Data collected for the noise studies reported here were obtained with the SAMPA in DAS mode.

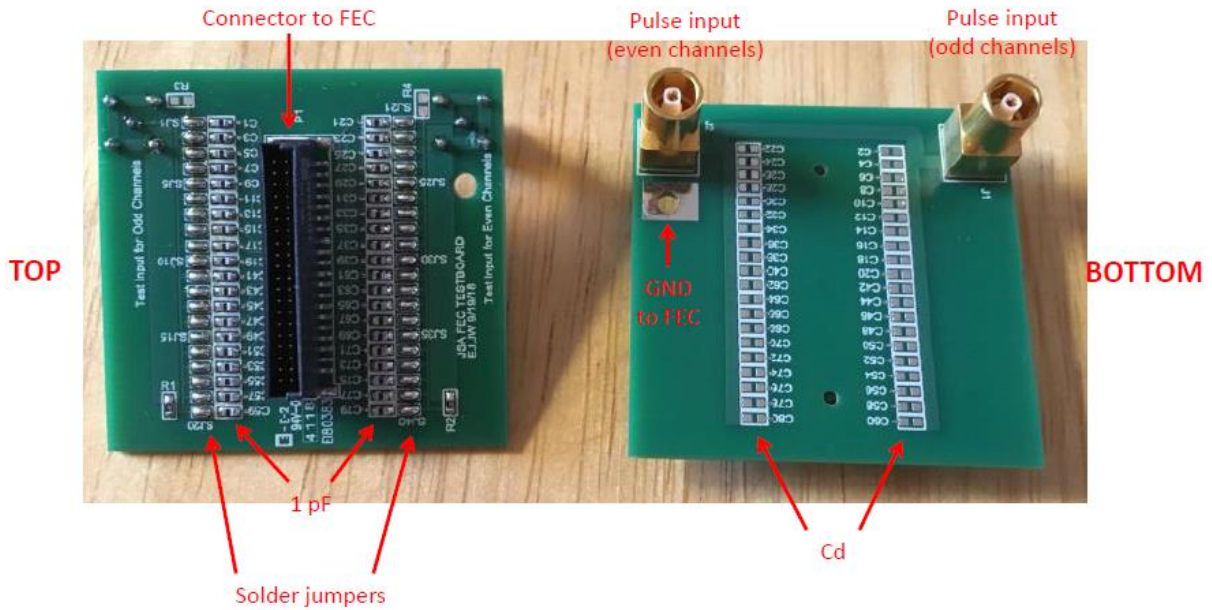
Method

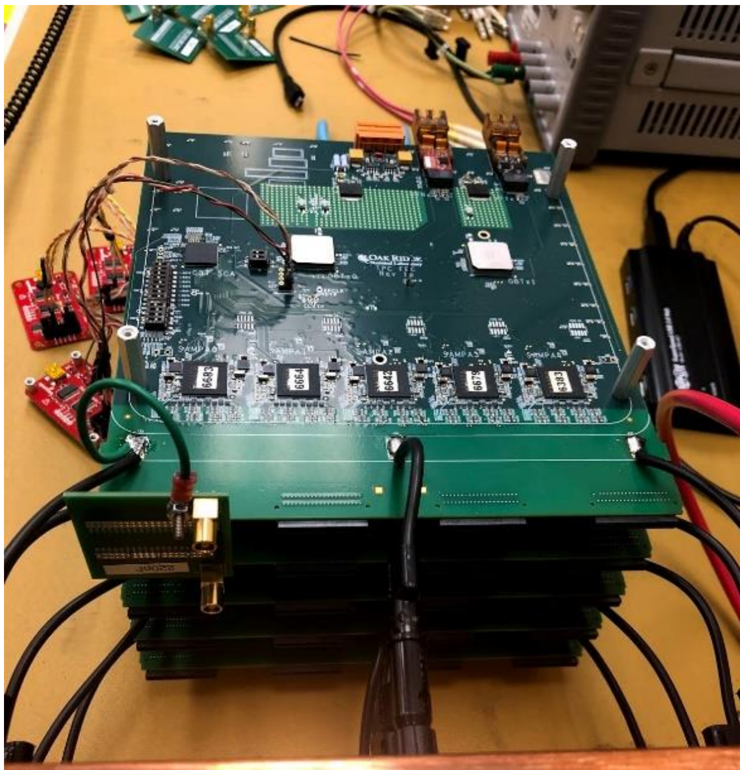
To study the SAMPA chip performance under controlled conditions a small and inexpensive Test Pulse Card was constructed. It enables the injection of a known charge Q into SAMPA inputs (via a 1 pF capacitor). It also allows the simulation of various detector capacitances by mounting discrete capacitors C_d on the board. The Test Card plugs directly into an FEC connector; each FEC connector handles 40 channels.

The Test Card schematic and an image of the card are shown below. Additional images of a Test Card mounted on an FEC follow.

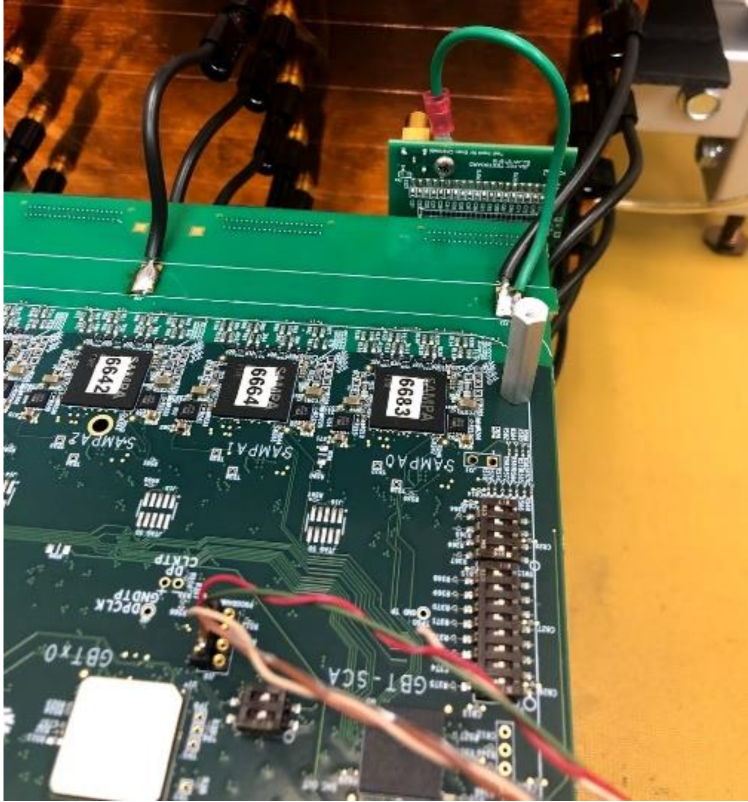


Test Pulse PCB





Mounted Test Card from the backside, showing the stack of 5 FECs. The Test Card is plugged directly into one of the connectors that would normally be cabled to the GEM detector. The capacitance C_d of the Test Card simulates the capacitance of the GEM detector and cable assembly.



Mounted Test Card shown from the front, plugged into the first first connector (40 channels) of the top FEC. The green wire connects the ground of the Test Card with the ground of the FEC.

Noise is manifested as fluctuations in the ADC sample values of the baseline (pedestal) when no charge is being injected. The measured standard deviation (sigma) of these sample values is the metric used to characterize the noise.

A total of six Test Cards were used in the study. The first card had no added capacitance ($C_d = 0$). Each of the remaining cards had a specific capacitance value assigned to it (Cd = 39, 75, 100, 150, 220 pF). To account for channel-to-channel variations, 5 channels of a given card had identical capacitors installed. The selected channels were the same for all 5 cards. To account for possible Test Card-to-Test Card variations, analysis of 4 channels not having additional capacitance was also performed.

Approximately 6250 ADC samples per channel were acquired in each test configuration.

Results

Graph 1

The highest and lowest standard deviation for each capacitance amidst the five channels they were applied to, along with a control value plotted at the average zero capacitance value. (Note: The control value is the value from the card with no capacitors.) The linear dependence of noise on detector capacitance is clearly exhibited.

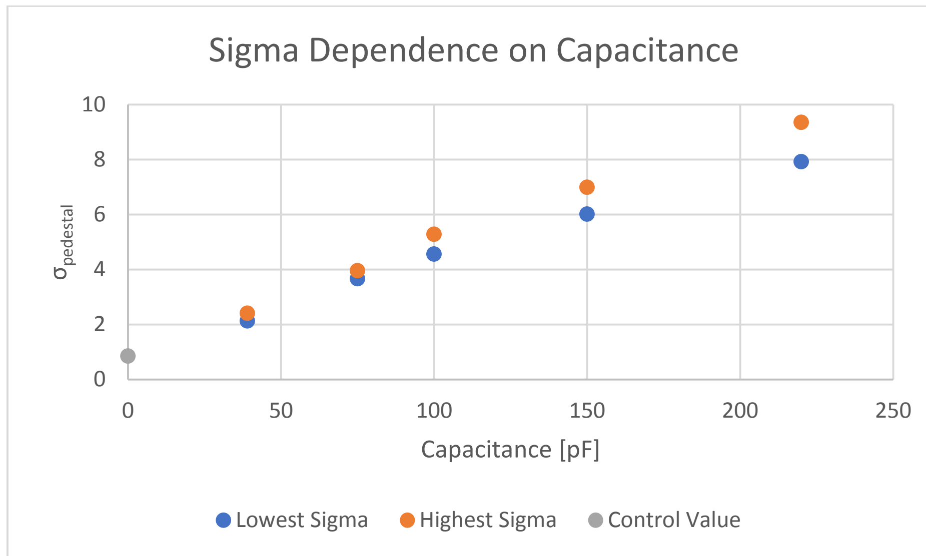


Table 1

Each standard deviation value found on the 5 channels the capacitors were attached to and the average value for each capacitance.

Cap [pF]	Ch. 1	Ch. 11	Ch. 21	Ch. 31	Ch. 39	Average
220	7.92	8.05	8.15	8.62	9.35	8.42
150	6.10	6.01	6.30	6.62	6.99	6.40
100	4.56	4.61	4.73	4.89	5.28	4.81
75	3.68	3.67	3.73	3.93	3.96	3.79
39	2.31	2.20	2.13	2.28	2.41	2.27

Noise is usually given as Equivalent Noise Charge (ENC) referred to the amplifier input. The total charge delivered by the sensor is the quantity of interest. Expressing the noise in terms of ENC allows a comparison between the noise floor and the signal to be measured.

$$\text{ENC} = \frac{\text{rms output noise(ADC counts)}}{\text{gain(ADC counts/fC)}}$$

In a separate measurement we determined that injecting 80 fC of charge into the input causes the ADC sample to change by 900 counts, yielding a gain equal to 11.25 ADC counts/fC. For an rms noise of 1 ADC count (noting that 1 fC = 6241 electrons):

$$ENC(1) = 0.0889 \text{ fC} = 555 \text{ electrons}$$

Refer to Table 2 to view the ENC versus the detector capacitance.

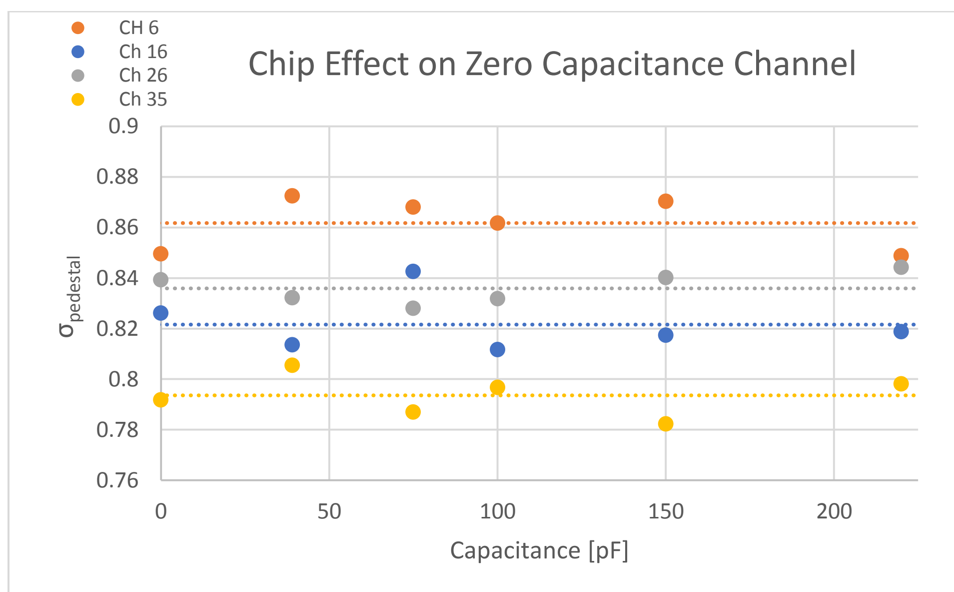
Table 2

The Equivalent Noise Charge (ENC) of the signal values, a common mode of analyzing noise beyond the standard deviation values.

Cap [pF]	Average Charge (fC)	Average Number of Electrons
220	0.740	4617
150	0.569	3554
100	0.428	2671
75	0.337	2105
39	0.201	1257

Graph 2

Values across channels with no added capacitance on each chip card. The points are classified along the x-axis using the capacitance of the card, but these specific channels did not have added capacitance. This indicates that the level of variation of σ from card to card is negligible.



References

[1] S.H.I Barboza et al., *SAMPA chip: a new ASIC for the ALICE TPC and MCH upgrades,* *https://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02088*

[2] Angelo Rivetti (2015). *CMOS Front-End Electronics for Radiation Sensors*. CRC Press.