CAEN Tools for Discovery — Electronic Instrumentation

# V775

## 32 Channel Multievent TDC (35÷300 ps)

- High channel density
- 12 bit resolution
- 5.7 µs / 32 ch conversion time
- 600 ns fast clear time
- Zero and overflow suppression for each channel
- ±0.1% integral non linearity
- ±1.5% differential non linearity
- 32 event buffer memory
- BLT32/MBLT64/CBLT32/CBLT64 data transfer
- Multicast commands
- Libraries, Demos (C and LabView) and Software tools for Windows and Linux

The Mod. V775 is a 1-unit wide VME 6U module housing 32 Time-to-Digital Conversion channels.
The Full Scale Range can be selected via VME from 140 ns to 1.2 µs with 8 bit resolution. The board can operate both in COMMON START and in COMMON STOP mode. Each time interval between the COM signal and the input signal is converted into a voltage level by the TAC sections. The outputs of the TAC sections are multiplexed and subsequently converted by two fast ADC modules (5.7 µs conversion time).
The integral non linearity is ±0.1% of full scale range (FSR), measured from 2% to 97% of FSR; the differential non linearity is ±1.5% of FSR, measured from 3% to 100% of FSR. The ADCs use a sliding scale technique to reduce the differential non-linearity.
Programmable zero suppression, multievent buffer memory, trigger counter and test features complete the flexibility of the unit. The module works in A24/A32 ADDRESS mode. The data transfer occurs in D16, D32, BLT32 or MBLT64 mode. The unit supports also the Chained Block Transfer (CBLT32/CBLT64) and the Multicast commands. The board supports the live insertion that allows inserting or removing them into the crate without switching it off.

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| **Packaging** | 1-unit wide 6U VME module (version AA requires the V430 backplane) |
| **Inputs** | 32 ECL inputs, 110 Ohm impedance |
| **Resolution** | 12 bit |
| **Full Scale Range** | VME programmable from 140 to 1200 ns<br>(if sliding Scale is used FSR is reduced from 4095 to 3840 counts) |
| **LSB** | VME programmable from 35 to 300 ps |
| **RMS Noise** | 0.8 counts typical, 2 counts maximum |
| **Integral non linearity** | ±0.1% of FSR<br>(measured from 5% to 95% of 3840 counts) |
| **Differential non linearity** | ±1%<br>(measured from 5% to 95% of 3840 counts) |
| **Interchannel Isolation** | > 66 dB |
| **Power rejection** | 0.01 count/mV (+5V); 0.02 count/mV (-5V)<br>0.005 count/mV (+12V); 0.001 count/mV (-12V) |
| **Fast clear time** | 600 ns |
| **Conversion time** | 5.7 µs for all channels |
| **Minimum Start/Stop delay** | Common Start mode: 14 ns<br>Common Stop mode: 4 ns |

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| **Zero suppression** | Threshold values programmable in:<br>16 ADC counts steps over the entire FSR<br>2 ADC counts steps over 1/8 of FSR |
| **GATE COMMON input** | Two LEMO 00 bridged connectors, NIM signal, high impedance<br>Common Start/Stop signal |
| **Control inputs** | active-high, differential ECL input signals:<br>RST: resets PEAK sections, MEB status and control registers<br>VETO: inhibits the conversion of the peaks<br>FCLR: FAST CLEAR of TAC sections<br>COM: Common Start/Stop signal |
| **Control outputs** | differential ECL output signals:<br>DRDY: indicates the presence of data<br>BUSY: board full, resetting, converting or in MEMORY TEST mode |
| **VME interface** | A24/A32<br>Geographical Addressing<br>Multicast commands<br>D16/D32,BLT21/MBLT64,CBLT32/CBLT64 |