From: "Ed Jastrzembski" <jastrzembski@jlab.org>
Subject: Re: Trigger Supervisor
Date: Tue, September 7, 2010 4:23 pm
To: hyde@jlab.org

Hi Charles,
The 'live' output is asserted (positive logic, differential ECL: Q = -0.8V, /Q = -1.6V) when the TS can accept a Level 1 trigger. 'busy' is the exact complement of 'live'.

Assuming buffered mode operation and a single level trigger:
When the TS accepts a trigger, 'live' is de-asserted (Q = -1.6V, /Q = -0.8V) and remains in this state until 'front end busy' is de-asserted and the trigger information (trigger type) is stored into a TS buffer. 'front end busy' represents the time for the front-end modules (ADCs, TDCs) to process the current trigger (i.e. L1 Accept from TS) - this is real dead time. 'front end busy' is de-asserted when all the modules are ready to accept the next trigger. The next trigger may be accepted while the previous trigger is being read out (no dead time attributed to readout). The fraction of time that 'live' is asserted is a true measure of the live time of the experiment. Readout will only contribute to the dead time if the 6-deep trigger buffer gets full. Then an event must be read out of the front-end modules to allow space for the next trigger.

- Ed J.

hyde@jlab.org wrote:
> Dear Ed,
> Following up our meeting on Hall A DVCS DAQ,
> Can you confirm the meaning of "TS Live", output 10
> of the Trigger Supervisor.
> What is the polarity (eg logic true = TS is live and ready for an event?)
> What aspect of the TS is "live" or "busy"?
>
> Sincerely,
> Charles Hyde
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