TDIS DAQ and trigger development

July 2020 TDIS collaboration meeting

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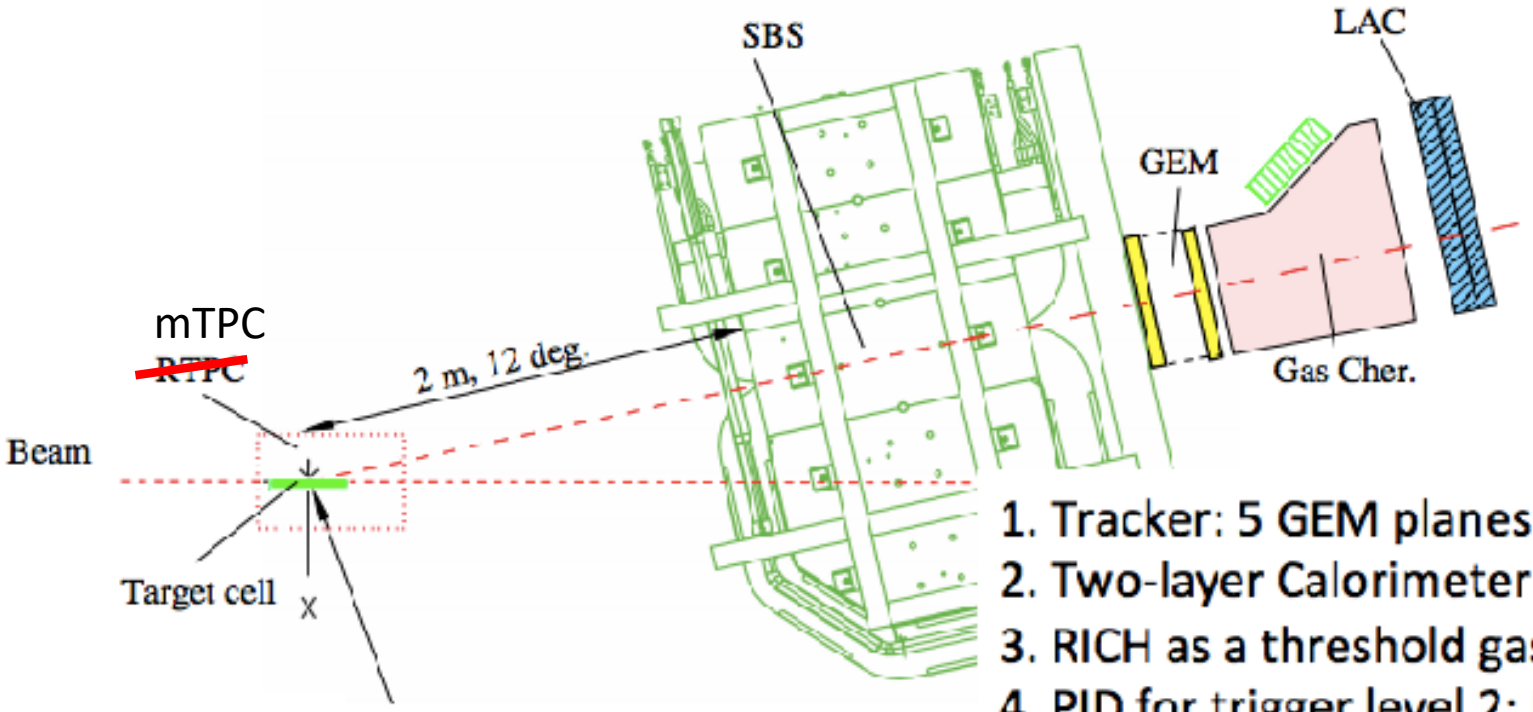
Overview

Scattered electron detection in Super Bigbite Spectrometer



1. Tracker: 5 GEM planes (from G_E^P expt.)
2. Two-layer Calorimeter (LAC from CLAS6)
3. RICH as a threshold gas Cherenkov
4. PID for trigger level 2: LAC + Cherenkov

2015 experimental layout

DAQ & trigger overview

- Primary physics trigger: electrons detected in SBS
  - Event rate ~ 6 kHz
- SBS DAQ
  - LAC: 256 PMTs, instrumented with GEP electronics or with FADC & VTP
  - RICH: 1938 PMTs, instrumented with VETROC
  - GEMs: instrumented with APV→MPD→SSP
- mTPC read out by SAMPA
  - Estimated data rate from mTPC @6 kHz: 1+ GB/s

Recent activities

- SAMPA test stand has been active

- Development of TDIS SBS DAQ and triggering has not been active
  - Similar to the Compton polarimeter DAQ upgrade & other planned DAQ systems
  - Recently reached out to begin planning discussions

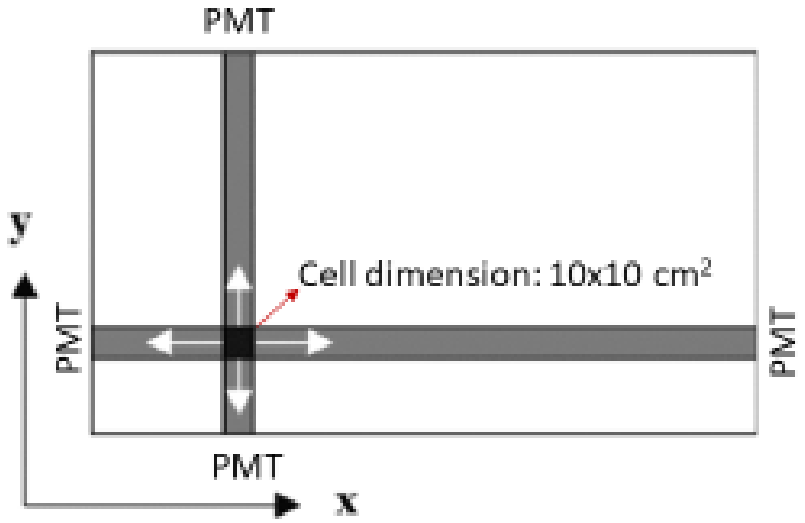
Triggering ideas

- PR12-15-006 proposed an L1 trigger formed by total energy deposition in LAC followed by L2 formed by relative energy deposition in both LAC layers plus the Cerenkov signal
  - Proposal had LAC instrumented by borrowing ECAL instrumentation
  - L1 trigger formed by discrimination of analog sums
  - Cerenkov signals would be combined in NINO into 250 signals
- Newer ideas
  - Cerenkov instrumented with all 2000 PMTs through VETROC
  - Instrument all 256 LAC PMTs using FADC→VTP to form clusters/check thresholds in FPGA

LAC: Cells and Trigger Configuration

→ **Each cell is the crossing of 2 adjacent stacks with different orientations**

→ We have a grid of 40x24 cells (960 cells total)



Trigger:

→ There are 256 channels (PMTs) in the LAC (64 stacks X 2)

→ We would "AND" the 2 sides of every stack

→ Then we would "AND" the "AND"s of 2 adjacent (in the vertical) stacks with different orientation; this would be a cell

→ Then we would "OR" all the cells

→ This would be done per region (inner, outer)

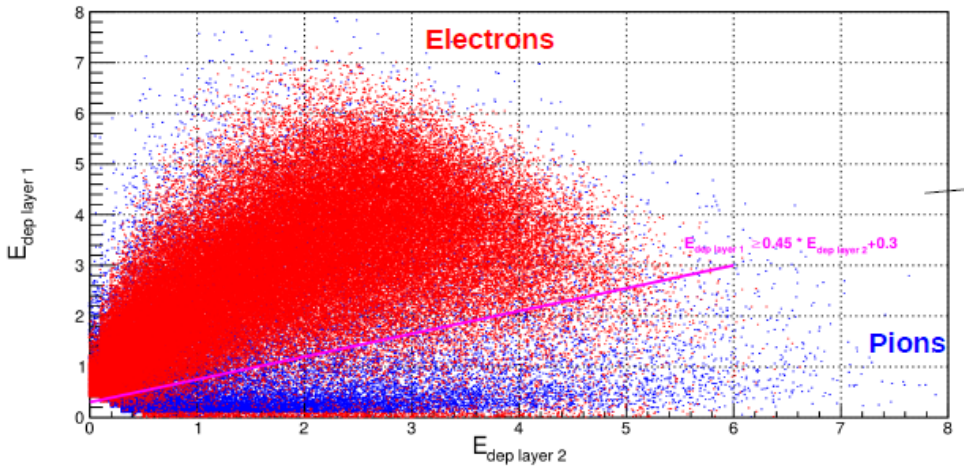
→ We would need all 256 channels read by FADCs (to get timing, amplitude, integral, PED)

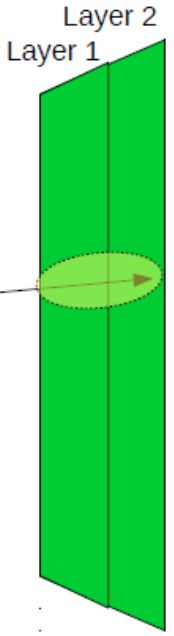
→ The trigger should be FPGA based

→ We would like to have the option to use the relative energy deposition in the two regions to do some pion rejection at the trigger level

Slide from S. Malace

LAC pion rejection





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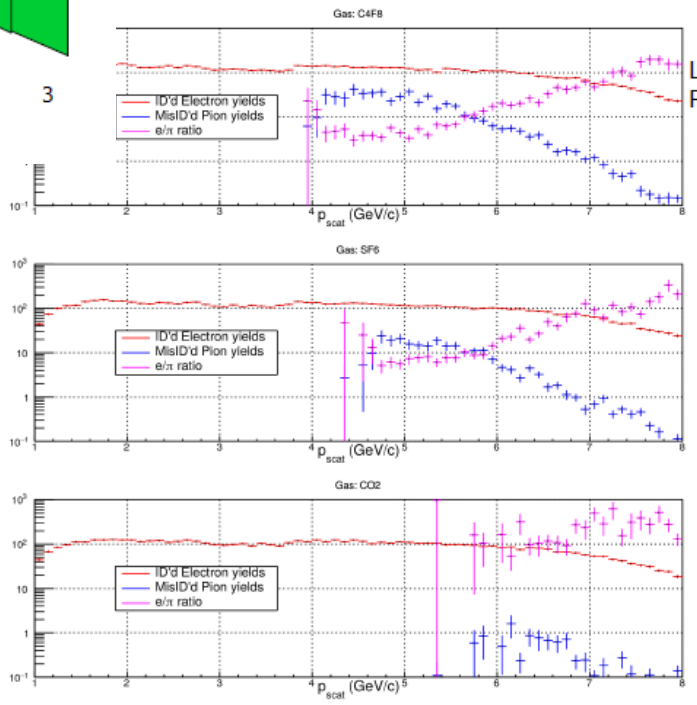
ion rejection: combination with RICH

PRELIMINARY



LAC e selection +
RICH e selection

From E.F on 19 May 2020

https://hallaweb.jlab.org/wiki/images/b/b7/ElectronAnalysis_PiRejection.pdf

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RATE NOTES FROM FEB2018 & C12-15-006 APPROVAL REQUEST

Rates in C12-15-006 approval request

- [PK]: Assuming 6 kHz triggering, 0.8 MHz average rate per mTPC pad, and 1.5us readout window, and 120 bits/hit (12 10-bit samples)
  - Raw rate of 2.7 GB/s (21.6 Gb/s) from all SAMPAs to 8 collector PCs
  - Pulse fitting reduces this by ~3 to 0.9 GB/s (7.2 Gb/s)
- [EJ]: With elevated 20kHz triggering, 1 MHz on all channels, and pulse fitting & zero suppression
  - Each of 8 PCs has 0.55 GB/s (4.4 Gb/s) for total of 4.4 GB/s
  - Scaling to 6kHz gives ~1.3 GB/s
- Neither consider any additional data filtering or compression to further reduce the network traffic

What is this based on?

- mTPC design with 10 5cm-long drift chambers arrange longitudinally; inner radius is 5 cm, outer radius is 15 cm.
  - Drift time in each chamber is ~1 us
  - Each chamber instrumented by ~2500 5mm x 5mm pads
- Rate estimates done by Marco
  - Initial rate estimates were for about 98 MHz of protons throughout each chamber → average rate per pad was ~0.8 MHz.
  - Rate estimates from Dec 2017 have ~68 MHz of charged particles crossing the inner ring of pads → average rate on inner ring ~1 MHz

Some data rate cases

- Assuming an average hit requires 12 50-ns time bins to be recorded (300 ns) and using the 0.8 MHz hit rate per pad, the “time-bin occupancy” will be 24%.
- Each chamber has 2500 pads sampling at 20 MHz, so there are 50e9 samples per second per chamber; 12e9 are filled.
  - Using SAMPA as a baseline, 1 chip handles 32 channels, with 10b sampling and 1.28 Gb/s output.
    - Keeping only filled bins & w/o timestamps would give 1.536 Gb/s, so to output 20 MHz sampling would require <26 pads per chip
- The trigger rate from electrons in the SBS should be ~6 kHz.
  - In each trigger, we expect an average of 0.8 hits/pad, so there would be 0.15e9 filled samples/chamber/trigger →0.6 GB/s/chamber at 4 bytes per filled sample (amplitude and timestamp)