TDIS DAQ Thoughts

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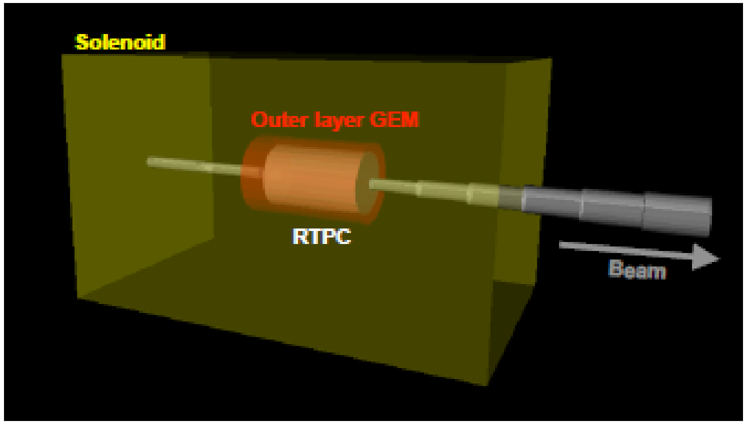
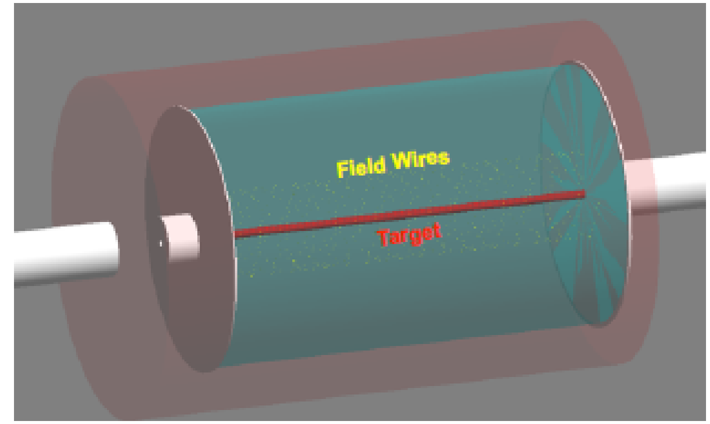
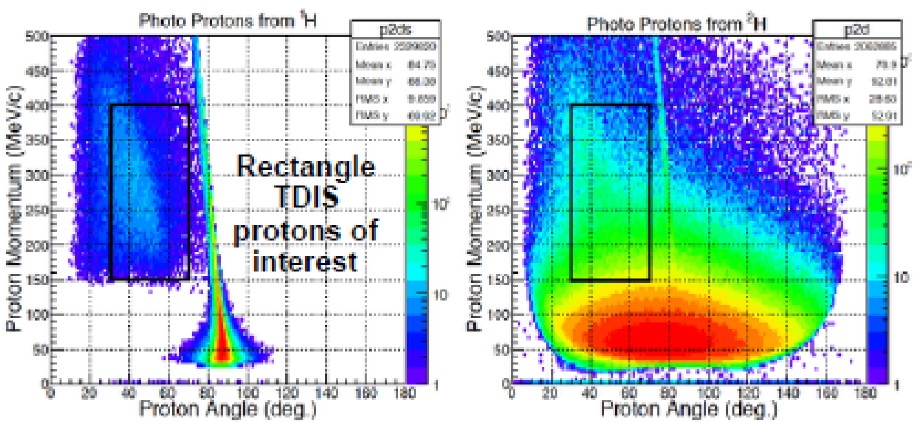
Some questions & remarks

- What is the longest drift time we need to handle?
  - Newest results suggest 20us should be possible
- How many strips will be hit per track?
  - Using a geometry of 22x817 (z , phi) strips per layer, ~410 strips are hit for an 100 MeV proton track
- How many hits per readout strip do we expect in each trigger?
  - ^{2}H: (357 MHz)*(410 strips hit)*(20us)/(18k strips) = 162 hits
  - Average time between hits: 20us/162 = 120ns
  - Rate for H tgt is lower, but how much lower?

Geant4 RTPC Geometry and Background Simulations







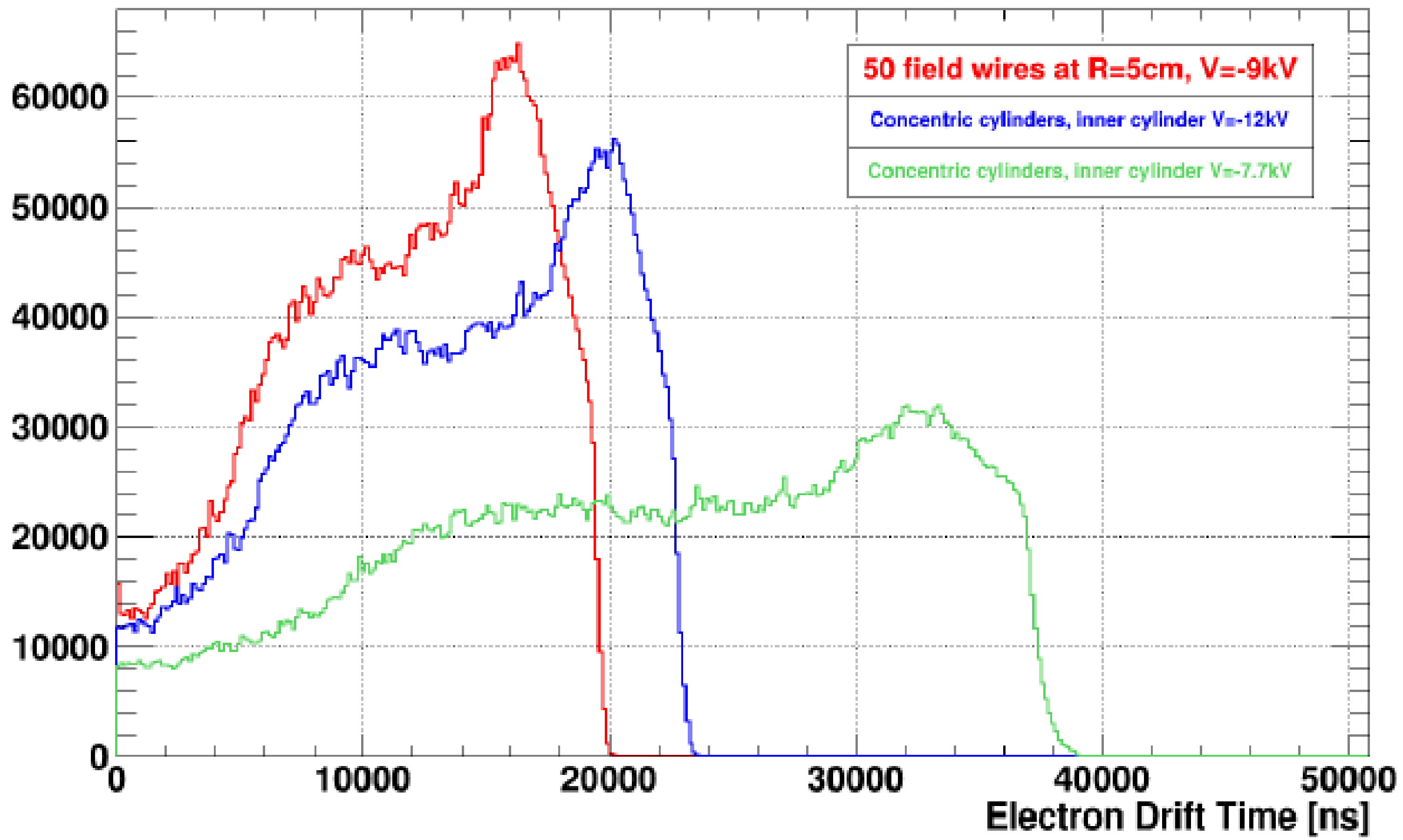
Proton background rates

Target	θ_p (deg.)	$70 < p_p < 250$ (MHz)	$p_p > 250$ (MHz)	$150 < p_p < 400$ (MHz)
^{1}H	30 - 70	2.3	7.4	6.3
^{2}H	30 - 70	357	20.1	64
^{2}H	100 - 140	204	3.1	–
^{27}Al	30 - 70	0.37	0.0	0.05
^{27}Al	100 - 140	0.10	0.0	–

- Realistic RTPC Geant4 geometry developed by J. Annand (as slide 2) to study background processes/rates
- Moeller electrons mostly contained by solenoid
- Dominant background - proton production by photonuclear processes
- ^{1}H target: mostly removed after quasi-elastic cuts.
- ^{2}H target: accidentals separation using time/vertex reconstruction (SBS +RTPC)
- Study of drift electrons within RTPC on-going…

From R. Montgomery, December BoNuS/TDIS meeting

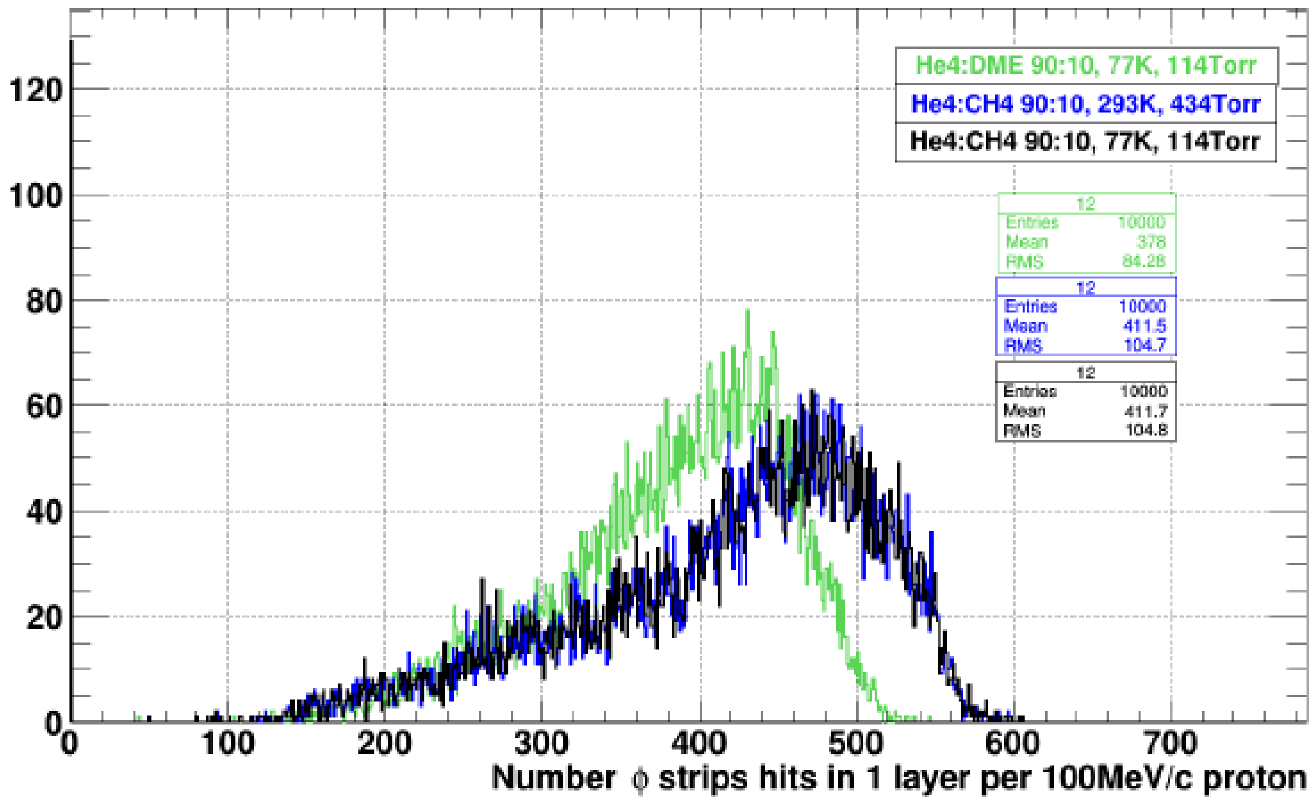
Electric Field Increase Shortens Drift Times!
~20 Microseconds achievable depending on field set-up



- Strips hit per proton still of roughly same magnitude
- For He:CH4 90:10, 77K, 114Torr and 50 field wires at r=5cm and V=-9kV then:
- Worst case for **H target: 2.3x10^6 x 20x10^-6 x 412strips = 18 952 strip hits at once, ~105% occupancy**
- Worst case for **H2 target and HeCH4: 357MHz x 20us x 412strips = 2 941 680 strips hit at once, ~16 342% occupancy**

From R. Mongomery, TDIS_RTPC_Sim_270317.pdf, pg 8

Readout Strip Occupancies



- Say 18k strips per layer (817 to cover phi, 22 to cover z)
- **Occupancy per layer and per 100MeV/c proton = 2.3%, say 2%**
- Take nominal he:CH4, 90:10, 77K, 114Torr, then upper drift time limit say 38us
- Background rate for H target and theta = 30-70degrees = 2.3MHz
- Background rate for H2 target and theta = 30-70degrees = 357MHz

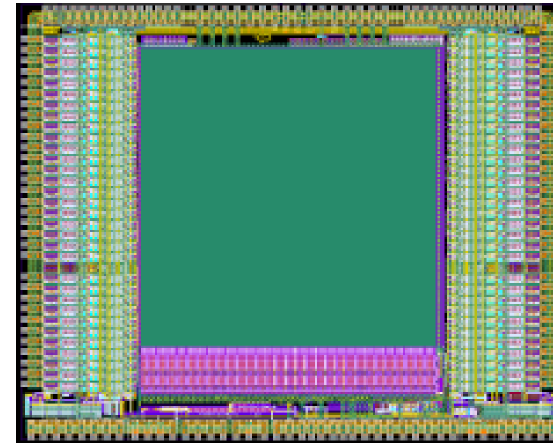
- Worst case for **H target and HeCH4: 2.3x10^6 x 38x10^-6 x 412strips = 36 009 strip hits at once, ~200% occupancy**
- Worst case for H target and HeDME: 2.3x10^6 x 35x10^-6 x 378strips = 30 429 strip hits at once, ~169% occupancy
- Worst case for **H2 target and HeCH4: 357MHz x 38us x 412strips = 5 589 192 strips hit at once, ~311 000% occupancy**
- Worst case for H2 target and HeDME: 357MHz x 35us x 378strips = 4 723 110 strips hit at once, ~262 000% occupancy

From R. Mongomery, TDIS_RTPC_Sim_270317.pdf, pg 7

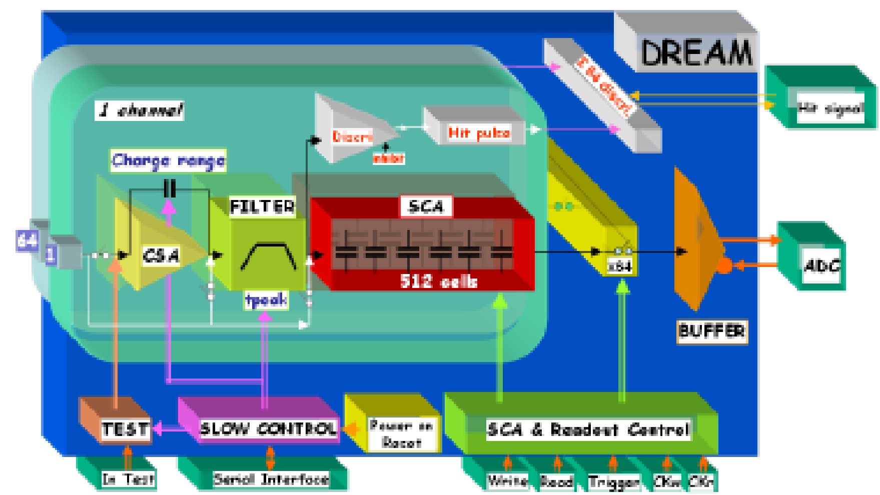
64-channel Dream ASIC

Dead-timeless **R**ead-out **E**lectronics **A**SIC for **M**icromegas

- Characteristics
  - → 4 gain ranges: 60 fC, 120 fC, 240 fC, 600 fC
  - → 16 programmable peaking times: from 50 ns à 1 μs
  - → Sampling rate: 1- 50 MHz
  - → 512-cell deep analog memory per channel
    - Trigger pipeline of 16 μs + de-randomizing
  - → Readout rate: max 25 MHz
  - → 128-pin 0.4 mm package
    - Small 17 mm x 17 mm footprint
  - → Adapted for different detector types



- ~1700 units produced and packaged
  - → ~100 still available
- ~300 unpackaged units available



From Irakli's talk at December BoNuS/TDIS meeting

More questions, fewer remarks

- How long will the charge collection for one hit last?
  - Taking the 20us full drift time divided by 400 pads suggests 50 ns drift time variation across a pad; ought to be modelled
  - DREAM chip has a minimum peaking time of 50 ns
- What is the peak charge we need to be recording?
- How many samples are needed to define each hit?
  - We had called for 10ns resolution in the proposal. To fit 20us in the 512 SCA, we'd need to be using ~40ns sample period. MVT readout expected to use 3 samples to find peak time & 10 samples to contain full pulse

Not even questions

- We'd be operating the DREAM chip in single trigger mode, without buffering. To read 500 samples from the DREAM chip at 25 MHz:
  - (500 samples)*(74 channels+overhead)*(40 ns) = 1.480 ms. Maximum rate: 675 Hz
  - Do we want that high a dead time…
- Possible ways to reduce readout time
  – Sparse readout: may make time resolution worse?
  – Zero suppression: only really helps if # of hits times samples per hit is much smaller than the full 500 samples