# VETROC Tests

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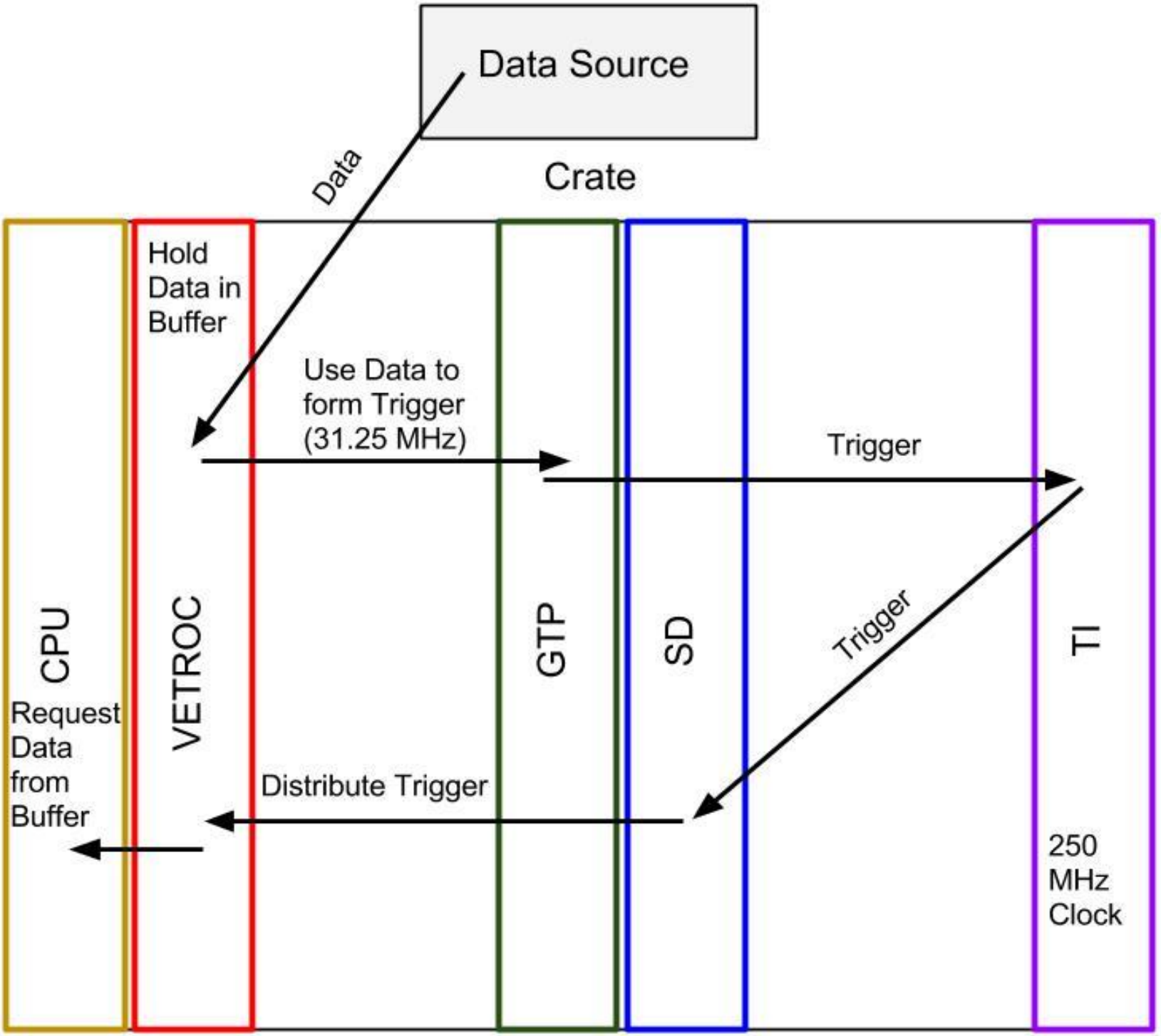
Thanks to: Bob Michaels, Ben Raydo, Alexandre Camsonne, Bryan Moffit

# VETROC Board

- High-rate pipelining TDC which together with a CTP is self-triggering.
  - TDC words have a Dynamic Range of 32 bits.
- Up to 128 channels of data per board.
  - Can use up to 17 boards (2176 channels) with a single CTP.
- 4 gigabit per second bandwidth.
- Works with any differential input (ECL, LVDS, etc.) from ± 100 mV to ± 4 V.

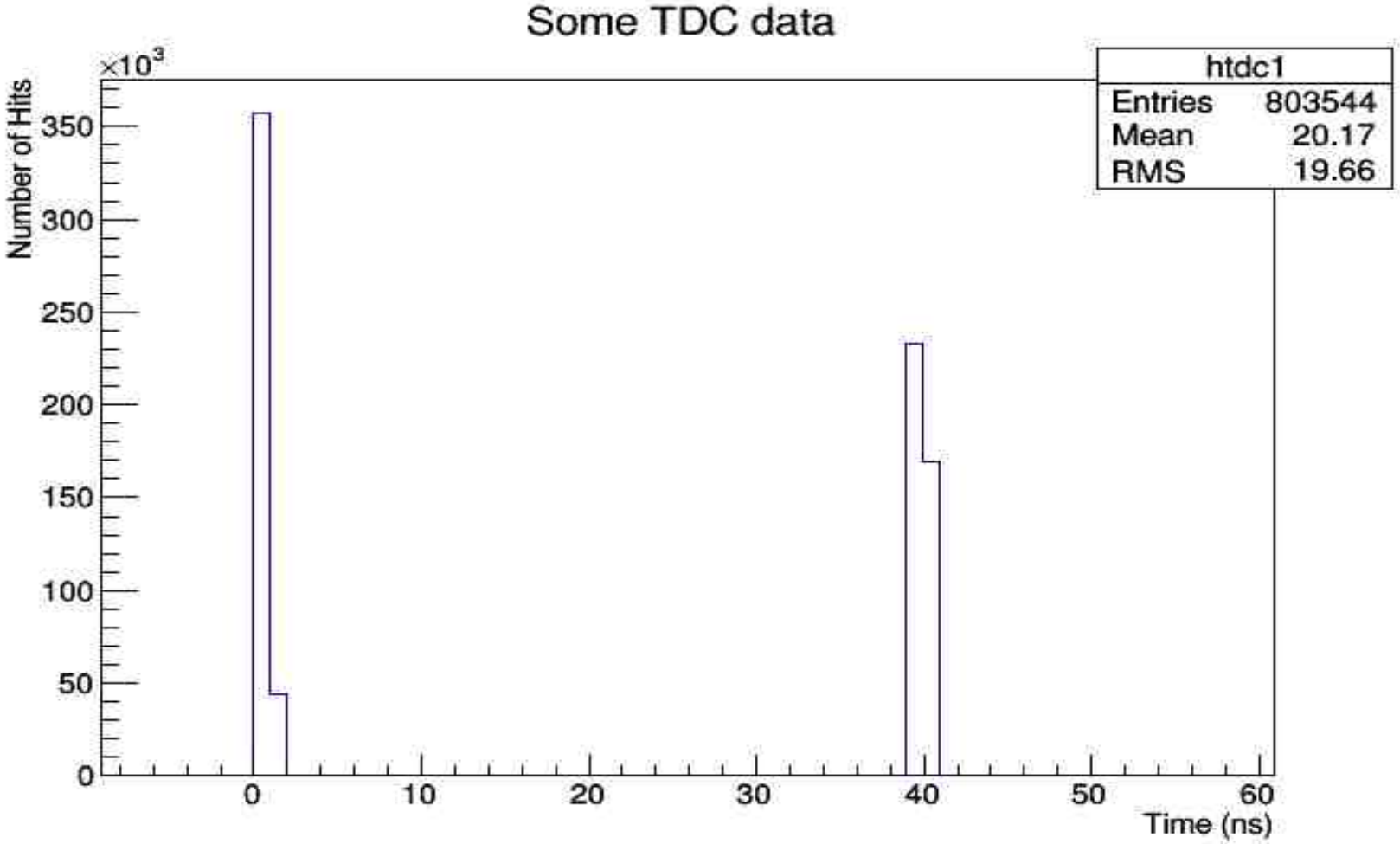
# VETROC Board Cont.

- Trigger can be formed in two ways:
  - Front panel triggers using external NIM electronics.
  - CTP (GTP) which uses data from the VETROC to form triggers. Useful for more complicated triggering.
- GTP trigger is programmed using FPGA run in Quartus.
  - Tested with simple M out of N trigger.
  - Working to implement more complicated trigger for detectors.
- Price for 1 board is less than $2000.


Data Source
Data
Crate
Hold
Data in
Buffer
Use Data to
form Trigger
(31.25 MHz)
Trigger
CPU
VETROC
GTP
SD
Trigger
TI
Request
Data
from
Buffer
Distribute Trigger
250
MHz
Clock

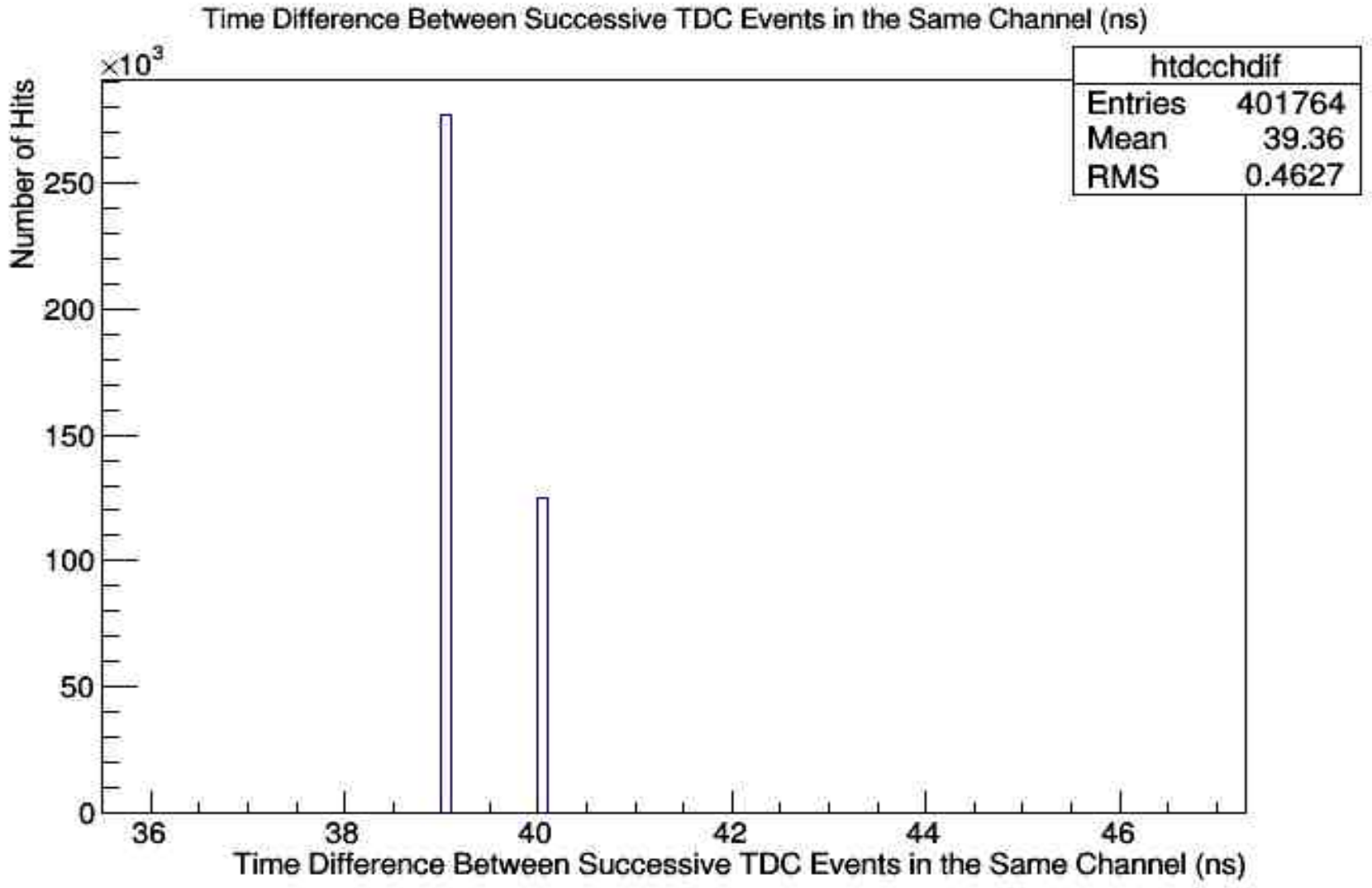
# TDC Data

- Single pulses of 40 ns width at 10 kHz rate in two channels.
- Requires reference channel to eliminate clock reference.
- Time Resolution of 1 ns.
  - Resolutions up to 20 ps have been observed by DAQ group.



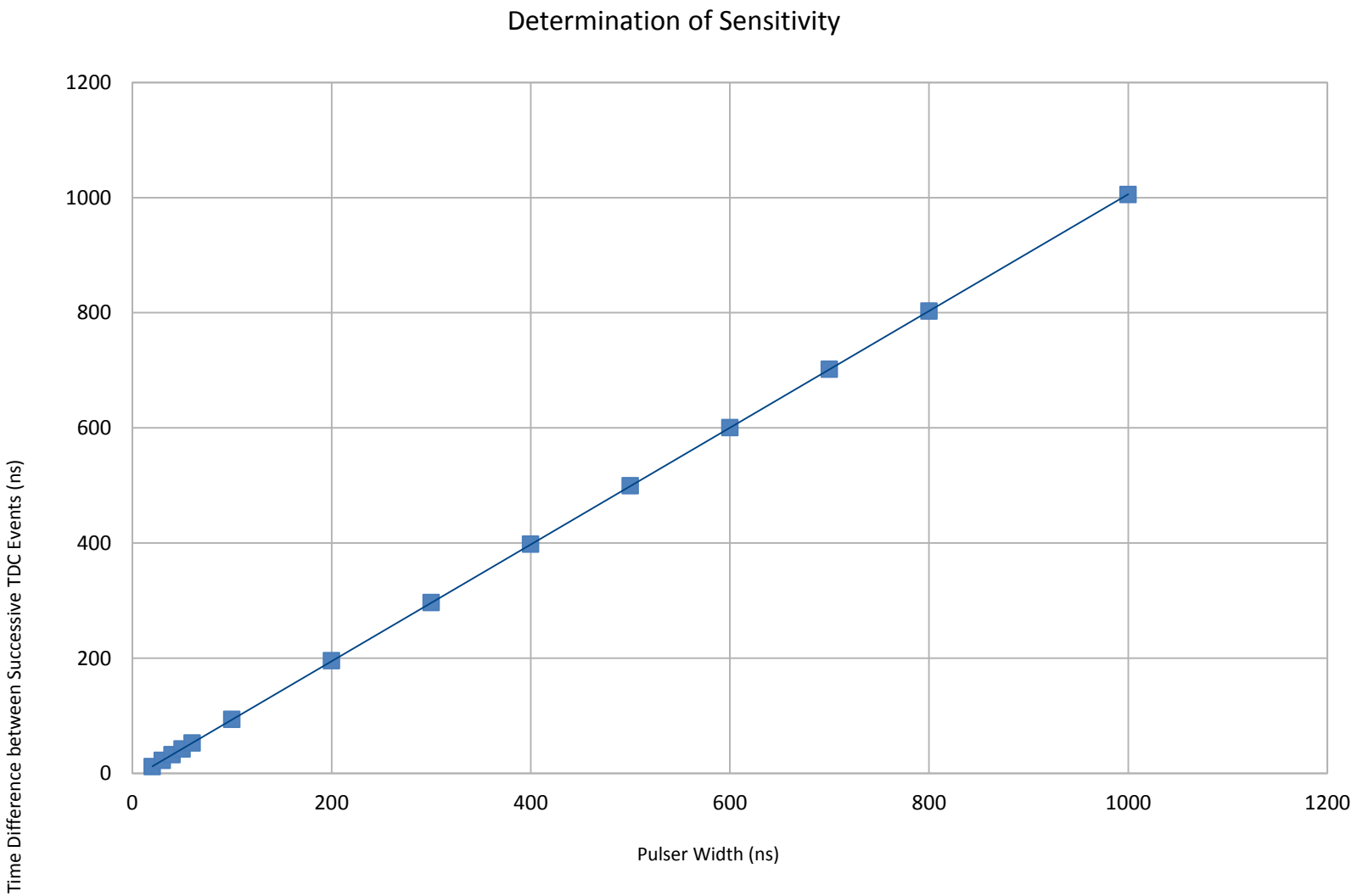
# Time Difference Between Events

- Single pulses of 40 ns width at 10 kHz rate in two channels.
- RMS of ~0.5 ns.



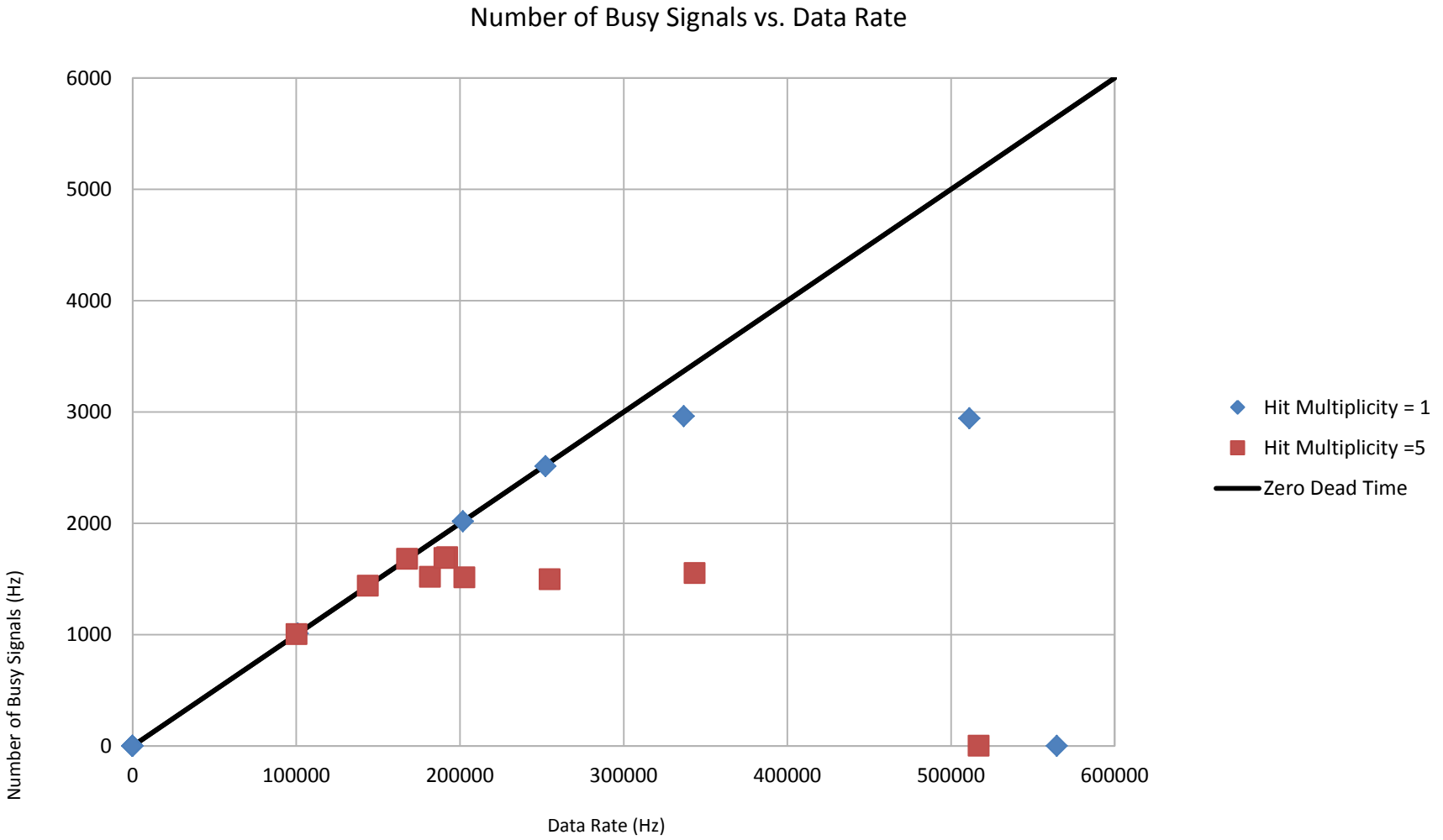
# Sensitivity/Resolution

- Determination of nanoseconds per TDC count.
  - 1 ns/count

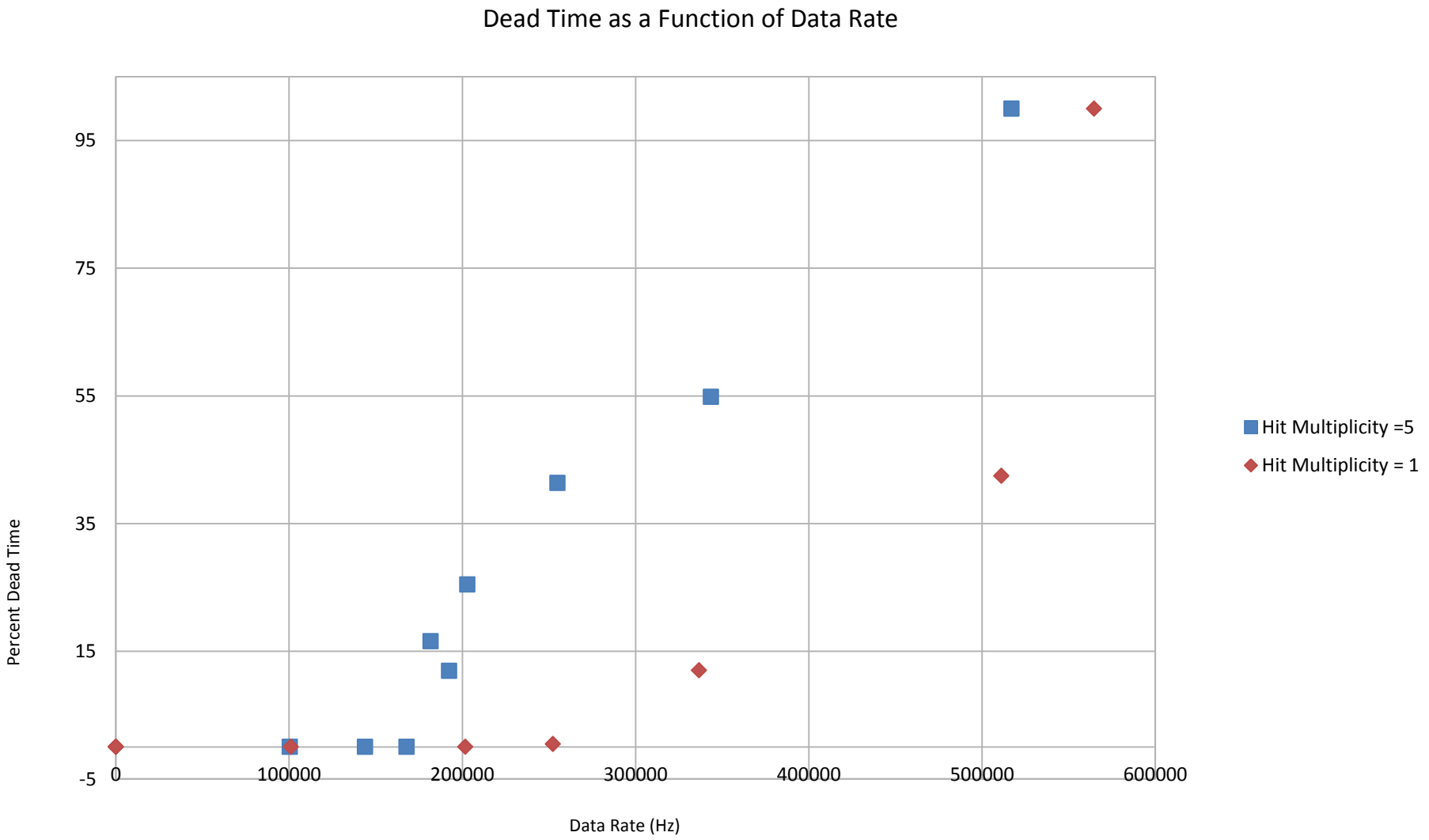


# Speed/Dead Time Measurements

- Tests done using block mode readout with blocks of 100 events.
  - Buffer set to hold 10 blocks.
- Dead time measured by reading busy signals out of TI and comparing to the data rate read by a scaler.
  - Expect 2000 busy signals at 200,000 Hz.

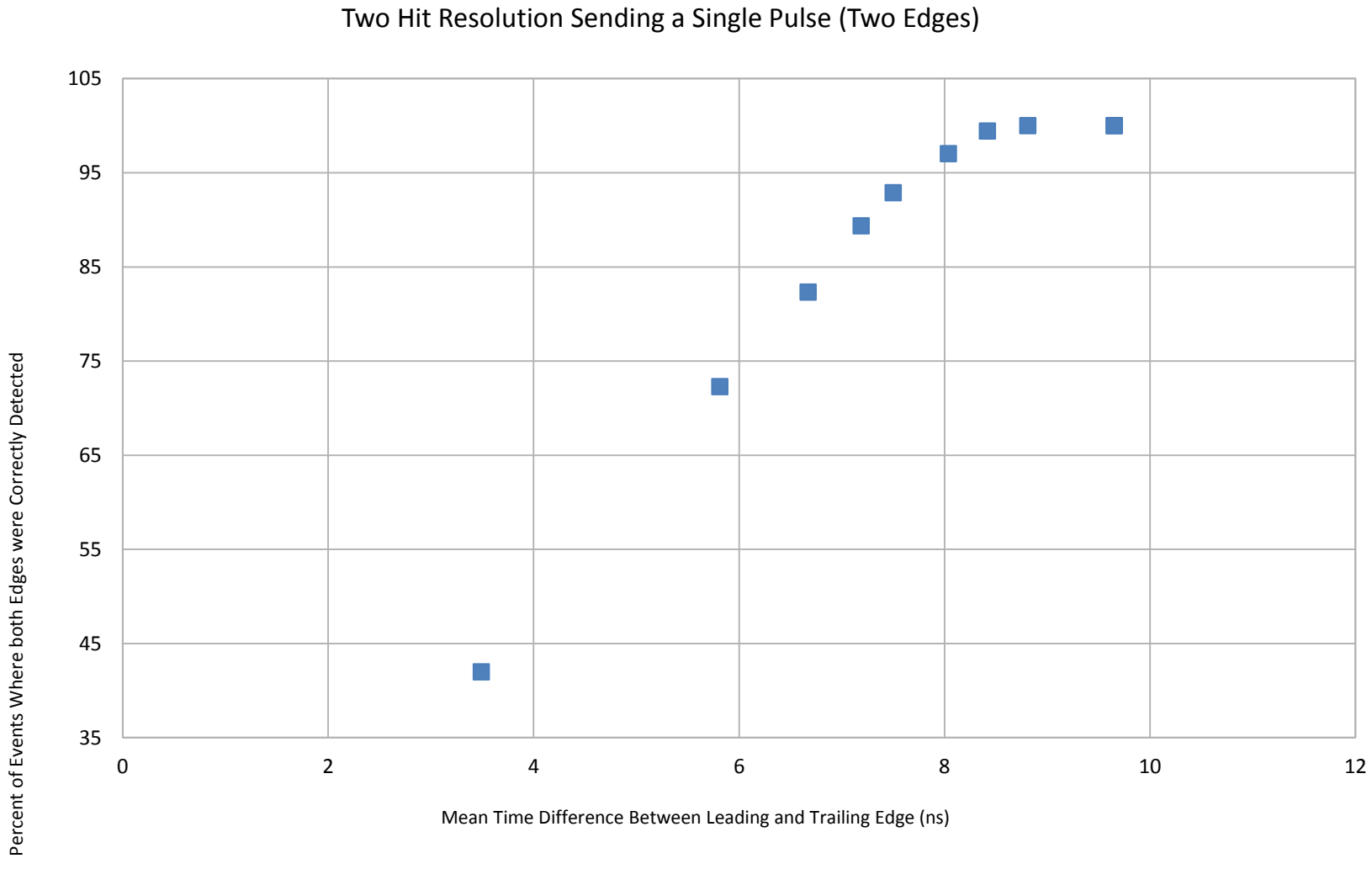


- Measured dead time for hit multiplicity = 1, 5.
  - Hit multiplicity 1 has zero dead time up to ~250 kHz.
  - Hit multiplicity 5 has zero dead time up to ~166 kHz.



# Two-hit Resolution

- Determined by measuring the difference of TDC times between the leading and trailing edges of a single pulse.
  - 0% events missed ~8.8 ns width
  - 10% events missed ~7.2 ns width



# Future Work/Conclusion

- Create more complex GTP triggers with FPGA.
- Tests with many channels.
  - Prototype detector from William and Mary.
- Random data instead of regular data.
  - Cosmics or other real data.
- Develop analysis software further.
- VETROC is a high rate TDC with many possible applications.
  - Can measure 1000s of channels with several boards.
  - Very high timing resolutions possible (20 ps).