APV-25 readout system options for the SBS back GEM tracker

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Introduction

The two SBS back trackers will consist of 40 GEM modules, each with an active area of 60 x 50 cm$^2$. The modules will have x-y Cartesian readout with a pitch of 400 µm in each direction. The readout strips along the x direction are organized into 12 128-pin connectors, while the y stripes are routed through 10 128-pin connectors. As such reading all readout strips in the 40 modules requires 112,640 (22x128x40) readout channels. It was initially anticipated that 4 adjacent readout strips could be combined into a single electronics channel to reduce the cost of electronics. However, tests with the prototype GEM modules and electronics have revealed that combining 4 strips is not possible due to charge saturation effects in electronics channels. While combining 2 strips will still result in some saturation, this may present a workable compromise between the optimum single strip readout and keeping electronics costs down. In this report we are assuming the 2-to-1 combination scenario. In the 2-to-1 combination scenario, given the geometric constraints of the GEM modules, 12 128-channel APV-25 cards are required to readout a single module, leading to 480 cards (61,440 channels) for all modules; with approximately 10 % spares, leading to 530 cards (67,840) channels in total.

We considered two APV-25 based readout systems for the SBS back tracker readout: first one based on the CERN Scalable Readout System (SRS) architecture, and the second, the MPD APV-25 system designed and built by our INFN colleagues for the SBS front tracker GEM readout. The discussion presented here is based on our tests done the 10,000 channel APV-25 readout system was assembled at the University of Virginia as part of the SBS pre R&D program. While we also assembled and tested a 2800 channel INFN-MPD system at UVa, there have been many improvements implemented on the MPD design since then. Therefore the results reported here for the MPD would be the ones provided by the INFN group.

APV25-SRS system

The test results from the prototype SRS system was presented in a previous report. Therefore only a summary of the SRS system performance is given here. It should be noted that since submitting the previous report a test beam run was conducted in Hall A. The results from this run confirmed the noise level performance of the SRS system indicated in the report. The figures 1-4 show results from the Hall A test run.

1. Pedestal noise level: the RMS noise level achieved for lab bench tests was approximately 10 ADC channels (2300 e- ENC) while the noise level observed at Jefferson lab was slightly higher at around 12 ADC channels (2760 e- ENC). A small number of channels (~ 5% of all channels) have noise levels around 20 channels. In practice, a five times pedestal RMS cut is required to cleanly remove pedestal noise. This gives a lower limit of around 60 ADC channels per strip for the SRS APV system. (The SRS APV saturates
at approximately 1800 ADC channels; the average MIP signal per strip, with a moderate gain of 5000, is approximately 200 ADC channels.

2. DAQ speed: The tests indicated that with the current setup the maximum DAQ speed with 3 sample readout would be approximately 1 kHz. As described in the previous report, the bottle-neck for this rate limitation comes from the 1 GB/s data transfer speed between the SRU unit of the SRS system and the DAQ PC. Currently there are plans underway to upgrade this link speed to 10 GB/s. More detail is given below.

3. Placement of the DAQ hardware in the hall: In the current configuration of the SRS, the HDMI cable connecting the APV hybrid card on the GEM module to the FEC card in the electronics crate has to be shorter than 5 m. In the SBS case this would require the electronics crate to be placed in a high radiation, high noise environment. There is new R&D planed for this summer to develop a new copper-to-optical coupling box that would allow the electronics crate to be moved much further from the spectrometer.

4. The timing accuracy: rejecting background under high luminosity SBS conditions requires the signal time to be known to about 10 ns accuracy. The data taken during the FNAL test run show that the APV SRS system provides the required timing accuracy (see Fig. 5).

Figure 1: A busy, multi-cluster event from the test run taken in Hall A, showing high signal to noise performance under Hall A conditions (estimated Gain of the detector is ~ 5000)
Figure 2: rms noise (in ADC counts) per channel for one apv25 FE card on top strips (top) and on bottom strips (bottom) for Jlab Hall A test run.

Figure 3: Distribution of the RMS noise (ADC counts) for APVs connected to the SBS detectors during the Hall A test run.
Figure 4: The ADC distribution, for the strip with the maximum ADC value in a cluster, obtained with SRS APV system for a run with a moderate gain (~5000). At this gain about 5% of the events show saturation.

Figure 5: Timing characteristics of the SRS APV-25 system: (left) the signal start time (with respect to the scintillator trigger) and (right) the pulse shaping time for data taken with the SBS prototype module during the test beam run at FNAL. Note that this figure shows the timing characteristics for one localized beam spot on the chamber. The variation of timing as a function of position in the detector is still under investigation.
New commercially produced APV25-SRS system

The RD-51 collaboration has recently licensed a commercial company, EicSys GmbH, to produce large scale SRS systems. This system will be based on the commercial standard ATCA (Advanced Telecommunications Computing Architecture) architecture. With the already established SRS technology they EicSys can produce the system described below. Proposed improvements to this system are outlined in the next section of this report.

The SRU-ATCA system consists of the following components:

- APV-25 hybrid cards mounted on the detector. These cards contain the 128 channel APV-25 chip which reads data from detector multiplexes the data and transmits analog to the ADC card.
- An ATCA blade housed in an ATCA crate. One ATCA blade accommodates two SRS-ADC mezzanines, each one containing 24 ADC chips. Each ADC chip is connected to an APV-25 hybrid card via an HDMI cable link; a single HDMI cable connects a pair of ADC chips with a pair of APV-25 hybrids. The ADC chip de-multiplexes data arriving from the APV chips and converts into digital format. The ATCA blade handles the clock and trigger synchronization. A single ATCA blade handles 48 APVs corresponding to 6144 channels.
- A RTM card that provides a direct link from the ATCA blade to the Scalable Readout Unit (SRU). In the current configuration this link is limited to 1 Gb/s; upgrade plans to 10 Gb/s as described below. The long term plans call for the SRU unit to be housed in the first slot of the ATCA crate and the communication between the ATCA blade and the SRU to go through the ATCA back plane. Once this is implemented the RTM is not needed. However this part of the SRS development will not be available in the SBS timescale, and thus, the plans presented here assume communications handled by RTM instead of the backplane.
- The Scalable Readout Unit (SRU), which distributes the clock and trigger synchronization to the ATCA blades and handles communication between multiple (up to 40) blades and the data acquisition computer. The SRU unit builds events using event fragments from the ATCA blades and transmits the event to the DAQ computer over an Ethernet link. While one SRU could support up to 40 blades, this number depends on the speed of the link between the SRU and the DAQ computer. Since this link carries the total data volume from the whole system, it is the speed here that becomes the bottleneck. The currently implemented SRU to DAQ PC speed is 10 Gb/s.
Figure 1: Two views of the ATCA blade – RTM combination the HDMI ports at the front of the ATCA blade connect it to the APV hybrid cards on the detector, while the DTC link at the back of the RTM provides the output to SRU. (Figure from Dr. Hans Muller at CERN)

Figure 2: RTM to SRU and then from SRU to DAQ PC connections.
Proposed Upgrades

1. **OC coupling box**: One critical issue with the implementation described above is that the ATCA crate housing the ATCA blades, which are connected to the APV cards by HDMI cables, has to be located within 5 m of the detector. In the case of SBS this would require the crate to be in a radiation environment. There is a planned upgrade to move the ADC chips from the ATCA blade into a copper to optical coupling box located within a few meters of the detector. This coupling box will be connected to the APV hybrid card on the detector via the HDMI cables and then send the output signals over an optical link to the DAQ crate located in the counting house. Figure 3 shows this proposed scheme.

### SRS Data Transmission from detector to counting room

Figure 3: The proposed scheme to move the SRS electronics crate to a low radiation area by using a optical to copper (OC) coupling box housing the ADC chips. The illustration shows the case for the VMM chip based hybrid cards proposed for ATLAS. The schematic for the SBS case would be similar with the VMM hybrids replaced with APV hybrids.
2. **Link speed upgrade:** In the currently tested architecture, the speed of the RTM to SRU is limited to 1 Gb/s. There are plans to upgrade the link to 10 Gb/s; however, the planned timescale for these upgrades is too far out for SBS. If we need to get these upgrades done sooner, we need to actively participate and contribute to related R&D this summer.

3. **Upgrade to radiation tolerant APV25-SRS Front End card:** Although the APV25 and PLL chips integrated on the APV25-SRS hybrids are specified for radhard operation up to the order of 10 MRad, the linear voltage regulators (LDO) which are used on the hybrids for local power conversion will most likely fail at integrated radiation levels above 0 (20 kRad). APV hybrid revision (APV25-SRSv5) for remote powering via the readout cables is underway. Such a scheme eliminates local voltage regulators from the hybrids. We would need to support this upgrade effort which requires minimal contribution and revisions.

The cost to participate in this upgrade is estimated to be around $20,000. This includes 1.5 months of salary for a CERN electronics engineer, and travel costs to participate in the upgrade and testing. Furthermore, we may have to support the firmware developer for the new architecture (ATCA-Blades, SRU …), a rough estimate for this cost is around $32,500. These development costs are included in the budget table.
DAQ speed:

The following analysis assumes that 10 Gb/s (or 1280 MB/s) links are available from ATCA to SRU and from SRU to PC.

The limiting data acquisition speed for an APV chips arises due to the fact that the outputs from 128 channels is multiplexed into a single serial line. For the 3 sample mode, the time to get the data out of the APV chip is of the order of $10 \mu s$, which give an intrinsic limiting rate of the order of $10^5$ Hz. However, data transmission links downstream of the APV chip limit the actual rate to much smaller values than this.

The tests with the SRS indicated the data volume for one APV card (128 channels) reading 3 samples is approximately 1.2 kB per event for 100% occupancy with no zero suppression. Thus running at 5 kHz, data rate per card would be 6 MB/s at 100% occupancy.

Each ATCA blade supports 48 APV cards, with a total data volume of 288 MB/s going from one ATCA blade to the SRU. This would be well within the 1280 MB/s (10 Gb/s) link planed for this link. However, it should be noted that the currently available 1 Gb/s link would limit the rate to about 2200 Hz.

While one SRU unit is capable of handling up to 40 ATCA blades, the 1280 MB/s link from SRU to DAQ PC will limit this to 5 ATCA blade, with a combined data volume of 1152 GB/s, per SRU/PC combination. Since the SBS back trackers will use a total of 480 APV cards (2880 MB/s), it will require 3 SRU/PC combinations (i.e. 3 CODA ROCs) to handle the total data volume.

Thus, the conclusion is, in the worst case scenario of 100% occupancy, the SRU will be able to take data at 5 kHz, given that we divide the data volume between 3 ROCs.

One important assumption made here is that the CODA will be able to handle and save the data arriving from all detectors at the above rate; this would be a very high rate, over 5 GB/s from the front and back GEM trackers alone. This issue is independent of the readout system used. The amount of data could be reduced by about 50% by using zero suppression. Furthermore, hardware level signal time analysis implemented in the FPGAs of either the ATCA blade (SRS) or the MPD unit (INFN system) could be used to remove about 90% of the background events and cut the data volume by a factor of 10. In addition selective triggering of only parts of the detector could help. However, none of these have been developed yet, and needs to be worked out whether we use SRS of MPD electronics.

The rate considerations for the MPD system are given in the MPD electronics report. Only the following important points for the MPD system are noted here.
1. In the MPD case, the plan is to host 15 APV cards on a single MPD module; therefore the data rate from one MPD would be 90 MB/s at 5 kHz with 100% occupancy; this is too high for the VME bus to handle. Therefore it is essential get the fast optical link from each MPD module to the Jlab SSP module.

2. The back tracker would require 32 MPD modules, these would have to be distributed over several SSP modules. The number of SSP modules needed would depend on the output data link for the SSP modules, which would provide the bottle neck. At 5 kHz with 100% occupancy, the total data rate from 32 MPD modules would be 2880 MB/s (or 23 Gb/s). So it would be desirable to ensure that at least a10 GB/s output link is available from the SSP module; this would make 3 SSP modules sufficient to handle the back tracker. If we are limited to the 5 GB/s VXS bus, we would need 5 SSP module + VXS crate combinations.
The cost of the SRS system

The company producing the SRS systems, EicSys GmbH, has provided us with a quote for an SRS system. The following estimate includes the cost of R&D efforts indicated above.

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<th>Item</th>
<th>Amount</th>
<th>Item Cost</th>
<th>Total</th>
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<td>ATCA crate</td>
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The estimated cost for a SRS system for the SBS back tracker.

The above estimate assumes 2-to-1 strip combination. This combination scheme requires 530 2-to-1 adapters (480 (290) + 10%spares). We estimate that the adapters would cost about $40,000. (Approximately $75 per adapter). This brings the total cost to $372,000.
The cost of the MPD system

For comparison the full cost of a similar sized MPD system is included here; a detailed description of this system could be found on the accompanying report. It should be noted that, the cost of any further R&D that may be required and the cost of firmware development is not added to this estimate. It is likely that these efforts required for the MPD system may be similar or even more than what is required for the SRS system. However, this work has to be done to get the MPD system working for the front tracker anyways, and thus, those costs are not included in this estimate.

<table>
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<th>Item cost Euro</th>
<th>Item Cost</th>
<th>Total</th>
</tr>
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Total                        |        |                |           | $334,263  |

The estimated cost for an MPD system for SBS back-tracker. The cost of any further R&D that may be required and the cost of firmware development is not added to this estimate because this work has to be done to get the MPD system working for the front tracker anyways.
The know-how

Dr. Kondo Gnanvo at UVa has many years of experience running the SRS system. Furthermore, having run the SRS system at UVa under the supervision of Dr. Gnanvo, the graduate students of the group have now gained significant experience in the SRS. The extra manpower requested is for the assembly, testing, and commissioning of the large system required for the SBS backtracker. Whether we use SRS or MPD electronics, this manpower would be required to get the readout system together.

Using SRS for SBS would require incorporating SRS readout into the CODA framework. I believe that given the level of SRS expertise we currently have at UVa this task and associated software migration into hall A analyzer could be done with manpower at hand (i.e. amounts specified in the research management plan), given available help and guidance from the Jlab DAQ group, and the hall A DAQ expert, Dr. Alex Camsonne.

One important fact to point out here that is that the SRS system uses the UDP Ethernet protocol for data transfer between the SRS and the DAQ PC. This protocol has the potential to be unreliable. As such, a knowledgeable expert will be needed to implement the hardware integration of SRS to ensure that no data loss occurs during the SRS to CODA transfer.

System Availability

Assuming that the SRS system upgrade R&D is successfully concluded this summer, it will be available for commercial production in the fall. EicSys GmbH has indicated to us that they can fabricate and deliver the 74,000 channel system within 3 months of receiving the order. Given this timeline we can expect to assemble and test an SRS based readout system for the SBS backtracker by summer 2015.

There is some uncertainty currently about priority assigned to the APV25 based SRS R&D at CERN. The ATLAS collaboration an important and a large prospective user of SRS electronics is trying to push SRS R&D towards the system based on the VMM chip, the readout chip ATLAS plans to use. This is why it is important for us to actively participate in the APV SRS R&D this summer and finalize the system.

Conclusion

With planned upgrades, the SRS will be capable of delivering performance required for the SBS backtracker. The MPD system is also expected to provide similar performance with the upgrades currently underway and planned for the near future. However, using the SRS system has the following advantages
• We could benefit from the SRS expertise already available at UVa.
• The SRS system is backed by the worldwide RD-51 collaboration and by the commercial company EicSys; this company plans to market this system to many clients in the future.

On the other hand using SRS would require some R&D commitment to finalize the system before the production could begin and would require maintaining two parallel readout systems. Getting either system integrated to Jlab DAQ to work at high rates would take a significant amount of expert manpower. Since this work is being done for the MPD system anyways, using MPD for the backtracker could save at least 0.5 FETY of expert manpower.

Our recommendation is that we commit to the relatively small amount of R&D required for SRS this summer, evaluate the finalized system in the fall. In the meantime assemble, setup run and evaluate the new configuration MPD electronics we recently acquired. Then by comparing system performance, firm costs, and production schedules, make a final decision by the end of fall.

References (Attached)

2. Presentations given by Dr. Hans Muller, head of the RD51 electronics working group, on SRS systems.
   a. Presentation given at the RD51 Collaboration Meeting, April 14, 2011: the currently available SRS system.
   b. Presentation given at the RD51 Collaboration Meeting, April 16, 2012: the ATCA based SRS system.