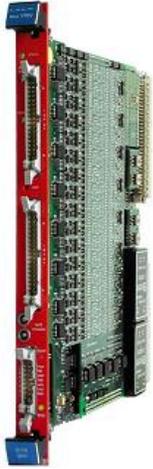


**V792**

**32 Channel Multievent QDC**



- High channel density
- 12-bit resolution
- 5.7  $\mu$ s / 32 ch conversion time
- 600 ns fast clear time
- Zero and overflow suppression for each channel
- $\pm 1.5\%$  differential non linearity
- $\pm 0.1\%$  integral non linearity
- 32 event buffer memory
- BLT32/MBLT64/CBLT32/CBLT64 data transfer
- Multicast commands
- Live insertion
- Libraries, Demos (C and LabView) and Software tools for Windows and Linux

The Mod. V792 is a 1-unit wide VME 6U module housing 32 Charge-to-Digital Conversion channels with current integrating negative inputs (50 Ohm impedance). For each channel, the input charge is converted to a voltage level by a QAC (Charge to Amplitude Conversion) section. Input range is 0  $\div$  400 pC. The outputs of the QAC sections are multiplexed and subsequently converted by two fast 12-bit ADCs. The integral non linearity is  $\pm 0.1\%$  of Full Scale Range (FSR) measured from 5% to 95% of FSR. The ADCs use a sliding scale technique to improve the differential non-linearity. The Mod. V792 offers a 32 event buffer memory, A24/A32 addressing mode, D16, D32, BLT32/MBLT64 and CBLT32/CBLT64 data transfer mode. Multicast commands are also supported. A 16 ch. decoupling board Mod. [A992](#) is available for the Mod. V792 to avoid ground loops and signal reflections when long flat cable (110 Ohm) connections to the 50 Ohm inputs are used (one V792 requires two A992 boards). A 16 channel flat cable to LEMO input adapter, Mod. [A392](#) is also available for the Mod. V792 (one V792 requires two A392 boards). The board supports the live insertion that allows inserting or removing them into the crate without switching it off.

<b>Packaging</b>	1-unit wide 6U VME module (version AA requires the V430 backplane)
<b>Inputs</b>	32 channels, 50 Ohm impedance, negative polarity, DC coupling
<b>Input range</b>	0 $\div$ 400 pC (if Sliding Scale is used FSR is reduced from 4095 to 3840 counts)
<b>Resolution</b>	12 bit
<b>Gain</b>	100 fC/count
<b>Max. tolerated positive voltage input</b>	15 mV
<b>Reflections</b>	< 5% with 2 ns fall time input signals
<b>Input offset</b>	$\pm 2$ mV
<b>RMS Noise</b>	0.5 counts typical
<b>Noise</b>	Gate width (ns) / Iped (count) / Average (count) / ? (count) 100 / 180 / 107.58 / 0.50 500 / 180 / 326.44 / 0.54 1000 / 180 / 597.32 / 0.56 2000 / 180 / 1139.92 / 0.61 Measured with GATE input only (no input on QDC channels)
<b>Integral non linearity</b>	0.1% of FSR (=3840 counts) from 5% to 95% of FSR
<b>Interchannel gain uniformity</b>	$\pm 10\%$

<b>interchannel gain uniformity</b>	±4%
<b>Interchannel Isolation</b>	> 60 dB
<b>Power rejection</b>	0.002 count/mV (+5V); 0.01 count/mV (-5V) 0.0046 count/mV (+12V); 0.0012 count/mV (-12V)
<b>Fast clear time</b>	600 ns
<b>Gate timing</b>	the Gate signal must precede the analog input by > 15 ns
<b>Conversion time</b>	5.7 µs for all channels
<b>Zero suppression</b>	Threshold values programmable in: 16 ADC counts steps over the entire FSR 2 ADC counts steps over 1/8 of FSR
<b>GATE/COM input</b>	NIM signal, high impedance temporal window for current integration
<b>Control inputs</b>	active-high, differential ECL input signals: GATE: temporal window for current integration . RST: resets QAC sections, MEB status and control registers. VETO: inhibits the conversion of the QAC signals. FCLR: FAST CLEAR of QAC sections.
<b>Control outputs</b>	differential ECL output signals: DRDY: indicates the presence of data BUSY: board full, resetting, converting or in MEMORY TEST mode
<b>VME interface</b>	A24/A32 Geographical Addressing Multicast commands D16/D32, BLT32/MBLT64, CBLT32/CBLT64