CAEN Tools for Discovery — Electronic Instrumentation

V792

32 Channel Multievent QDC

- High channel density
- 12-bit resolution
- 5.7 µs / 32 ch conversion time
- 600 ns fast clear time
- Zero and overflow suppression for each channel
- ±1.5% differential non linearity
- ±0.1% integral non linearity
- 32 event buffer memory
- BLT32/MBLT64/CBLT32/CBLT64 data transfer
- Multicast commands
- Live insertion
- Libraries, Demos (C and LabView) and Software tools for Windows and Linux

The Mod. V792 is a 1-unit wide VME 6U module housing 32 Charge-to-Digital Conversion channels with current integrating negative inputs (50 Ohm impedance).
For each channel, the input charge is converted to a voltage level by a QAC (Charge to Amplitude Conversion) section. Input range is 0 ÷ 400 pC.
The outputs of the QAC sections are multiplexed and subsequently converted by two fast 12-bit ADCs.
The integral non linearity is ±0.1% of Full Scale Range (FSR) measured from 5% to 95% of FSR. The ADCs use a sliding scale technique to improve the differential non-linearity.
The Mod. V792 offers a 32 event buffer memory, A24/A32 addressing mode, D16, D32, BLT32/MBLT64 and CBLT32/CBLT64 data transfer mode. Multicast commands are also supported.
A 16 ch. decoupling board Mod. **A992** is available for the Mod. V792 to avoid ground loops and signal reflections when long flat cable (110 Ohm) connections to the 50 Ohm inputs are used (one V792 requires two A992 boards).
A 16 channel flat cable to LEMO input adapter, Mod. **A392** is also available for the Mod. V792 (one V792 requires two A392 boards).
The board supports the live insertion that allows inserting or removing them into the crate without switching it off.

Packaging	1-unit wide 6U VME module (version AA requires the V430 backplane)
Inputs	32 channels, 50 Ohm impedance, negative polarity, DC coupling
Input range	0 ÷ 400 pC (if Sliding Scale is used FSR is reduced from 4095 to 3840 counts)
Resolution	12 bit
Gain	100 fC/count
Max. tolerated positive voltage input	15 mV
Reflections	< 5% with 2 ns fall time input signals
Input offset	±2 mV
RMS Noise	0.5 counts typical
Noise	Gate width (ns) / Iped (count) / Average (count) / ? (count) 100 / 180 / 107.58 / 0.50 500 / 180 / 326.44 / 0.54 1000 / 180 / 597.32 / 0.56 2000 / 180 / 1139.92 / 0.61 Measured with GATE input only (no input on QDC channels)
Integral non linearity	0.1% of FSR (=3840 counts) from 5% to 95% of FSR
Interchannel gain uniformity	±4%

Interchannel gain uniformity	±4%
Interchannel Isolation	> 60 dB
Power rejection	0.002 count/mV (+5V); 0.01 count/mV (-5V) 0.0046 count/mV (+12V); 0.0012 count/mV (-12V)
Fast clear time	600 ns
Gate timing	the Gate signal must precede the analog input by > 15 ns
Conversion time	5.7 µs for all channels
Zero suppression	Treshold values programmable in: 16 ADC counts steps over the entire FSR 2 ADC counts steps over 1/8 of FSR
GATE/COM input	NIM signal, high impedance temporal window for current integration
Control inputs	active-high, differential ECL input signals: GATE: temporal window for current integration . RST: resets QAC sections, MEB status and control registers. VETO: inhibits the conversion of the QAC signals. FCLR: FAST CLEAR of QAC sections.
Control outputs	differential ECL output signals: DRDY: indicates the presence of data BUSY: board full, resetting, converting or in MEMORY TEST mode
VME interface	A24/A32 Geographical Addressing Multicast commands D16/D32,BLT32/MBLT64,CBLT32/CBLT64